PRELIMINARY PRODUCT INFORMATION

NEC

MOS INTEGRATED CIRCUIT

μPD78F4937

16-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F4937, 78K/IV Series' product, is a flash memory version of the μPD784937 with internal masked ROM. Data can be written to or erased from the flash memory of the μPD78F4937 with the microcontroller mounted on the printed wiring board.

For specific functions and other detailed information, consult the following user's manuals.
These manuals are required reading for design work.

μPD784937 Subseries User's Manual, Hardware : To be created
78K/IV Series User's Manual, Instruction : U10905E

FEATURES

- Pin-compatible with mask ROM model (except V_{PP} pin)
- Flash memory: 192K bytes
- Internal RAM: 8,192 bytes
- Same operating voltage as mask ROM model (V_{DD} = 4.0 to 5.5 V)

ORDERING INFORMATION

Part number	Package	Internal ROM
μPD78F4937GC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)	Flash memory
μPD78F4937GF-3BA	100-pin plastic QFP (14 × 20 mm)	Flash memory

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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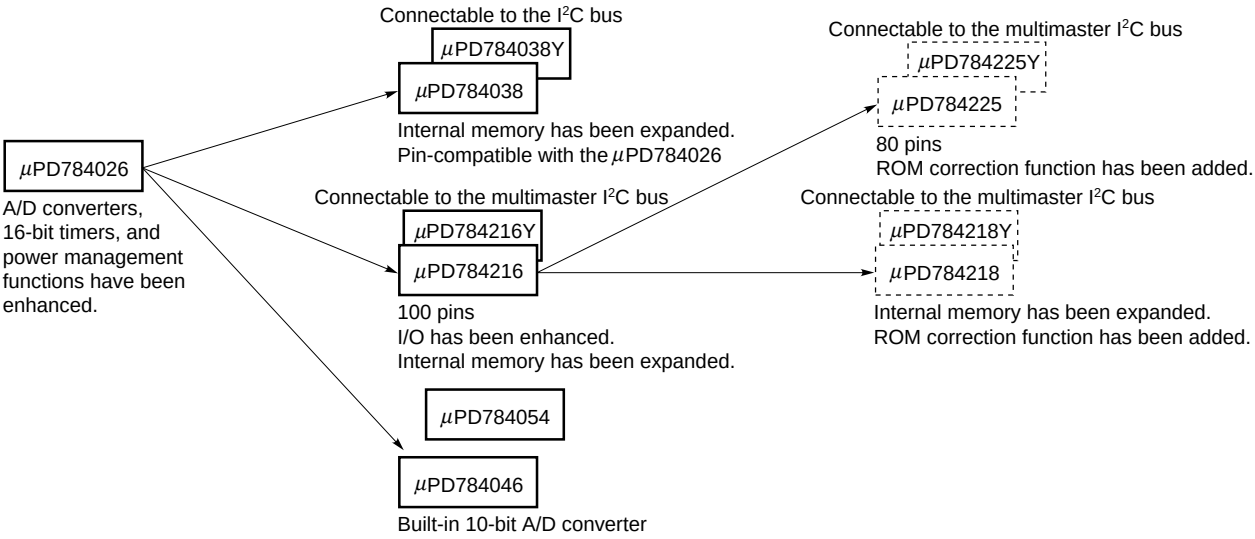
78K/IV SERIES PRODUCT DEVELOPMENT DIAGRAM

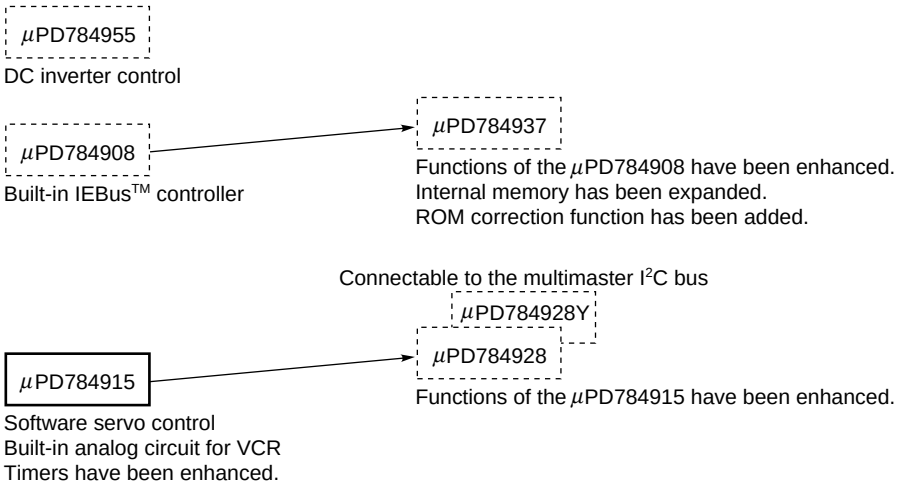
: In production

: Under development

Standard Products Development



ASSP Development



FUNCTIONS

(1/2)

Item		Function
Number of basic instructions (mnemonics)		113
General-purpose register		8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)
Minimum instruction execution time		160 ns/320 ns/636 ns/1.27 μs (at 12.58 MHz)
Internal memory	Flash memory	192K bytes
	RAM	8,192 bytes
Memory space		Program and data: 1M byte
I/O ports	Total	80
	Input	8
	Input/output	72
Additional function pins[Note]	LED direct drive outputs	24
	Transistor direct drive	8
	N-ch open drain	4
Real-time output ports		4 bits × 2, or 8 bits × 1
IEBus controller		Incorporated (simple version)
Timer/counter		Timer/counter 0 (16 bits): Timer register × 1; Capture register × 1; Compare register × 2; Pulse output capability: • Toggle output • PWM/PPG output • One-shot pulse output
		Timer/counter 1 (16 bits): Timer register × 1; Capture register × 1; Capture/compare register × 1; Compare register × 1; Real-time output port
		Timer/counter 2 (16 bits): Timer register × 1; Capture register × 1; Capture/compare register × 1; Compare register × 1; Pulse output capability: • Toggle output • PWM/PPG output
		Timer 3 (16 bits): Timer register × 1; Compare register × 1
Clock timer		Interrupt requests are generated at 0.5-second intervals. (A clock timer oscillator is incorporated.) Either the main clock (12.58 MHz) or real-timer clock (32.768 kHz) can be selected as the input clock.
Clock output		Selected from f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, or $f_{CLK}/16$ (can be used as a 1-bit output port)
PWM outputs		12-bit resolution × 2 channels
Serial interface		UART/IOE (3-wire serial I/O) : 2 channels (incorporating baud rate generator) CSI (3-wire serial I/O) : 2 channels

Note Additional function pins are included in the I/O pins.

(2/2)

Item		Function
A/D converter		8-bit resolution × 8 channels
Watchdog timer		1 channel
ROM correction function		Internal (four correction addresses can be set.)
External expansion function		Provided (up to 1M byte)
Standby		HALT/STOP/IDLE mode
Interrupt	Hardware source	27 (20 internals, 7 externals (sampling clock variable input: 1))
	Software	BRK or BRKCS instruction, operand error
	Nonmaskable	1 internal, 1 external
	Maskable	19 internals, 6 externals
		• 4-level programmable priority • 3 operation statuses: vectored interrupt, macro service, context switching
Power supply voltage		V_{DD} = 4.0 to 5.5 V
Package		• 100-pin plastic LQFP (fine pitch) (14 × 14 mm) • 100-pin plastic QFP (14 × 20 mm)

CONTENTS

1. DIFFERENCES AMONG MODELS IN μPD784937 SUBSERIES

The only difference among the μPD784935, μPD784936, and μPD784937 models lie in the internal memory capacity.

The μPD78F4937 has a 192K-byte flash memory instead of the mask ROM featured by the μPD784935, μPD784936, and μPD784937. Table 1-1 shows the differences among these products.

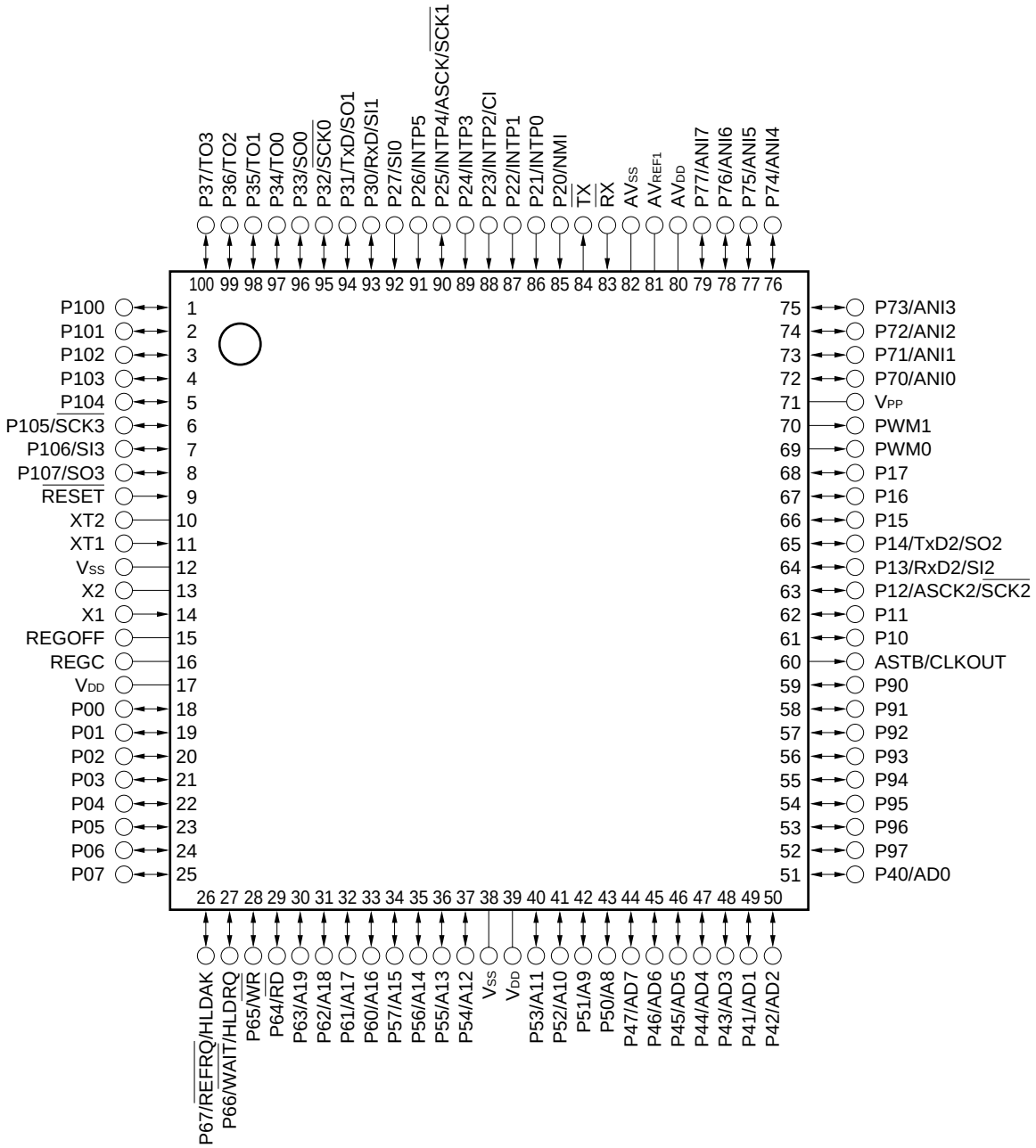
Table 1-1. Differences Among Models in μPD784937 Subseries

Item \ Product	μPD784935	μPD784936	μPD784937	μPD78F4937
Internal ROM	96K bytes	128K bytes	192K bytes	
	Mask ROM			Flash memory
Internal RAM	5,120 bytes	6,656 bytes	8,192 bytes	
Regulator	Provided			None
Internal memory switching register Note	None			Provided
IC pin	Provided			None
V_{PP} pin	None			Provided

Note The internal flash memory capacity and internal RAM capacity can be changed by setting the internal memory switching register (IMS).

2. PIN CONFIGURATION (TOP VIEW)

- **100-pin plastic LQFP (fine pitch) (14 × 14 mm)**
  μPD78F4937GC-8EU

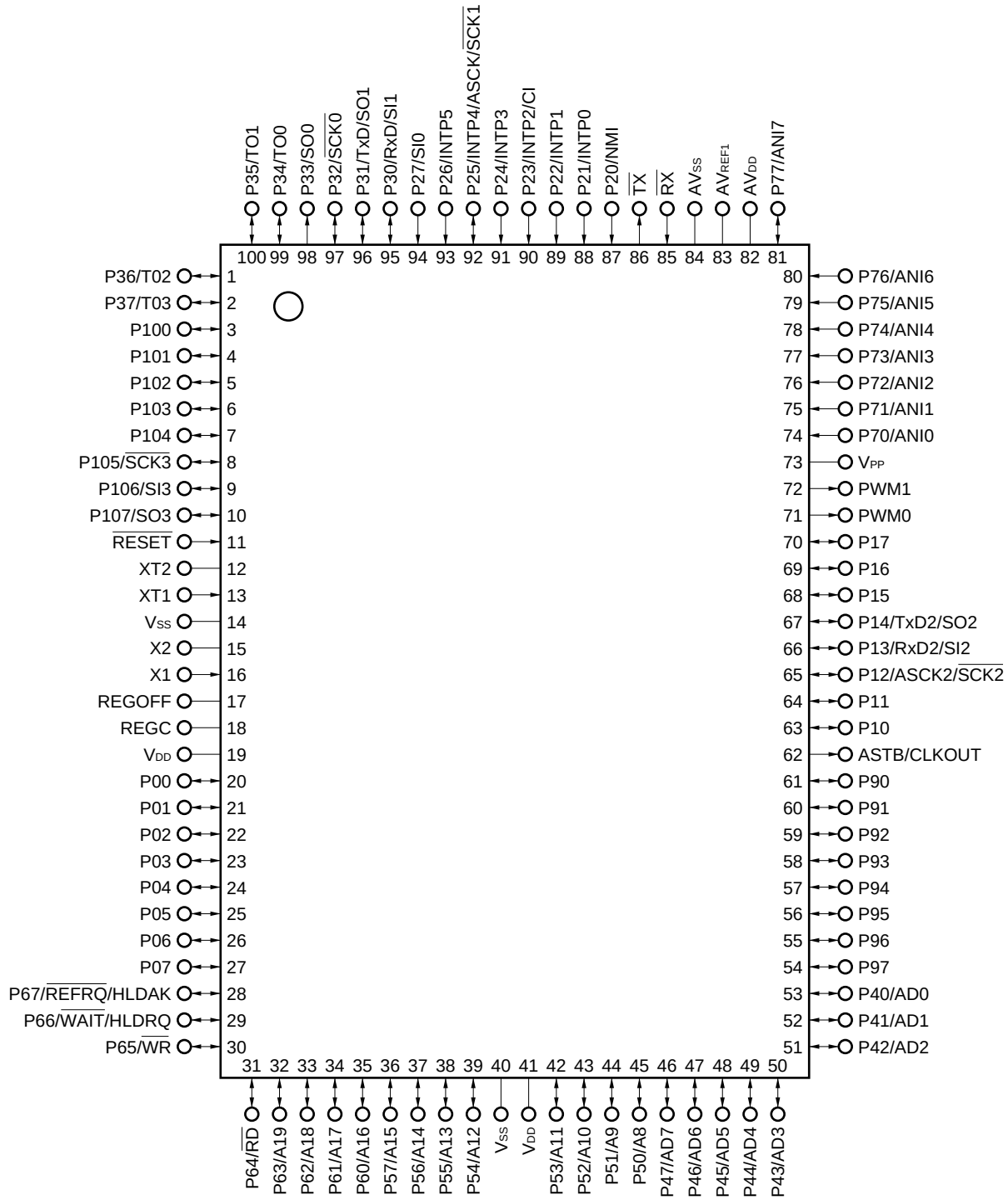


Cautions 1. In normal operation, connect the V_{PP} pin directly to the V_{SS} pin.

2. Connect the AV_{DD} pin directly to the V_{DD} pin.

3. Connect the AV_{SS} pin directly to the V_{SS} pin.

- **100-pin plastic QFP (14 × 20 mm)**
  μPD78F4937GF-3BA



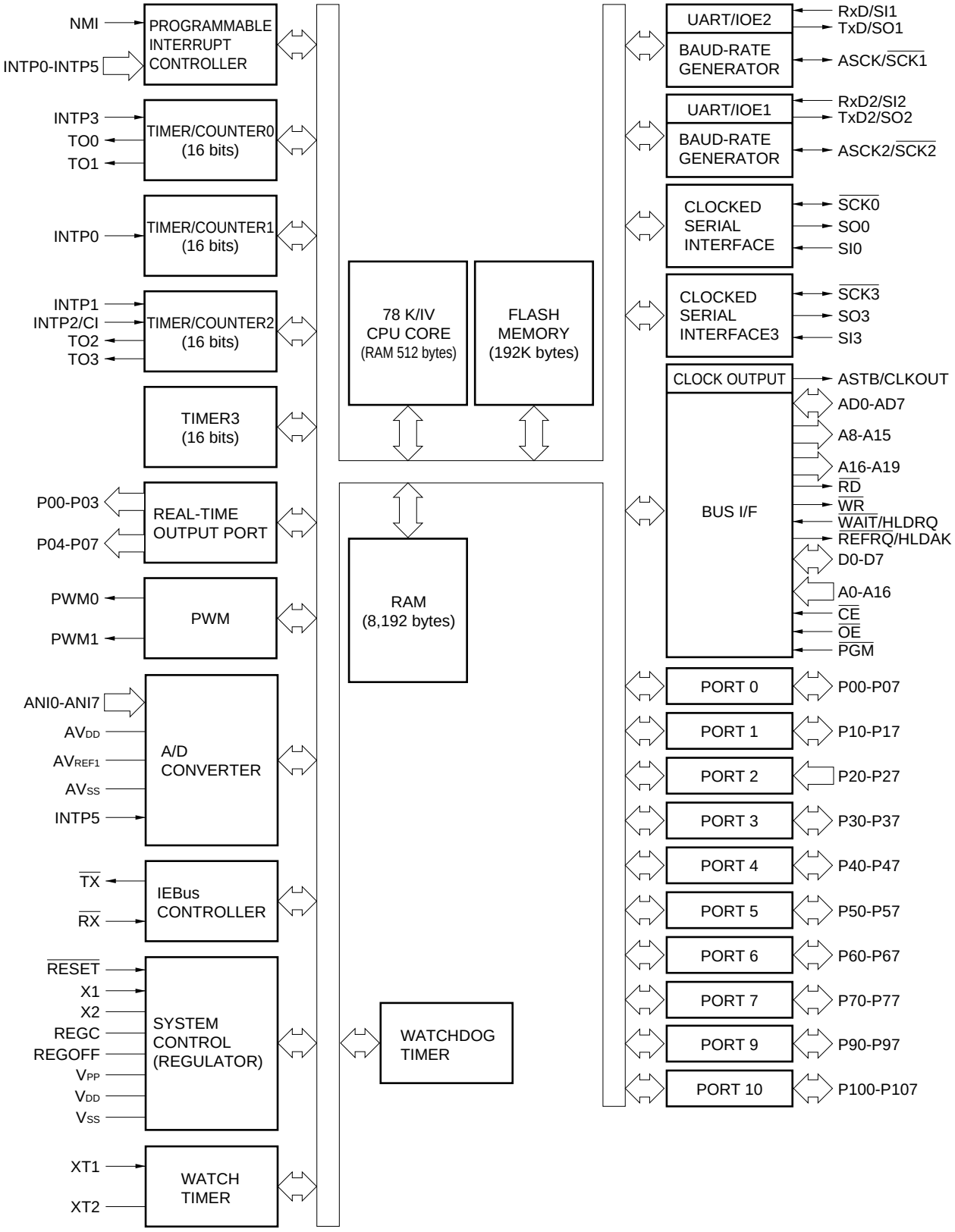
Cautions 1. In normal operation, connect the V_{PP} pin directly to the V_{SS} pin.

2. Connect the AV_{DD} pin directly to the V_{DD} pin.

3. Connect the AV_{SS} pin directly to the V_{SS} pin.

A8-A19	:	Address Bus
AD0-AD7	:	Address/Data Bus
ANI0-ANI7	:	Analog Input
ASCK, ASCK2	:	Asynchronous Serial Clock
ASTB	:	Address Strobe
AV_{DD}	:	Analog Power Supply
AV_{REF1}	:	Reference Voltage
AV_{SS}	:	Analog Ground
CI	:	Clock Input
CLKOUT	:	Clock Output
HLDAK	:	Hold Acknowledge
HLDRQ	:	Hold Request
INTP0-INTP5	:	Interrupt from Peripherals
NMI	:	Non-maskable Interrupt
P00-P07	:	Port 0
P10-P17	:	Port 1
P20-P27	:	Port 2
P30-P37	:	Port 3
P40-P47	:	Port 4
P50-P57	:	Port 5
P60-P67	:	Port 6
P70-P77	:	Port 7
P90-P97	:	Port 9
P100-P107	:	Port 10
PWM0, PWM1	:	Pulse Width Modulation Output
$\overline{RD}$	:	Read Strobe
$\overline{REFRQ}$	:	Refresh Request
REGC	:	Regulator Capacitance
REGOFF	:	Regulator Off
$\overline{RESET}$	:	Reset
$\overline{RX}$	:	IEBus Receive Data
RxD, RxD2	:	Receive Data
$\overline{SCK0}$-$\overline{SCK3}$	:	Serial Clock
SI0-SI3	:	Serial Input
SO0-SO3	:	Serial Output
TO0-TO3	:	Timer Output
$\overline{TX}$	:	IEBus Transmit Data
TxD, TxD2	:	Transmit Data
V_{DD}	:	Power Supply
V_{PP}	:	Programming Power Supply
V_{SS}	:	Ground
$\overline{WAIT}$	:	Wait
$\overline{WR}$	:	Write Strobe
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Watch)

3. BLOCK DIAGRAM



4. LIST OF PIN FUNCTIONS

4.1 Port Pins (1/2)

Pin	I/O	Dual-function	Function
P00-P07	I/O	–	Port 0 (P0): • 8-bit I/O port. • Functions as a real-time output port (4 bits × 2). • Inputs and outputs can be specified bit by bit. • The use of pull-up resistors can be simultaneously specified by software for all pins in input mode. • Can drive a transistor.
P10	I/O	–	Port 1 (P1): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of pull-up resistors can be simultaneously specified by software for all pins in input mode. • Can drive LED.
P11		–	
P12		ASCK2/$\overline{\text{SCK2}}$	
P13		RxD2/SI2	
P14		TxD2/SO2	
P15-P17		–	
P20	Input	NMI	Port 2 (P2): • 8-bit input-only port. • P20 does not function as a general-purpose port (nonmaskable interrupt). However, the input level can be checked by an interrupt service routine. • The use of pull-up resistors can be specified by software for pins P22 to P27 (in units of 6 bits). • The P25/INTP4/ASCK/$\overline{\text{SCK1}}$ pin functions as the $\overline{\text{SCK1}}$ I/O pin by CSIM1.
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK/$\overline{\text{SCK1}}$	
P26		INTP5	
P27		SI0	
P30	I/O	RxD/SI1	Port 3 (P3): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of pull-up resistors can be simultaneously specified by software for all pins in input mode. • P32 and P33 can be set as the N-ch open-drain pin.
P31		TxD/SO1	
P32		$\overline{\text{SCK0}}$	
P33		SO0	
P34-P37		TO0-TO3	
P40-P47	I/O	AD0-AD7	Port 4 (P4): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of pull-up resistors can be simultaneously specified by software for all pins in input mode. • Can drive LED.

4.1 Port Pins (2/2)

Pin	I/O	Dual-function	Function
P50-P57	I/O	A8-A15	Port 5 (P5): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of pull-up resistors can be simultaneously specified by software for all pins in input mode. • Can drive LED.
P60-P63	I/O	A16-A19	Port 6 (P6): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of pull-up resistors can be simultaneously specified by software for all pins in input mode.
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$/HLDRQ	
P67		$\overline{REFRQ}$/HLDAK	
P70-P77	I/O	ANI0-ANI7	Port 7 (P7): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit.
P90-P97	I/O	–	Port 9 (P9): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of pull-up resistors can be simultaneously specified by software for all pins in input mode.
P100-P104	I/O	–	Port 10 (P10): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of pull-up resistors can be simultaneously specified by software for all pins in input mode. • P105 and P107 can be set as the N-ch open-drain pin.
P105		$\overline{SCK3}$	
P106		SI3	
P107		SO3	

4.2 Non-Port Pins (1/2)

Pin	I/O	Dual-function	Function	
TO0-TO3	Output	P34-P37	Timer output	
CI	Input	P23/INTP2	Input of a count clock for timer/counter 2	
RxD	Input	P30/SI1	Serial data input (UART0)	
RxD2		P13/SI2	Serial data input (UART2)	
TxD	Output	P31/SO1	Serial data output (UART0)	
TxD2		P14/SO2	Serial data output (UART2)	
ASCK	Input	P25/INTP4/$\overline{SCK1}$	Baud rate clock input (UART0)	
ASCK2		P12/$\overline{SCK2}$	Baud rate clock input (UART2)	
SI0	Input	P27	Serial data input (3-wire serial I/O0)	
SI1		P30/RxD	Serial data input (3-wire serial I/O1)	
SI2		P13/RxD2	Serial data input (3-wire serial I/O2)	
SI3		P106	Serial data input (3-wire serial I/O3)	
SO0	Output	P33	Serial data output (3-wire serial I/O0)	
SO1		P31/TxD	Serial data output (3-wire serial I/O1)	
SO2		P14/TxD2	Serial data output (3-wire serial I/O2)	
SO3		P107	Serial data output (3-wire serial I/O3)	
$\overline{SCK0}$	I/O	P32	Serial clock I/O (3-wire serial I/O0)	
$\overline{SCK1}$		P25/INTP4/ASCK	Serial clock I/O (3-wire serial I/O1)	
$\overline{SCK2}$		P12/ASCK	Serial clock I/O (3-wire serial I/O2)	
$\overline{SCK3}$		P105	Serial clock I/O (3-wire serial I/O3)	
NMI	Input	P20	External interrupt request	–
INTP0		P21		• Input of a count clock for timer/counter 1 • Capture/trigger signal for CR11 or CR12
INTP1		P22		• Input of a count clock for timer/counter 2 • Capture/trigger signal for CR22
INTP2		P23/CI		• Input of a count clock for timer/counter 2 • Capture/trigger signal for CR21
INTP3		P24		• Input of a count clock for timer/counter 0 • Capture/trigger signal for CR02
INTP4		P25/ASCK/$\overline{SCK1}$		–
INTP5		P26		Input of a conversion start trigger for A/D converter
AD0-AD7	I/O	P40-P47	Time multiplexing address/data bus (for connecting external memory)	
A8-A15	Output	P50-P57	High-order address bus (for connecting external memory)	
A16-A19	Output	P60-P63	High-order address during address expansion (for connecting external memory)	
$\overline{RD}$	Output	P64	Strobe signal output for reading the contents of external memory	
$\overline{WR}$	Output	P65	Strobe signal output for writing on external memory	
$\overline{WAIT}$	Input	P66/HLDRQ	Wait signal insertion	
$\overline{REFRQ}$	Output	P67/HLDAK	Refresh pulse output to external pseudo static memory	
HLDRQ	Input	P66/$\overline{WAIT}$	Input of bus hold request	
HLDAK	Output	P67/$\overline{REFRQ}$	Output of bus hold response	
ASTB	Output	CLKOUT	Latch timing output of time multiplexing address (A0-A7) (for connecting external memory)	

4.2 Non-Port Pins (2/2)

Pin	I/O	Dual-function	Function
CLKOUT	Output	ASTB	Clock output
PWM0	Output	–	PWM output 0
PWM1	Output	–	PWM output 1
$\overline{RX}$	Input	–	Data input (IEBus)
$\overline{TX}$	Output	–	Data output (IEBus)
REGC	–	–	Capacitor connection for stabilizing the regulator output
REGOFF	–	–	Signal for specifying regulator operation
$\overline{RESET}$	Input	–	Chip reset
X1	Input	–	Crystal input for system clock oscillation (A clock pulse can also be input to the X1 pin.)
X2	–		
XT1	Input	–	Real-time clock connection pin
XT2	–	–	
ANI0-ANI7	Input	P70-P77	Analog voltage inputs for the A/D converter
AV_{REF1}	–	–	Application of A/D converter reference voltage
AV_{DD}			Positive power supply for the A/D converter
AV_{SS}			Ground for the A/D converter
V_{DD}			Positive power supply
V_{SS}			Ground
V_{PP}	Input		This pin is used to set the flash memory programming mode and applies a high voltage when a program is written or verified. In normal operation mode, connect this pin directly to the V_{SS} pin.

4.3 I/O Circuits for Pins and Handling of Unused Pins

Table 4-1 describes the types of I/O circuits for pins and the handling of unused pins.
Figure 4-1 shows the configuration of these various types of I/O circuits.

Table 4-1. Types of I/O Circuits for Pins and Handling of Unused Pins (1/2)

Pin	I/O circuit type	I/O	Recommended connection method for unused pins
P00-P07	5-A	I/O	Input state: Connect these pins to the V_{DD} pin. Output state: Leave these pins open.
P10, P11			
P12/ASCK2/$\overline{SCK2}$	8-A		
P13/RxD2/SI2	5-A		
P14/TxD2/SO2			
P15-P17			
P20/NMI	2	Input	Connect these pins to the V_{DD} or V_{SS} pin.
P21/INTP0			
P22/INTP1	2-A		Connect these pins to the V_{DD} pin.
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK/$\overline{SCK1}$	8-A	I/O	Input state: Connect this pin to the V_{DD} pin. Output state: Leave this pin open.
P26/INTP5	2-A	Input	Connect these pins to the V_{DD} pin.
P27/SI0			
P30/RxD/SI1	5-A	I/O	Input state: Connect these pins to the V_{DD} pin. Output state: Leave these pins open.
P31/TxD/SO1			
P32/$\overline{SCK0}$	10-A		
P33/SO0			
P34/TO0-P37/TO3	5-A		
P40/AD0-P47/AD7			
P50/A8-P57/A15			
P60/A16-P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$/HLDRQ			
P67/$\overline{REFRQ}$/HLDAK			
P70/ANI0-P77/ANI7	20	I/O	Input state: Connect these pins to the V_{DD} or V_{SS} pin. Output state: Leave these pins open.
P90-P97	5-A		
P100-P104			
P105/$\overline{SCK3}$	10-A		
P106/SI3	8-A		
P107/SO3	10-A		
ASTB/CLKOUT	4	Output	Leave this pin open.

Table 4-1. Types of I/O Circuits for Pins and Handling of Unused Pins (2/2)

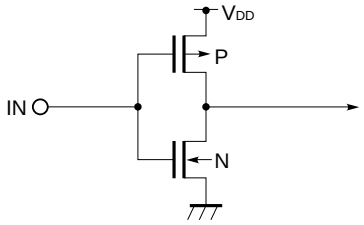
Pin	I/O circuit type	I/O	Recommended connection method for unused pins
$\overline{\text{RESET}}$	2	Input	–
XT2	–	–	Leave this pin open.
XT1	–	Input	Connect this pin to the V_{SS} pin.
REGOFF	1	–	Connect these pins to the V_{DD} pin.
REGC	–	–	
PWM0, PWM1	3	Output	Leave this pin open.
$\overline{\text{RX}}$	2	Input	Connect this pin to the V_{DD} or V_{SS} pin.
$\overline{\text{TX}}$	3	Output	Leave this pin open.
AV_{REF1}	–	–	Connect these pins to the V_{SS} pin.
AV_{SS}			
AV_{DD}			Connect this pin to the V_{DD} pin.
V_{PP}		Input	Connect this pin directly to the V_{SS} pin.

Caution When the I/O mode of an I/O dual-function pin is unpredictable, connect the pin to V_{DD} through a resistor of 10 to 100 kilohms (particularly when the voltage of the reset input pin becomes higher than that of the low level input at power-on or when I/O is switched by software).

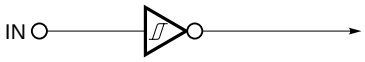
Remark Since type numbers are consistent in the 78K Series, those numbers are not always serial in each product. (Some circuits are not included.)

Figure 4-1. I/O Circuits for Pins

Type 1

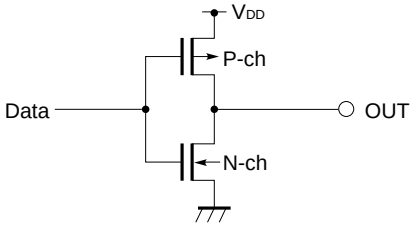


Type 2

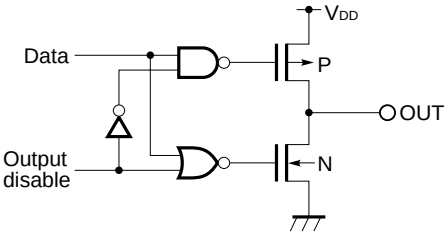


Schmitt trigger input with hysteresis characteristics

Type 3

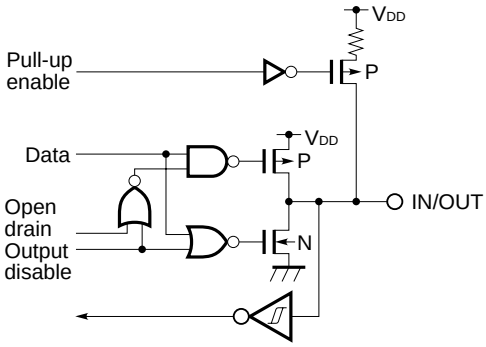


Type 4

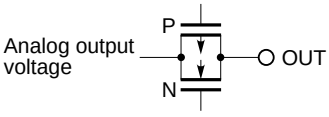


Push-pull output which can output high impedance
(both the positive and negative channels are off.)

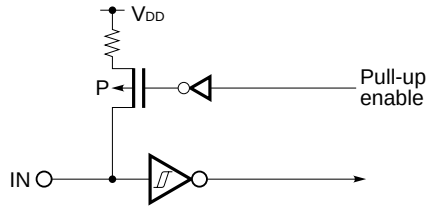
Type 10-A



Type 12

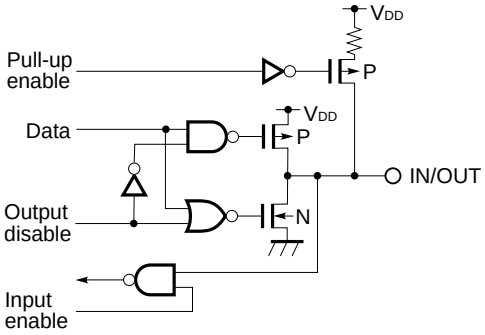


Type 2-A

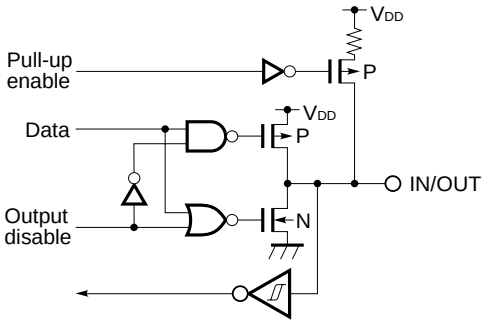


Schmitt trigger input with hysteresis characteristics

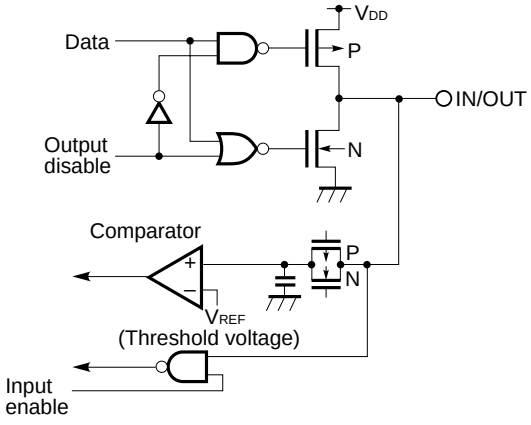
Type 5-A



Type 8-A



Type 20



5. INTERNAL MEMORY SWITCHING (IMS) REGISTER

This register enables the software to avoid using part of the internal memory. The IMS register can be set to establish the same memory mapping as used in ROM products that have different internal memory (ROM and RAM) configurations.

The IMS register is set using 8-bit memory operation instructions.

A $\overline{\text{RESET}}$ input sets the IMS register to FFH.

Figure 5-1. Internal Memory Switching (IMS) Register

Address: 0FFFCH When reset: FFH W/R

	7	6	5	4	3	2	1	0
IMS	1	1	ROM1	ROM0	1	1	RAM1	RAM0

ROM1	ROM0	Internal ROM capacity selection
0	0	Not to be set
0	1	96K bytes
1	0	128K bytes
1	1	192K bytes

RAM1	RAM0	Internal RAM capacity selection
0	0	Not to be set
0	1	5,120 bytes
1	0	6,656 bytes
1	1	8,192 bytes

Caution The IMS is not contained in a mask ROM product (μPD784935, μPD784936, or μPD784937).

The IMS setting to obtain the same memory map as masked ROM products are shown in Table 5-1.

Table 5-1. Internal Memory Switching Register (IMS) Setting Value

Product	IMS setting value
μPD784935	DDH
μPD784936	EEH
μPD784937	FFH

6. FLASH MEMORY PROGRAMMING

The flash memory can be written even while the device is mounted in the target system (on-board write). To write a program into the flash memory, connect the dedicated flash writer (Flashpro III) to both the host machine and target system.

Remark The Flashpro III is manufactured by Naito Densei Machida Mfg. Co., Ltd.

6.1 Selecting the Transmission Method

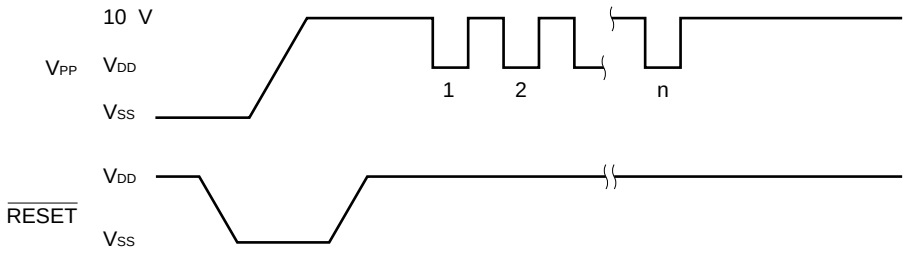
The Flashpro III writes into flash memory by means of serial transmission. The transmission method to be used for writing is selected from those listed in Table 6-1. To select a transmission method, use the format shown in Figure 6-1, according to the number of V_{PP} pulses listed in Table 6-1.

Table 6-1. Transmission Methods

Transmission method	Number of channels	Pins	Number of V_{PP} pulses
3-wire serial I/O	1	$\overline{SCK3}$/P105 SO3/P107 SI3/P106	0
UART	1	TxD/SO1/P31 RxD/SI1/P30	8

Caution To select a transmission method, always use the corresponding number of V_{PP} pulses listed in Table 6-1.

Figure 6-1. Format of Transmission Method Selection



6.2 Flash Memory Programming Functions

Flash memory writing and other operations can be performed by transmitting/receiving commands and data according to the selected transmission method. Table 6-2 lists the main flash memory programming functions.

Table 6-2. Main Flash Memory Programming Functions

Function	Description
Batch erase	Erases the entire contents of memory.
Block erase	Erases the contents of specified memory block.
Batch blank check	Checks that the entire contents of memory have been erased.
Block blank check	Checks that the contents of specified block have been erased.
Data write	Write to the flash memory according to the specified write start address and number of bytes of data to be written.
Batch verify	Compares the entire contents of memory with the input data.
Block verify	Compares the contents of specified memory block with the input data.

6.3 Connecting the Flashpro III

The connection between the Flashpro III and μPD78F4937 varies with the transmission method. Figures 6-2 and 6-3 show the connection for each transmission method.

Figure 6-2. Flashpro III Connection in 3-Wire Serial I/O Mode

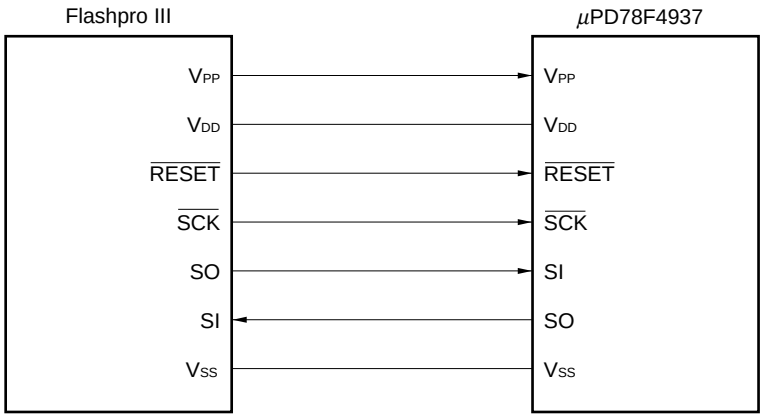
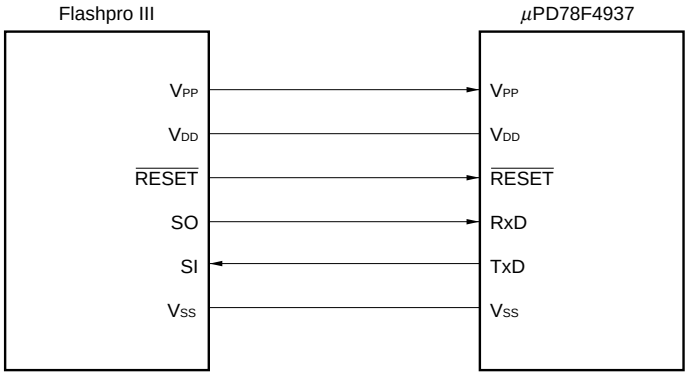
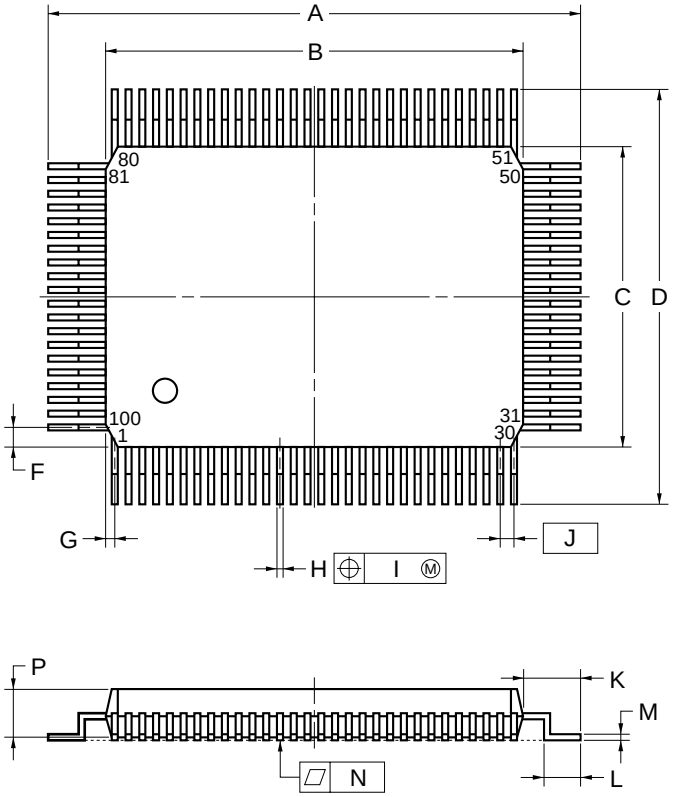


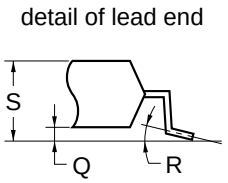
Figure 6-3. Flashpro III Connection in UART Mode



7. PACKAGE DRAWINGS

100PIN PLASTIC QFP (14x20)





NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

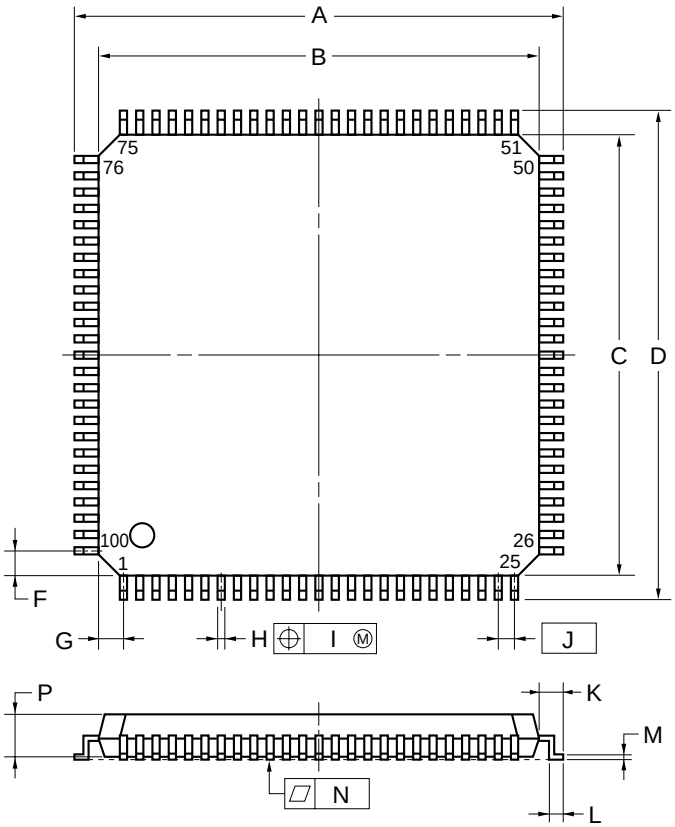
REMARK

The shape and material of the ES product is the same as the mass produced product.

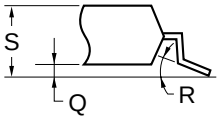
ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P100GF-65-3BA1-3

100 PIN PLASTIC LQFP (FINE PITCH) (14×14)



detail of lead end



NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

REMARK

The shape and material of the ES product is the same as the mass produced product.

ITEM	MILLIMETERS	INCHES
A	16.00±0.20	0.630±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.08	0.003
P	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.	0.063 MAX.

S100GC-50-8EU

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F4937.
See also **(5)**.

(1) Language processing software

RA78K4	Assembler package used in common with 78K/IV Series
CC78K4	C compiler package used in common with 78K/IV Series
DF784937	Device file for μPD784937 Subseries
CC78K4-L	C compiler library source file used in common with 78K/IV Series

(2) Flash memory write tools

Flashpro III[Note] (PG-FPIII)	Flash writer used only for microcontrollers with internal flash memory
FA-100GF	Flash memory writing adapter for 100-pin plastic QFP (GF-3BA type). Wiring must be performed according to product being used.
FA-100GC	Flash memory writing adapter for 100-pin plastic LQFP (GC-8EU type). Wiring must be performed according to product being used.
Flashpro III controller[Note]	Program controlled by a personal computer and which is supported by Flashpro III. Runs under Windows™95, etc.

(3) Debugging tools

- **When using the in-circuit emulator IE-78K4-NS**

IE-78K4-NS	In-circuit emulator used in common with 78K/IV Series
IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
IE-70000-98-IF-C	Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine
IE-70000-CD-IF-C	PC card and interface cable when a PC-9800 series notebook is used as the host machine
IE-70000-PC-IF-C	Interface adapter when the IBM PC/AT™ compatible is used as the host machine
IE-784937-NS-EM1[Note]	Emulation board for emulating μPD784937 Subseries
NP-100GF	Emulation probe for 100-pin plastic QFP (GF-3BA type)
NP-100GC	Emulation probe for 100-pin plastic LQFP (GC-8EU type)
EV-9200-GF-100	Socket for mounting on target system board made for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter for connecting the target system board made for 100-pin plastic LQFP (GC-8EU type) with NP-100GC
ID78K4-NS	Integrated debugger for IE-78K4-NS
SM78K4	System simulator used in common with 78K/IV Series
DF789437	Device file for μPD784937 Subseries

Note Under development

- **When using the in-circuit emulator IE-784000-R**

IE-784000-R	In-circuit emulator used in common with 78K/IV Series
IE-70000-98-IF-B IE-70000-98-IF-C	Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine
IE-70000-98N-IF	Interface adapter and cable when a PC-9800 series notebook is used as the host machine
IE-70000-PC-IF-B IE-70000-PC-IF-C	Interface adapter when the IBM PC/AT compatible is used as the host machine
IE-78000-R-SV3	Interface adapter and cable when the EWS is used as the host machine
IE-784937-NS-EM1[Note] IE-784937-R-EM1[Note]	Emulation board for emulating μPD784937 Subseries
IE-78400-R-EM	Emulation board used in common with 78K/IV Series
IE-78K4-R-EX2[Note]	Conversion board for emulation probes required to use the IE-784937-NS-EM1 on the IE-784000-R. The board is not needed when the IE-784937-R-EM1 is used.
EP-78064GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EP-78064GC-R	Emulation probe for 100-pin plastic LQFP (GC-8EU type)
EV-9200GF-100	Socket for mounting on target system board made for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter for connecting the target system board made for 100-pin plastic LQFP (GC-8EU type) with NP-100GC
ID78K4	Integrated debugger for IE-784000-R
SM78K4	System simulator used in common with 78K/IV Series
DF784937	Device file for μPD784937 Subseries

Note Under development

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV Series
MX78K4	OS for the 78K/IV Series

(5) Notes when using development tools

- The ID78K4-NS, ID78K4, and SM78K4 can be used in combination with the DF784937.
- The CC78K4 and RX78K/IV can be used in combination with the RA78K4 and DF784937.
- The Flashpro III, FA-100GF, FA-100GC, NP-100GF, and NP-100GC are manufactured by Naito Densei Machida Mfg. Co., Ltd. (044-822-3813). Consult the NEC sales representative for purchasing.
- The TGC-100SDW is a product from TOKYO ELETECH CORPORATION.
  Refer to: Daimaru Kogyo, Ltd.
  Tokyo Electronic Components Division (03-3820-7112)
  Osaka Electronic Components Division (06-244-6672)
- The host machines and operating systems corresponding to each software are shown below.

Host machine / [OS] / Software	PC	EWS
	PC-9800 series [Windows] IBM PC/AT compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K4	O Note	O
CC78K4	O Note	O
ID78K4-NS	O	–
ID78K4	O	O
SM78K4	O	–
RX78K/IV	O Note	O
MX78K4	O Note	O

Note Software under MS-DOS

APPENDIX B RELATED DOCUMENTS

- **Documents Related to Devices**

Document name	Document No.	
	Japanese	English
μPD784935, 784936, 784937 Preliminary Product Information	U13572J	To be created
μPD78F4937 Preliminary Product Information	U13573J	This manual
μPD784937 Subseries User's Manual, Hardware	To be created	To be created
μPD784937 Subseries Special Function Registers	To be created	–
78K/IV Series User's Manual, Instruction	U10905J	U10905E
78K/IV Series Instruction Summary Sheet	U10594J	–
78K/IV Series Instruction Set	U10595J	–
78K/IV Series Application Note, Software Basic	U10095J	U10095E

- **Documents Related to Development Tools (User's Manual)**

Document name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	U11334J	U11334E
	Language	U11162J	U11162E
RA78K Series Structured Assembler Preprocessor		U11743J	U11743E
CC78K Series C Compiler	Operation	U11571J	U11571E
	Language	U11572J	U11572E
IE-78K4-NS		U13356J	To be created
IE-784000-R		U12903J	EEU-1534
IE-784937-R-EM1		To be created	To be created
IE-784937-NS-EM1		To be created	To be created
EP-78064		EEU-934	EEU-1469
SM78K4 System Simulator Windows Base	Reference	U10093J	U10093E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E
ID78K4-NS Integrated Debugger	Reference	U12796J	U12796E
ID78K4 Integrated Debugger Windows Base	Reference	U10440J	U10440E
ID78K4 Integrated Debugger HP-UX, SunOS, NEWS-OS Base	Reference	U11960J	U11960E

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

- **Documents Related to Software to Be Incorporated into the Product (User's Manual)**

Document name		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Basic	U10603J	U10603E
	Installation	U10604J	U10604E
	Debugger	U10364J	–
OS for 78K/IV Series MX78K4		U11779J	–

- **Other Documents**

Document name	Document No.	
	Japanese	English
IC PACKAGE MANUAL	C10943X	
SMD Surface Mount Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Semiconductor Device Quality Control/Reliability Handbook	C12769J	–
Guide for Products Related to Microcomputer: Other Companies	U11416J	–

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.1.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

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Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
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NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
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NEC Electronics Hong Kong Ltd.
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Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
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Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-719-2377
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NEC do Brasil S.A.
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Fax: 011-6465-6829

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Some related documents may be preliminary versions. Note that, however, what documents are preliminary is not indicated in this document.

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