PRELIMINARY PRODUCT INFORMATION

MOS INTEGRATED CIRCUIT μ PD78F4937

16-BIT SINGLE-CHIP MICROCONTROLLER

The μ PD78F4937, 78K/IV Series' product, is a flash memory version of the μ PD784937 with internal masked ROM. Data can be written to or erased from the flash memory of the μ PD78F4937 with the microcontroller mounted on the printed wiring board.

For specific functions and other detailed information, consult the following user's manuals.

These manuals are required reading for design work.

μPD784937 Subseries User's Manual, Hardware : To be created 78K/IV Series User's Manual, Instruction : U10905E

FEATURES

NEC

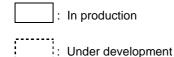
- Pin-compatible with mask ROM model (except VPP pin)
- Flash memory: 192K bytes
- Internal RAM: 8,192 bytes
- Same operating voltage as mask ROM model (VDD = 4.0 to 5.5 V)

ORDERING INFORMATION

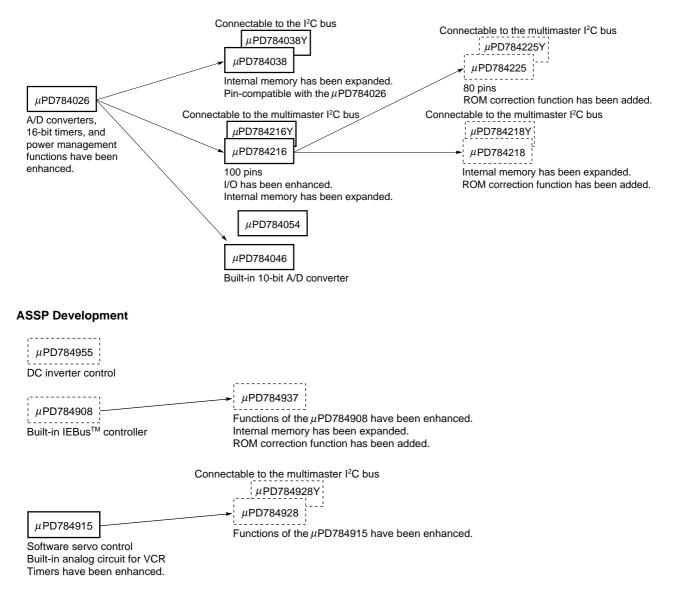
| Part number | Package | Internal ROM |
|------------------|--|--------------|
| μΡD78F4937GC-8EU | 100-pin plastic LQFP (fine pitch) (14 $	imes$ 14 mm) | Flash memory |
| μΡD78F4937GF-3BA | 100-pin plastic QFP (14 $	imes$ 20 mm) | Flash memory |

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

78K/IV SERIES PRODUCT DEVELOPMENT DIAGRAM



Standard Products Development



FUNCTIONS

| Item | | | Function | | | | | | | | |
|--|---------------------|--------------------------------|---|--|--|--|--|--|--|--|--|
| Number of basic instructions (mnemonics) | | | 113 | 113 | | | | | | | |
| Ge | eneral-purpose | e register | 8 bits × 16 registers | s \times 8 banks, or 16 bits \times 8 regist | ters $	imes$ 8 banks (memory mapping) | | | | | | |
| Miı tim | | tion execution | 160 ns/320 ns/636 | ns/1.27 μs (at 12.58 MHz) | | | | | | | |
| Int | ernal | Flash memory | 192K bytes | | | | | | | | |
| me | emory | RAM | 8,192 bytes | | | | | | | | |
| Me | emory space | | Program and data: | 1M byte | | | | | | | |
| I/O |) ports | Total | 80 | | | | | | | | |
| | | Input | 8 | | | | | | | | |
| | | Input/output | 72 | | | | | | | | |
| | Additional function | LED direct drive outputs | 24 | | | | | | | | |
| | Note pins | Transistor direct drive | 8 | | | | | | | | |
| | | N-ch open drain | 4 | | | | | | | | |
| Re | al-time outpu | t ports | 4 bits \times 2, or 8 bits | × 1 | | | | | | | |
| IEE | Bus controller | | Incorporated (simple version) | | | | | | | | |
| Tin | ner/counter | | Timer/counter 0 : (16 bits) | Timer register \times 1 Capture register \times 1 Compare register \times 2 | Pulse output capability Toggle output PWM/PPG output One-shot pulse output | | | | | | |
| | | | Timer/counter 1 : (16 bits) | Timer register \times 1 Capture register \times 1 Capture/compare register \times 1 Compare register \times 1 | Real-time output port | | | | | | |
| | | Timer/counter 2 : (16 bits) | Timer register \times 1 Capture register \times 1 Capture/compare register \times 1 Compare register \times 1 | Pulse output capability Toggle output PWM/PPG output | | | | | | | |
| | | | Timer 3 : (16 bits) | Timer register \times 1 Compare register \times 1 | | | | | | | |
| Clock timer | | | Interrupt requests are generated at 0.5-second intervals. (A clock timer oscillator is incorporated.) Either the main clock (12.58 MHz) or real-timer clock (32.768 kHz) can be selected as the input clock. | | | | | | | | |
| Clo | ock output | | Selected from fclk, fclk/2, fclk/4, fclk/8, or fclk/16 (can be used as a 1-bit output port) | | | | | | | | |
| P٧ | VM outputs | | 12-bit resolution × 2 | 2 channels | | | | | | | |
| Se | rial interface | | UART/IOE (3-wire serial I/O) : 2 channels (incorporating baud rate generator) CSI (3-wire serial I/O) : 2 channels | | | | | | | | |

Note Additional function pins are included in the I/O pins.

(2/2)

| lte | em | Function | | | | |
|----------------------|-----------------|---|--|--|--|--|
| A/D converter | - | 8-bit resolution × 8 channels | | | | |
| Watchdog timer | | 1 channel | | | | |
| ROM correction t | function | Internal (four correction addresses can be set.) | | | | |
| External expansi | on function | Provided (up to 1M byte) | | | | |
| Standby | | HALT/STOP/IDLE mode | | | | |
| Interrupt | Hardware source | 27 (20 internals, 7 externals (sampling clock variable input: 1)) | | | | |
| | Software | BRK or BRKCS instruction, operand error | | | | |
| | Nonmaskable | 1 internal, 1 external | | | | |
| | Maskable | 19 internals, 6 externals | | | | |
| | | 4-level programmable priority 3 operation statuses: vectored interrupt, macro service, context switching | | | | |
| Power supply voltage | | V _{DD} = 4.0 to 5.5 V | | | | |
| Package | | 100-pin plastic LQFP (fine pitch) (14 × 14 mm) 100-pin plastic QFP (14 × 20 mm) | | | | |

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1. DIFFERENCES AMONG MODELS IN μ PD784937 SUBSERIES

The only difference among the μ PD784935, μ PD784936, and μ PD784937 models lie in the internal memory capacity.

The μ PD78F4937 has a 192K-byte flash memory instead of the mask ROM featured by the μ PD784935, μ PD784936, and μ PD784937. Table 1-1 shows the differences among these products.

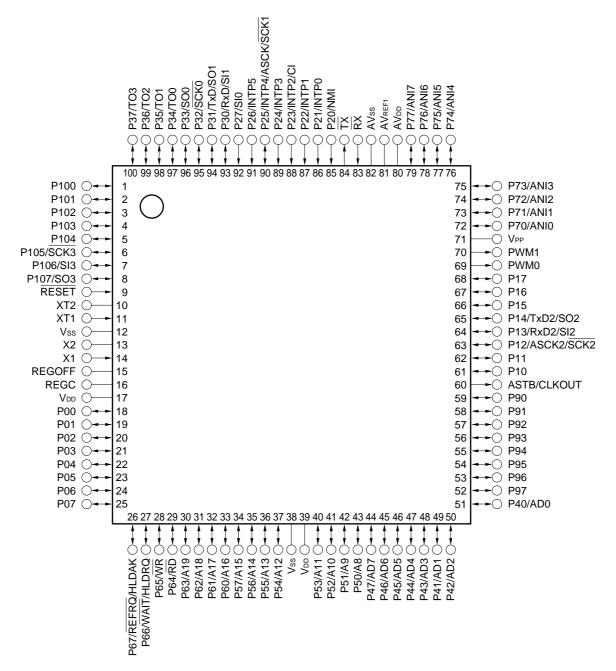
| Table 1-1. | Differences Amon | g Models in | µPD784937 | Subseries |
|------------|------------------|-------------|-----------|-----------|
|------------|------------------|-------------|-----------|-----------|

| Product | μPD784935 | μPD784936 | μPD784937 | μPD78F4937 | | | | | |
|---|-------------|-------------|-------------|--------------|--|--|--|--|--|
| Item | | | | | | | | | |
| Internal ROM | 96K bytes | 128K bytes | 192K bytes | | | | | | |
| | Mask ROM | | | Flash memory | | | | | |
| Internal RAM | 5,120 bytes | 6,656 bytes | 8,192 bytes | | | | | | |
| Regulator | Provided | | | None | | | | | |
| Internal memory Note switching register | None | None | | | | | | | |
| IC pin | Provided | Provided | | | | | | | |
| VPP pin | None | | | Provided | | | | | |

Note The internal flash memory capacity and internal RAM capacity can be changed by setting the internal memory switching register (IMS).

2. PIN CONFIGURATION (TOP VIEW)

 100-pin plastic LQFP (fine pitch) (14 × 14 mm) μPD78F4937GC-8EU



Cautions 1. In normal operation, connect the VPP pin directly to the Vss pin.

- 2. Connect the AVDD pin directly to the VDD pin.
- 3. Connect the AVss pin directly to the Vss pin.

• **100-pin plastic QFP (14 × 20 mm)** μPD78F4937GF-3BA

| | O P35/T01 | O P34/T00 | | O P32/SCK0 | O P31/TxD/SO1 | O P30/RxD/SI1 | | -O P26/INTP5 | O P25/INTP4/ASCK/SCK1 | | -O P23/INTP2/CI | | | | | - O RX | | O AVREF1 | O AVDD | O P77/ANI7 | |
|----------------------------------|-----------|------------|---------|------------|---------------|---------------|---------|--------------|-----------------------|-------|-----------------|-----------|-------------|--------|----------|-----------|-----------|-----------|------------|------------------|--|
| | 10 | 0 99 | 98 | 97 | 96 | 95 | 94 | 93 | 92 | 91 | 90 | 89 | 88 | 87 | 86 | 85 | 84 | 83 | 82 | 81 | |
| P36/T02 O++ | 1 | _ | _ | | | | | | | | | | | | | | | | | 80 | ──O P76/ANI6 |
| P37/T03 O - + | 2 | (|) | | | | | | | | | | | | | | | | | 79 | ──O P75/ANI5 |
| P100 O - + | 3 | | - | | | | | | | | | | | | | | | | | 78 | → O P74/ANI4 |
| | 4 | | | | | | | | | | | | | | | | | | | 77 | O P73/ANI3 |
| | 5 | | | | | | | | | | | | | | | | | | | 76 | - O P72/ANI2 |
| P103 O | | | | | | | | | | | | | | | | | | | | 75 | - O P71/ANI1 |
| | | | | | | | | | | | | | | | | | | | | 74 | - O P70/ANI0 |
| - | 8 | | | | | | | | | | | | | | | | | | | 73 | |
| - | 9 10 | | | | | | | | | | | | | | | | | | | 72 71 | ─ - O PWM1 ─ - O PWM0 |
| P107/SO3 O RESET O | 10 | | | | | | | | | | | | | | | | | | | 70 | |
| | 12 | | | | | | | | | | | | | | | | | | | 69 | O P16 |
| XT2 O XT1 O | 12 | | | | | | | | | | | | | | | | | | | 68 | O P15 |
| Vss O | 14 | | | | | | | | | | | | | | | | | | | 67 | |
| X2 O | 15 | | | | | | | | | | | | | | | | | | | 66 | O P13/RxD2/SI2 |
| X1 O→ | 16 | | | | | | | | | | | | | | | | | | | 65 | O P12/ASCK2/SCK2 |
| REGOFF O | 17 | | | | | | | | | | | | | | | | | | | 64 | O P11 |
| REGC O | 18 | | | | | | | | | | | | | | | | | | | 63 | O P10 |
| | 19 | | | | | | | | | | | | | | | | | | | 62 | |
| P00 O ► | 20 | | | | | | | | | | | | | | | | | | | 61 | |
| P01 O | 21 | | | | | | | | | | | | | | | | | | | 60 | O P91 |
| P02 O | 22 | | | | | | | | | | | | | | | | | | | 59 | →O P92 |
| P03 O | 23 | | | | | | | | | | | | | | | | | | | 58 | O P93 |
| P04 O | 24 | | | | | | | | | | | | | | | | | | | 57 | O P94 |
| P05 O | | | | | | | | | | | | | | | | | | | | 56 | • O P95 |
| P06 O | | | | | | | | | | | | | | | | | | | | 55 | O P96 |
| P07 O | 27 | | | | | | | | | | | | | | | | | | | 54 | O P97 |
| P67/REFRQ/HLDAK O - ► | | | | | | | | | | | | | | | | | | | | 53 | O P40/AD0 |
| | 29 | | | | | | | | | | | | | | | | | | | 52 | → → O P41/AD1 |
| P65/WR O | | 1 32 | 22 | 34 | 35 | 36 | 37 | 38 | 30 | 40 | <i>4</i> 1 | 42 | 43 | 11 | 45 | 46 | 47 | 48 | <u>1</u> 0 | 51 50 | →O P42/AD2 |
| | 4 | . 52 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | | 12 | 1 | 1 | | 1 | 1 | 1 | 1 | 1 | I |
| | 6 | o 6 | 9 | 9 | 6 | 9 | 9 | 9 | 9 | þ | þ | 6 | 9 | 9 | 9 | 9 | 9 | 6 | 9 | 6 | |
| | RD | 119 | ٦18 | 317 | ٦16 | 315 | 314 | 413 | 312 | Vss O | | 411 | 3 10 | /A9 | /A8 | VD7 | ND6 | ND5 | D4 | D3 | |
| | P64/RD | P63/A19 | P62/A18 | P61/A17 | P60/A16 | P57/A15 | P56/A14 | P55/A13 O | P54/A12 C | | - | P53/A11 C | P52/A10 C | P51/A9 | P50/A8 C | P47/AD7 C | P46/AD6 O | P45/AD5 O | P44/AD4 C | P43/AD3 O | |
| | Δ. | . <u>c</u> | ď | đ | ď | đ | đ | đ | đ | | | <u>ă</u> | đ, | - | | 4 | д | д | 4 | д | |

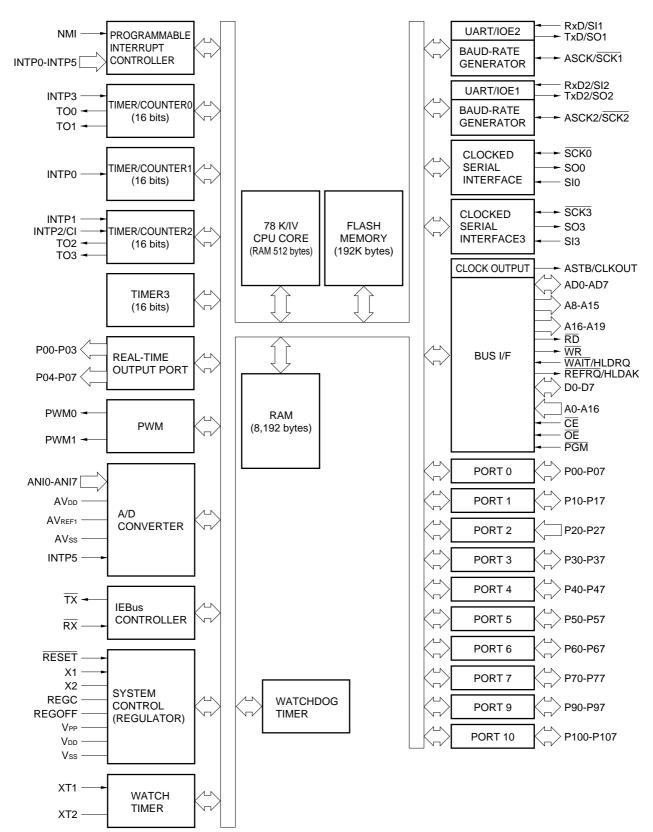
Cautions 1. In normal operation, connect the VPP pin directly to the Vss pin.

- 2. Connect the AVDD pin directly to the VDD pin.
- 3. Connect the AVss pin directly to the Vss pin.

NEC

| A8-A19 | : Address Bus | PWM0, PWM1 | : Pulse Width Modulation Output |
|-------------|-------------------------------|------------|---------------------------------|
| AD0-AD7 | : Address/Data Bus | RD | : Read Strobe |
| ANI0-ANI7 | : Analog Input | REFRQ | : Refresh Request |
| ASCK, ASCK | 2 : Asynchronous Serial Clock | REGC | : Regulator Capacitance |
| ASTB | : Address Strobe | REGOFF | : Regulator Off |
| AVdd | : Analog Power Supply | RESET | : Reset |
| AVREF1 | : Reference Voltage | RX | : IEBus Receive Data |
| AVss | : Analog Ground | RxD, RxD2 | : Receive Data |
| CI | : Clock Input | SCK0-SCK3 | : Serial Clock |
| CLKOUT | : Clock Output | SI0-SI3 | : Serial Input |
| HLDAK | : Hold Acknowledge | SO0-SO3 | : Serial Output |
| HLDRQ | : Hold Request | TO0-TO3 | : Timer Output |
| INTP0-INTP5 | : Interrupt from Peripherals | TX | : IEBus Transmit Data |
| NMI | : Non-maskable Interrupt | TxD, TxD2 | : Transmit Data |
| P00-P07 | : Port 0 | Vdd | : Power Supply |
| P10-P17 | : Port 1 | Vpp | : Programming Power Supply |
| P20-P27 | : Port 2 | Vss | : Ground |
| P30-P37 | : Port 3 | WAIT | : Wait |
| P40-P47 | : Port 4 | WR | : Write Strobe |
| P50-P57 | : Port 5 | X1, X2 | : Crystal (Main System Clock) |
| P60-P67 | : Port 6 | XT1, XT2 | : Crystal (Watch) |
| P70-P77 | : Port 7 | | |
| P90-P97 | : Port 9 | | |
| P100-P107 | : Port 10 | | |

3. BLOCK DIAGRAM



4. LIST OF PIN FUNCTIONS

4.1 Port Pins (1/2)

| Pin | I/O | Dual-function | Function | | | | | |
|---------|-------|-----------------|---|--|--|--|--|--|
| P00-P07 | I/O | _ | Port 0 (P0): 8-bit I/O port. Functions as a real-time output port (4 bits × 2). Inputs and outputs can be specified bit by bit. The use of pull-up resistors can be simultaneously specified by software for all pins in input mode. Can drive a transistor. | | | | | |
| P10 | I/O | _ | Port 1 (P1): | | | | | |
| P11 | | _ | 8-bit I/O port. Inputs and outputs can be specified bit by bit. | | | | | |
| P12 | | ASCK2/SCK2 | The use of pull-up resistors can be simultaneously specified by software | | | | | |
| P13 | | RxD2/SI2 | for all pins in input mode. | | | | | |
| P14 | | TxD2/SO2 | Can drive LED. | | | | | |
| P15-P17 | | _ | | | | | | |
| P20 | Input | NMI | Port 2 (P2): | | | | | |
| P21 | | INTP0 | 8-bit input-only port. P20 does not function as a general-purpose port (nonmaskable interrupt). | | | | | |
| P22 | | INTP1 | However, the input level can be checked by an interrupt service routine. | | | | | |
| P23 | | INTP2/CI | • The use of pull-up resistors can be specified by software for pins P22 to | | | | | |
| P24 | | INTP3 | P27 (in units of 6 bits). The P25/INTP4/ASCK/SCK1 pin functions as the SCK1 I/O pin by CSIM1 | | | | | |
| P25 | | INTP4/ASCK/SCK1 | | | | | | |
| P26 | | INTP5 | | | | | | |
| P27 | | SI0 | | | | | | |
| P30 | I/O | RxD/SI1 | Port 3 (P3): | | | | | |
| P31 | | TxD/SO1 | 8-bit I/O port. Jonute and outputs can be appearied bit by bit | | | | | |
| P32 | | SCK0 | Inputs and outputs can be specified bit by bit. The use of pull-up resistors can be simultaneously specified by software | | | | | |
| P33 | | SO0 | for all pins in input mode. | | | | | |
| P34-P37 | | TO0-TO3 | P32 and P33 can be set as the N-ch open-drain pin. | | | | | |
| P40-P47 | I/O | AD0-AD7 | Port 4 (P4): 8-bit I/O port. Inputs and outputs can be specified bit by bit. The use of pull-up resistors can be simultaneously specified by software for all pins in input mode. Can drive LED. | | | | | |

4.1 Port Pins (2/2)

| Pin | I/O | Dual-function | Function |
|-----------|-----|---------------|--|
| P50-P57 | I/O | A8-A15 | Port 5 (P5): 8-bit I/O port. Inputs and outputs can be specified bit by bit. The use of pull-up resistors can be simultaneously specified by software for all pins in input mode. Can drive LED. |
| P60-P63 | I/O | A16-A19 | Port 6 (P6): |
| P64 | | RD | 8-bit I/O port. Inputs and outputs can be specified bit by bit. |
| P65 | | WR | The use of pull-up resistors can be simultaneously specified by software |
| P66 | | WAIT/HLDRQ | for all pins in input mode. |
| P67 | | REFRQ/HLDAK | |
| P70-P77 | I/O | ANIO-ANI7 | Port 7 (P7):8-bit I/O port.Inputs and outputs can be specified bit by bit. |
| P90-P97 | I/O | _ | Port 9 (P9): 8-bit I/O port. Inputs and outputs can be specified bit by bit. The use of pull-up resistors can be simultaneously specified by software for all pins in input mode. |
| P100-P104 | I/O | - | Port 10 (P10): |
| P105 | | SCK3 | 8-bit I/O port. Insute and outputs can be appointed bit by bit |
| P106 | | SI3 | Inputs and outputs can be specified bit by bit. The use of pull-up resistors can be simultaneously specified by software |
| P107 | | SO3 | for all pins in input mode.P105 and P107 can be set as the N-ch open-drain pin. |

4.2 Non-Port Pins (1/2)

| Pin | I/O | Dual-function | | Function | | | | |
|---------|--------|----------------|---|---|--|--|--|--|
| TO0-TO3 | Output | P34-P37 | Timer output | | | | | |
| CI | Input | P23/INTP2 | Input of a count clock for timer/counter 2 | | | | | |
| RxD | Input | P30/SI1 | Serial data input (UART0) | | | | | |
| RxD2 | | P13/SI2 | Serial data input (UART2) | | | | | |
| TxD | Output | P31/SO1 | Serial data output (UART0 |)) | | | | |
| TxD2 | | P14/SO2 | Serial data output (UART2 | 2) | | | | |
| ASCK | Input | P25/INTP4/SCK1 | Baud rate clock input (UAF | RT0) | | | | |
| ASCK2 | | P12/SCK2 | Baud rate clock input (UAF | RT2) | | | | |
| SI0 | Input | P27 | Serial data input (3-wire se | erial I/O0) | | | | |
| SI1 | | P30/RxD | Serial data input (3-wire se | erial I/O1) | | | | |
| SI2 | | P13/RxD2 | Serial data input (3-wire se | erial I/O2) | | | | |
| SI3 | | P106 | Serial data input (3-wire se | erial I/O3) | | | | |
| SO0 | Output | P33 | Serial data output (3-wire | serial I/O0) | | | | |
| SO1 | | P31/TxD | Serial data output (3-wire s | serial I/O1) | | | | |
| SO2 | | P14/TxD2 | Serial data output (3-wire | serial I/O2) | | | | |
| SO3 | | P107 | Serial data output (3-wire s | serial I/O3) | | | | |
| SCK0 | I/O | P32 | Serial clock I/O (3-wire ser | rial I/O0) | | | | |
| SCK1 | | P25/INTP4/ASCK | Serial clock I/O (3-wire ser | rial I/O1) | | | | |
| SCK2 | | P12/ASCK | Serial clock I/O (3-wire ser | rial I/O2) | | | | |
| SCK3 | | P105 | Serial clock I/O (3-wire ser | rial I/O3) | | | | |
| NMI | Input | P20 | External interrupt request | _ | | | | |
| INTP0 | | P21 | | Input of a count clock for timer/counter 1 Capture/trigger signal for CR11 or CR12 | | | | |
| INTP1 | | P22 | - | Input of a count clock for timer/counter 2 Capture/trigger signal for CR22 | | | | |
| INTP2 | | P23/CI | | Input of a count clock for timer/counter 2 Capture/trigger signal for CR21 | | | | |
| INTP3 | | P24 | - | Input of a count clock for timer/counter 0 Capture/trigger signal for CR02 | | | | |
| INTP4 | _ | P25/ASCK/SCK1 | - | _ | | | | |
| INTP5 | _ | P26 | - | Input of a conversion start trigger for A/D converter | | | | |
| AD0-AD7 | I/O | P40-P47 | Time multiplexing address | /data bus (for connecting external memory) | | | | |
| A8-A15 | Output | P50-P57 | | or connecting external memory) | | | | |
| A16-A19 | Output | P60-P63 | | address expansion (for connecting external memory) | | | | |
| RD | Output | P64 | | ading the contents of external memory | | | | |
| WR | Output | P65 | Strobe signal output for wr | | | | | |
| WAIT | Input | P66/HLDRQ | Wait signal insertion | - * | | | | |
| REFRQ | Output | P67/HLDAK | | ternal pseudo static memory | | | | |
| HLDRQ | Input | P66/WAIT | Input of bus hold request | · · · | | | | |
| HLDAK | Output | P67/REFRQ | Output of bus hold response | se | | | | |
| ASTB | Output | CLKOUT | Latch timing output of time multiplexing address (A0-A7) (for connecting external memory) | | | | | |

4.2 Non-Port Pins (2/2)

| Pin | I/O | Dual-function | Function |
|--------------------|--------|---------------|--|
| CLKOUT | Output | ASTB | Clock output |
| PWM0 | Output | - | PWM output 0 |
| PWM1 | Output | - | PWM output 1 |
| RX | Input | - | Data input (IEBus) |
| TX | Output | - | Data output (IEBus) |
| REGC | - | - | Capacitor connection for stabilizing the regulator output |
| REGOFF | - | - | Signal for specifying regulator operation |
| RESET | Input | - | Chip reset |
| X1 | Input | - | Crystal input for system clock oscillation (A clock pulse can also be input to the |
| X2 | - | | X1 pin.) |
| XT1 | Input | - | Real-time clock connection pin |
| XT2 | - | - | |
| ANI0-ANI7 | Input | P70-P77 | Analog voltage inputs for the A/D converter |
| AV _{REF1} | - | - | Application of A/D converter reference voltage |
| AVdd | | | Positive power supply for the A/D converter |
| AVss | | | Ground for the A/D converter |
| Vdd | | | Positive power supply |
| Vss | | | Ground |
| Vpp | Input | | This pin is used to set the flash memory programming mode and applies a high voltage when a program is written or verified. In normal operation mode, connect this pin directly to the $V_{\rm SS}$ pin. |

4.3 I/O Circuits for Pins and Handling of Unused Pins

Table 4-1 describes the types of I/O circuits for pins and the handling of unused pins. Figure 4-1 shows the configuration of these various types of I/O circuits.

Table 4-1. Types of I/O Circuits for Pins and Handling of Unused Pins (1/2)

| P12/ASCK2/SCK2 8-A P13/RxD2/SI2 5-A P14/TxD2/SO2 5-A P15-P17 P20/NMI P20/NMI 2 P21/INTP0 2-A P22/INTP1 2-A | Pin | I/O circuit type | I/O | Recommended connection method for unused pins |
|--|---------------------|------------------|--------|---|
| In. P11 In. P12 P13/Rx02/S0/2 5-A P14/Tx02/S0/2 5-A P14/Tx02/S0/2 5-A P15/P17 Connect these pins to the Voo or Vss pin. P22/INTP0 2-A P23/INTP2/CI P-A P24/INTP3 2-A P25/INTP4/ASCK/SCK1 8-A P26/INTP5 2-A P26/INTP5 2-A P30/RD/S11 5-A P31/Tx0/S01 10-A P33/S00 10-A P34/T00-P3/T03 5-A P4/IO-P4/AD7 5-A P6/WRT 20 P6/WRT 20 P00-P104 | P00-P07 | 5-A | I/O | Input state: Connect these pins to the VDD pin. |
| P13RxD2/S12 5-A P14/TxD2/S02 5-A P15-P17 P10 P20/NMI 2 P21/INTP0 2-A P21/INTP1 2-A P23/INTP2/C1 P10 P24/INTP3 P10 P25/INTP4/ASCK/SCK1 8-A IV0 Input state: Connect these pins to the Voo pin. Output state: Connect these pins to the Voo pin. P26/INTP5 2-A P27/INTP 5-A P30/RD01 10-A P33/S00 10-A P30/RD0-P37/R03 5-A P4/RD 5-A P60/WR1/HLDRQ 5-A P60/R01/HLDRA Input state: P60/R01/HLDRA Voo P70/ANIC-P77/ANI7 20 P00-P104 Input state: P100-P104 10-A P100-P104 5-A P100-P104 10-A | P10, P11 | | | Output state: Leave these pins open. |
| P14/TxD2/SO2 Imput Connect these pins to the Voo or Vss pin. P20/NMI 2 Input Connect these pins to the Voo or Vss pin. P22/INTP1 2-A Connect these pins to the Voo pin. P23/INTP2/CI P24/INTP3 Connect these pins to the Voo pin. P24/INTP3 P26/INTP4/ASCK/SCK1 8-A I/O Input state: Connect these pins to the Voo pin. P26/INTP5 2-A Input Connect these pins to the Voo pin. Connect these pins to the Voo pin. P26/INTP5 2-A Input Connect these pins to the Voo pin. P27/ISI0 2-A Input state: Connect these pins to the Voo pin. P30/RxD/S11 5-A I/O Input state: Connect these pins to the Voo pin. P33/S00 P34/TOO-P37/T03 5-A I/O P40/ADO-P47/AD7 P30/AND-P47/AD7 P50/AB-P57/A15 Formation of the Parameter parameter pins to the Voo or Vss pin. P36/WR P66/WAT/HLDR0 P66/WAT/HLDR0 P90-P97 5-A Input state: Connect these pins to the Voo or Vss pin. P100-P104 P10-P104 P10-P10 | P12/ASCK2/SCK2 | 8-A | | |
| P15-P17 Imput P20INMI 2 Imput P21/INTP0 2.A Connect these pins to the Voo or Vss pin. P22/INTP1 2.A Connect these pins to the Voo pin. P23/INTP2/CI P24/INTP3 Connect these pins to the Voo pin. P25/INTP4/ASCK/SCK1 8-A I/O Input state: Connect this pin to the Voo pin. P26/INTP5 2-A Input Connect these pins to the Voo pin. P27/ISI0 2-A Input Connect these pins to the Voo pin. P26/INTP5 2-A Input Connect these pins to the Voo pin. P26/INTP5 2-A Input Connect these pins to the Voo pin. P27/ISI0 5-A I/O Input state: Connect these pins to the Voo pin. P31/TxD/S01 5-A I/O Input state: Connect these pins to the Voo pin. P33/S00 10-A 5-A I/O P34/T00-P37/T03 5-A Input state: Connect these pins to the Voo or Vss pin. P60/WR P60/WR P60/WR P60/WR P66/WRTP1 20 Input state: Connect these pins to the Voo or Vss pin. P100-P104 P100-P104 P100-P104 P100-P104 10-A P10/P104 P100/S03 10-A P10 | P13/RxD2/SI2 | 5-A | | |
| P20/INII P21/INTP02 CInput CConnect these pins to the Voo or Vss pin.P22/INTP12-AConnect these pins to the Voo pin.P23/INTP2/CIP24/INTP3Connect these pins to the Voo pin.P24/INTP3P25/INTP4/ASCK/SCKI8-AVOInput state: Connect these pins to the Voo pin.P26/INTP52-AInputConnect these pins to the Voo pin.P27/IOP30/RxD/S115-AInputP30/RxD/S115-AVAVAP31/TxD/S015-AVAP30/ADO-P37/T035-AVAP60/WAT/HLDRQ5-AVAP60/WAT/HLDRQ5-AVAP60/WAT/HLDRQ5-AVAP60/WAT/HLDRQ5-AVAP100-P1045-AVAP100-P10410-AP105/SGX310-AP105/SGX310-AP105/SGX310-AP105/SGX310-AP105/SGX310-AP105/SGX310-A | P14/TxD2/SO2 | | | |
| P21/INTP0 Image: Constant of the section | P15-P17 | | | |
| P22/INTP1 2-A Connect these pins to the Vop pin. P23/INTP2/CI P24/INTP3 Connect these pins to the Vop pin. P25/INTP4/ASCK/SCK1 8-A I/O Input state: Connect this pin to the Vop pin. P26/INTP5 2-A Input Connect these pins to the Vop pin. P26/INTP5 2-A Input Connect these pins to the Vop pin. P26/INTP5 2-A Input Connect these pins to the Vop pin. P26/INTP5 2-A Input Connect these pins to the Vop pin. P26/INTP5 2-A Input state: Connect these pins to the Vop pin. P27/SI0 5-A I/O Input state: Connect these pins to the Vop pin. P31/TxD/SO1 5-A I/O Input state: Connect these pins open. P33/SO0 10-A P6//AD P6//AD P60/A16-P63/A19 F6//AD P6//AD P6//REFRQ/HLDAK I/O Input state: Connect these pins to the Vop or Ves pin. P100-P104 F0 V/O Input state: Connect these pins to the Vop or Ves pin. P106/SI3 8-A Input state: Connect these pins open. <td< td=""><td>P20/NMI</td><td>2</td><td>Input</td><td>Connect these pins to the VDD or VSS pin.</td></td<> | P20/NMI | 2 | Input | Connect these pins to the VDD or VSS pin. |
| P23/INTP2/CI P24/INTP3 P24/INTP3 8-A I/O Input state: Connect this pin to the Voo pin. P26/INTP4/ASCK/SCK1 8-A I/O Input state: Leave this pin open. P26/INTP5 2-A Input Connect these pins to the Voo pin. P27/SI0 | P21/INTP0 | | | |
| P24/INTP3 Image: Constant of the second | P22/INTP1 | 2-A | | Connect these pins to the VDD pin. |
| P25/INTP4/ASCK/SCK1 8-A I/O Input state: Connect this pin to the Voo pin. P26/INTP5 2-A Input Connect these pins to the Voo pin. P27/SI0 | P23/INTP2/CI | | | |
| P26/INTP5 2-A Input Connect these pins to the Voo pin. P27/S10 | P24/INTP3 | | | |
| P27/S10Image: constant of the section of | P25/INTP4/ASCK/SCK1 | 8-A | I/O | |
| P30/RxD/SI1 5-A I/O P31/TxD/SO1 5-A I/O P32/SCK0 10-A P33/SO0 10-A P34/T00-P37/T03 5-A P40/AD0-P47/AD7 5-A P60/A16-P63/A19 5-A P66/WAIT/HLDRQ 66/WAIT/HLDRQ P66/WAIT/HLDRQ 10-A P70/ANI0-P77/ANI7 20 P100-P104 10-A P105/SCK3 10-A P106/SI3 8-A P107/SO3 10-A | P26/INTP5 | 2-A | Input | Connect these pins to the VDD pin. |
| P31/TxD/SQ1 Output state: Leave these pins open. P32/SCK0 10-A P33/S00 10-A P33/S00 5-A P40/AD0-P47/AD7 5-A P50/A8-P57/A15 5-A P60/A16-P63/A19 P64/RD P65/WR P66/WAIT/HLDRQ P66/WAIT/HLDRQ P67/REFRQ/HLDAK P70/ANI0-P77/ANI7 20 P100-P104 10-A P106/SI3 8-A P107/SQ3 10-A | P27/SI0 | | | |
| P3/17kD/SO1 Io-A P32/SCK0 10-A P33/S00 5-A P40/AD0-P37/T03 5-A P40/AD0-P47/AD7 5-A P50/A8-P57/A15 P60/A16-P63/A19 P60/A16-P63/A19 P66/WR P66/WAIT/HLDRQ P66/WAIT/HLDRQ P67/REFRQ/HLDAK P70/ANI0-P77/ANI7 20 I/O P100-P104 P105/SCK3 P106/SI3 8-A P107/SO3 10-A | P30/RxD/SI1 | 5-A | I/O | Input state: Connect these pins to the VDD pin. |
| P33/S00 | P31/TxD/SO1 | | | Output state: Leave these pins open. |
| P34/TO0-P37/TO3 5-A P40/AD0-P47/AD7 5-A P50/A8-P57/A15 | P32/SCK0 | 10-A | | |
| P40/AD0-P47/AD7 P50/A8-P57/A15 P60/A16-P63/A19 P64/RD P64/RD P64/RD P65/WR P66/WAIT/HLDRQ P67/REFRQ/HLDAK P70/ANI0-P77/ANI7 20 I/O P90-P97 5-A P100-P104 P105/SCK3 10-A | P33/SO0 | | | |
| P50/A8-P57/A15 P60/A16-P63/A19 P60/A16-P63/A19 P64/RD P64/RD P65/WR P66/WAIT/HLDRQ P66/WAIT/HLDAK P70/ANI0-P77/ANI7 20 P70/ANI0-P77/ANI7 20 P100-P104 I/O P105/SCK3 10-A P106/SI3 8-A P107/SO3 10-A | P34/T00-P37/T03 | 5-A | | |
| P60/A16-P63/A19 P65/WR P65/WR P65/WR P66/WAIT/HLDRQ P67/REFRQ/HLDAK P70/ANI0-P77/ANI7 20 P70/ANI0-P77/ANI7 20 P90-P97 5-A P100-P104 P105/SCK3 P106/SI3 8-A P107/SO3 10-A | P40/AD0-P47/AD7 | | | |
| P64/RD P65/WR P65/WAIT/HLDRQ P66/WAIT/HLDRQ P67/REFRQ/HLDAK I/O P70/ANI0-P77/ANI7 20 P90-P97 5-A P100-P104 Output state: Leave these pins open. P105/SCK3 10-A P106/SI3 8-A P107/SO3 10-A | P50/A8-P57/A15 | | | |
| P65/WR P66/WAIT/HLDRQ P66/WAIT/HLDRQ P66/WAIT/HLDRQ P67/REFRQ/HLDAK P70/ANI0-P77/ANI7 20 I/O P90-P97 5-A P100-P104 5-A P105/SCK3 10-A P106/SI3 8-A P107/SO3 10-A | P60/A16-P63/A19 | | | |
| P66/WAIT/HLDRQP67/REFRQ/HLDAKP70/ANI0-P77/ANI720P70/ANI0-P77/ANI720P90-P975-AP100-P104P105/SCK310-AP106/SI38-AP107/SO310-A | P64/RD | | | |
| P67/REFRQ/HLDAK P0/P0/P1/2 20 I/O P90-P97 5-A 10-A P100-P104 10-A P106/SI3 8-A P107/SO3 10-A | P65/WR | | | |
| P70/ANI0-P77/ANI7 20 I/O P90-P97 5-A Output state: Connect these pins to the Vob or Vss pin. P100-P104 | P66/WAIT/HLDRQ | | | |
| P90-P97 5-A P100-P104 Output state: Leave these pins open. P105/SCK3 10-A P106/SI3 8-A P107/SO3 10-A | P67/REFRQ/HLDAK | | | |
| P100-P104 5-A P105/SCK3 10-A P106/SI3 8-A P107/SO3 10-A | P70/ANI0-P77/ANI7 | 20 | I/O | |
| P105/SCK3 10-A P106/SI3 8-A P107/SO3 10-A | P90-P97 | 5-A | | Output state: Leave these pins open. |
| P106/SI3 8-A P107/SO3 10-A | P100-P104 | | | |
| P107/SO3 10-A | P105/SCK3 | 10-A | | |
| | P106/SI3 | 8-A | | |
| ASTB/CLKOUT 4 Output Leave this pin open. | P107/SO3 | 10-A | | |
| | ASTB/CLKOUT | 4 | Output | Leave this pin open. |

| Pin | I/O circuit type | I/O | Recommended connection method for unused pins |
|--------------------|------------------|--------|---|
| RESET | 2 | Input | _ |
| XT2 | - | - | Leave this pin open. |
| XT1 | - | Input | Connect this pin to the Vss pin. |
| REGOFF | 1 | - | Connect these pins to the Voo pin. |
| REGC | - | - | |
| PWM0, PWM1 | 3 | Output | Leave this pin open. |
| RX | 2 | Input | Connect this pin to the V_{DD} or V_{SS} pin. |
| TX | 3 | Output | Leave this pin open. |
| AV _{REF1} | - | - | Connect these pins to the Vss pin. |
| AVss | | | |
| AVdd | | | Connect this pin to the V_{DD} pin. |
| Vpp | | Input | Connect this pin directly to the Vss pin. |

Table 4-1. Types of I/O Circuits for Pins and Handling of Unused Pins (2/2)

- Caution When the I/O mode of an I/O dual-function pin is unpredictable, connect the pin to VDD through a resistor of 10 to 100 kilohms (particularly when the voltage of the reset input pin becomes higher than that of the low level input at power-on or when I/O is switched by software).
- **Remark** Since type numbers are consistent in the 78K Series, those numbers are not always serial in each product. (Some circuits are not included.)

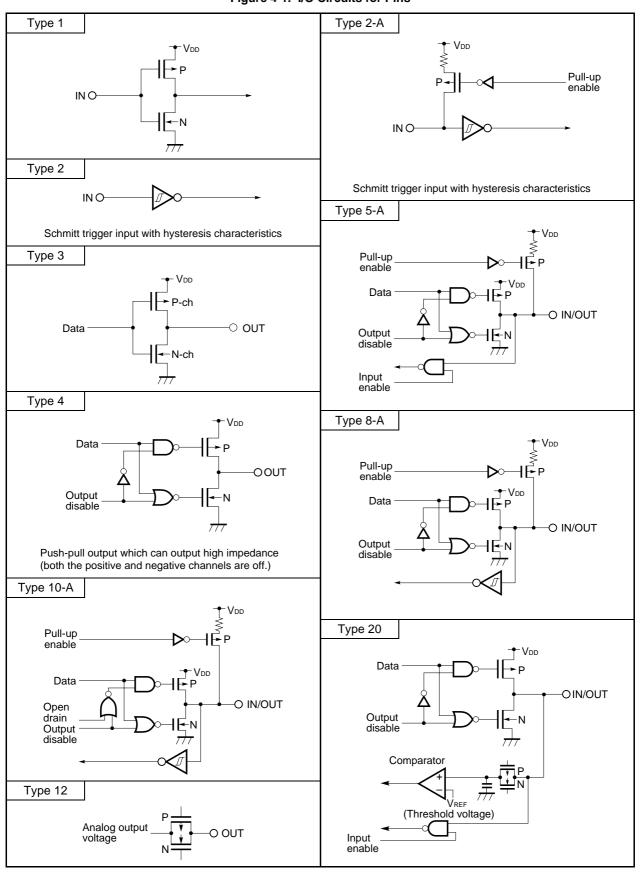


Figure 4-1. I/O Circuits for Pins

5. INTERNAL MEMORY SWITCHING (IMS) REGISTER

This register enables the software to avoid using part of the internal memory. The IMS register can be set to establish the same memory mapping as used in ROM products that have different internal memory (ROM and RAM) configurations.

The IMS register is set using 8-bit memory operation instructions.

A RESET input sets the IMS register to FFH.

Figure 5-1. Internal Memory Switching (IMS) Register

| Addre | ess: 0FFF | СН | When rese | et: FFH | W/R | | | |
|-------|-----------|----|-----------|---------|-----|---|------|------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IMS | 1 | 1 | ROM1 | ROM0 | 1 | 1 | RAM1 | RAM0 |

| ROM1 | ROM0 | Internal ROM capacity selection |
|------|------|---------------------------------|
| 0 | 0 | Not to be set |
| 0 | 1 | 96K bytes |
| 1 | 0 | 128K bytes |
| 1 | 1 | 192K bytes |

| RAM1 | RAM0 | Internal RAM capacity selection | |
|------|------|---------------------------------|--|
| 0 | 0 | Not to be set | |
| 0 | 1 | 5,120 bytes | |
| 1 | 0 | 6,656 bytes | |
| 1 | 1 | 8,192 bytes | |

Caution The IMS is not contained in a mask ROM product (µPD784935, µPD784936, or µPD784937).

The IMS setting to obtain the same memory map as masked ROM products are shown in Table 5-1.

Table 5-1. Internal Memory Switching Register (IMS) Setting Value

| Product | IMS setting value |
|-----------|-------------------|
| μPD784935 | DDH |
| μPD784936 | EEH |
| μPD784937 | FFH |

6. FLASH MEMORY PROGRAMMING

The flash memory can be written even while the device is mounted in the target system (on-board write). To write a program into the flash memory, connect the dedicated flash writer (Flashpro III) to both the host machine and target system.

Remark The Flashpro III is manufactured by Naito Densei Machida Mfg. Co., Ltd.

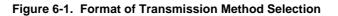
6.1 Selecting the Transmission Method

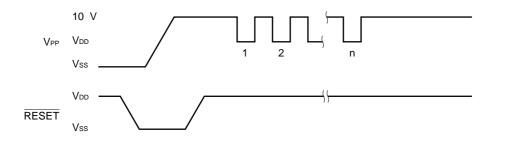
The Flashpro III writes into flash memory by means of serial transmission. The transmission method to be used for writing is selected from those listed in Table 6-1. To select a transmission method, use the format shown in Figure 6-1, according to the number of VPP pulses listed in Table 6-1.

| Table 6-1. | Transmission | Methods |
|------------|--------------|---------|
|------------|--------------|---------|

| Transmission method | Number of channels | Pins | Number of VPP pulses |
|---------------------|--------------------|-----------------------------------|----------------------|
| 3-wire serial I/O | 1 | SCK3/P105 SO3/P107 SI3/P106 | 0 |
| UART | 1 | TxD/SO1/P31 RxD/SI1/P30 | 8 |

Caution To select a transmission method, always use the corresponding number of VPP pulses listed in Table 6-1.





6.2 Flash Memory Programming Functions

Flash memory writing and other operations can be performed by transmitting/receiving commands and data according to the selected transmission method. Table 6-2 lists the main flash memory programming functions.

| Function | Description |
|-------------------|---|
| Batch erase | Erases the entire contents of memory. |
| Block erase | Erases the contents of specified memory block. |
| Batch blank check | Checks that the entire contents of memory have been erased. |
| Block blank check | Checks that the contents of specified block have been erased. |
| Data write | Write to the flash memory according to the specified write start address and number of bytes of data to be written. |
| Batch verify | Compares the entire contents of memory with the input data. |
| Block verify | Compares the contents of specified memory block with the input data. |

| Table 6-2. | Main Flash | Memory | Programming | Functions |
|------------|------------|----------|-------------|-----------|
| | manninaon | incomo y | riogrammig | |

6.3 Connecting the Flashpro III

The connection between the Flashpro III and μ PD78F4937 varies with the transmission method. Figures 6-2 and 6-3 show the connection for each transmission method.

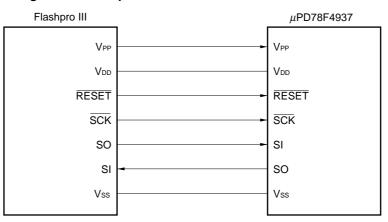
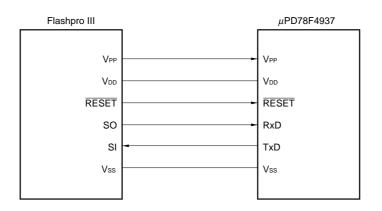


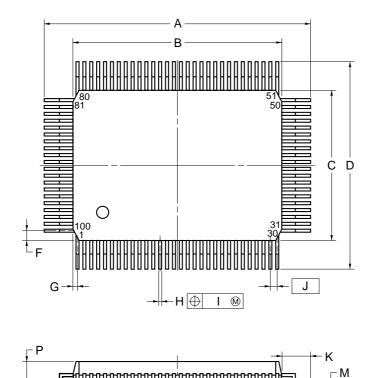
Figure 6-2. Flashpro III Connection in 3-Wire Serial I/O Mode

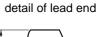


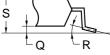


7. PACKAGE DRAWINGS

100PIN PLASTIC QFP (14x20)







NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

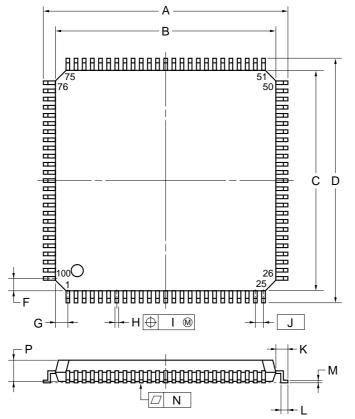
Ν

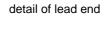
REMARK

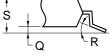
The shape and material of the ES product is the same as the mass produced product.

| ITEM | MILLIMETERS | S INCHES |
|------|------------------------|---------------------------|
| Α | 23.6±0.4 | 0.929±0.016 |
| В | 20.0±0.2 | $0.795^{+0.009}_{-0.008}$ |
| С | 14.0±0.2 | $0.551^{+0.009}_{-0.008}$ |
| D | 17.6±0.4 | 0.693±0.016 |
| F | 0.8 | 0.031 |
| G | 0.6 | 0.024 |
| н | 0.30±0.10 | $0.012^{+0.004}_{-0.005}$ |
| I | 0.15 | 0.006 |
| J | 0.65 (T.P.) | 0.026 (T.P.) |
| К | 1.8±0.2 | $0.071^{+0.008}_{-0.009}$ |
| L | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| М | $0.15^{+0.10}_{-0.05}$ | $0.006^{+0.004}_{-0.003}$ |
| N | 0.10 | 0.004 |
| Р | 2.7±0.1 | $0.106^{+0.005}_{-0.004}$ |
| Q | 0.1±0.1 | 0.004±0.004 |
| R | 5°±5° | 5°±5° |
| S | 3.0 MAX. | 0.119 MAX. |
| | | P100GF-65-3BA1-3 |

100 PIN PLASTIC LQFP (FINE PITCH) (14×14)







NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

REMARK

The shape and material of the ES product is the same as the mass produced product.

| ITEM | MILLIMETERS | INCHES |
|------|------------------------|-------------------------------|
| А | 16.00±0.20 | 0.630 ± 0.008 |
| В | 14.00±0.20 | 0.551 +0.009 -0.008 |
| С | 14.00±0.20 | $0.551^{+0.009}_{-0.008}$ |
| D | 16.00±0.20 | 0.630±0.008 |
| F | 1.00 | 0.039 |
| G | 1.00 | 0.039 |
| н | $0.22^{+0.05}_{-0.04}$ | 0.009±0.002 |
| I | 0.08 | 0.003 |
| J | 0.50 (T.P.) | 0.020 (T.P.) |
| к | 1.00±0.20 | $0.039^{+0.009}_{-0.008}$ |
| L | 0.50±0.20 | $0.020^{+0.008}_{-0.009}$ |
| М | $0.17^{+0.03}_{-0.07}$ | $0.007^{+0.001}_{-0.003}$ |
| N | 0.08 | 0.003 |
| Р | 1.40±0.05 | 0.055±0.002 |
| Q | 0.10±0.05 | 0.004±0.002 |
| R | 3°+7° -3° | 3° ^{+7°} -3° |
| S | 1.60 MAX. | 0.063 MAX. |
| | | S100GC-50-8EU |

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μ PD78F4937. See also (5).

(1) Language processing software

| RA78K4 | Assembler package used in common with 78K/IV Series |
|----------|--|
| CC78K4 | C compiler package used in common with 78K/IV Series |
| DF784937 | Device file for μ PD784937 Subseries |
| CC78K4-L | C compiler library source file used in common with 78K/IV Series |

(2) Flash memory write tools

| Flashpro III ^{Note} (PG-FPIII) | Flash writer used only for microcontrollers with internal flash memory |
|--|---|
| FA-100GF | Flash memory writing adapter for 100-pin plastic QFP (GF-3BA type). Wiring must be performed according to product being used. |
| FA-100GC | Flash memory writing adapter for 100-pin plastic LQFP (GC-8EU type). Wiring must be performed according to product being used. |
| Flashpro III controller | Program controlled by a personal computer and which is supported by Flashpro III. Runs under Windows TM 95, etc. |

(3) Debugging tools

• When using the in-circuit emulator IE-78K4-NS

| IE-78K4-NS | In-circuit emulator used in common with 78K/IV Series |
|------------------|---|
| IE-70000-MC-PS-B | Power supply unit for IE-78K4-NS |
| IE-70000-98-IF-C | Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine |
| IE-70000-CD-IF-C | PC card and interface cable when a PC-9800 series notebook is used as the host machine |
| IE-70000-PC-IF-C | Interface adapter when the IBM PC/AT TM compatible is used as the host machine |
| IE-784937-NS-EM1 | Emulation board for emulating μ PD784937 Subseries |
| NP-100GF | Emulation probe for 100-pin plastic QFP (GF-3BA type) |
| NP-100GC | Emulation probe for 100-pin plastic LQFP (GC-8EU type) |
| EV-9200-GF-100 | Socket for mounting on target system board made for 100-pin plastic QFP (GF- 3BA type) |
| TGC-100SDW | Conversion adapter for connecting the target system board made for 100-pin plastic LQFP (GC-8EU type) with NP-100GC |
| ID78K4-NS | Integrated debugger for IE-78K4-NS |
| SM78K4 | System simulator used in common with 78K/IV Series |
| DF789437 | Device file for μ PD784937 Subseries |

Note Under development

• When using the in-circuit emulator IE-784000-R

| IE-784000-R | In-circuit emulator used in common with 78K/IV Series |
|---|--|
| IE-70000-98-IF-B IE-70000-98-IF-C | Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine |
| IE-70000-98N-IF | Interface adapter and cable when a PC-9800 series notebook is used as the host machine |
| IE-70000-PC-IF-B IE-70000-PC-IF-C | Interface adapter when the IBM PC/AT compatible is used as the host machine |
| IE-78000-R-SV3 | Interface adapter and cable when the EWS is used as the host machine |
| IE-784937-NS-EM1 ^{Note} IE-784937-R-EM1 ^{Note} | Emulation board for emulating μ PD784937 Subseries |
| IE-78400-R-EM | Emulation board used in common with 78K/IV Series |
| IE-78K4-R-EX2 ^{Note} | Conversion board for emulation probes required to use the IE-784937-NS-EM1 on the IE-784000-R. The board is not needed when the IE-784937-R-EM1 is used. |
| EP-78064GF-R | Emulation probe for 100-pin plastic QFP (GF-3BA type) |
| EP-78064GC-R | Emulation probe for 100-pin plastic LQFP (GC-8EU type) |
| EV-9200GF-100 | Socket for mounting on target system board made for 100-pin plastic QFP (GF-3BA type) |
| TGC-100SDW | Conversion adapter for connecting the target system board made for 100-pin plastic LQFP (GC-8EU type) with NP-100GC |
| ID78K4 | Integrated debugger for IE-784000-R |
| SM78K4 | System simulator used in common with 78K/IV Series |
| DF784937 | Device file for μ PD784937 Subseries |

Note Under development

(4) Real-time OS

| RX78K/IV | Real-time OS for 78K/IV Series |
|----------|--------------------------------|
| MX78K4 | OS for the 78K/IV Series |

(5) Notes when using development tools

- The ID78K4-NS, ID78K4, and SM78K4 can be used in combination with the DF784937.
- The CC78K4 and RX78K/IV can be used in combination with the RA78K4 and DF784937.
- The Flashpro III, FA-100GF, FA-100GC, NP-100GF, and NP-100GC are manufactured by Naito Densei Machida Mfg. Co., Ltd. (044-822-3813). Consult the NEC sales representative for purchasing.
- The TGC-100SDW is a product from TOKYO ELETECH CORPORATION.
- Refer to: Daimaru Kogyo, Ltd.

Tokyo Electronic Components Division (03-3820-7112)

- Osaka Electronic Components Division (06-244-6672)
- The host machines and operating systems corresponding to each software are shown below.

| Host machine | PC | EWS |
|------------------|---|--|
| [OS] Software | PC-9800 series [Windows] IBM PC/AT compatibles [Japanese/English Windows] | HP9000 series 700 [™] [HP-UX [™]] SPARCstation [™] [SunOS [™] , Solaris [™]] NEWS [™] (RISC) [NEWS-OS [™]] |
| RA78K4 | O ^{Note} | 0 |
| CC78K4 | ONote | 0 |
| ID78K4-NS | 0 | _ |
| ID78K4 | 0 | 0 |
| SM78K4 | 0 | - |
| RX78K/IV | ONote | 0 |
| MX78K4 | O ^{Note} | 0 |

Note Software under MS-DOS

APPENDIX B RELATED DOCUMENTS

• Documents Related to Devices

| Document name | Document No. | |
|--|---------------|---------------|
| | Japanese | English |
| μ PD784935, 784936, 784937 Preliminary Product Information | U13572J | To be created |
| μ PD78F4937 Preliminary Product Information | U13573J | This manual |
| μ PD784937 Subseries User's Manual, Hardware | To be created | To be created |
| μ PD784937 Subseries Special Function Registers | To be created | _ |
| 78K/IV Series User's Manual, Instruction | U10905J | U10905E |
| 78K/IV Series Instruction Summary Sheet | U10594J | _ |
| 78K/IV Series Instruction Set | U10595J | _ |
| 78K/IV Series Application Note, Software Basic | U10095J | U10095E |

• Documents Related to Development Tools (User's Manual)

| Document name | | Document No. | |
|---|--|---------------|---------------|
| | | Japanese | English |
| RA78K Series Assembler Package | Operation | U11334J | U11334E |
| | Language | U11162J | U11162E |
| RA78K Series Structured Assembler Preprocessor | | U11743J | U11743E |
| CC78K Series C Compiler | Operation | U11571J | U11571E |
| | Language | U11572J | U11572E |
| IE-78K4-NS | | U13356J | To be created |
| IE-784000-R | | U12903J | EEU-1534 |
| IE-784937-R-EM1 | | To be created | To be created |
| IE-784937-NS-EM1 | | To be created | To be created |
| EP-78064 | | EEU-934 | EEU-1469 |
| SM78K4 System Simulator Windows Base | Reference | U10093J | U10093E |
| SM78K Series System Simulator | External Parts User Open Interface Specifications | U10092J | U10092E |
| ID78K4-NS Integrated Debugger | Reference | U12796J | U12796E |
| ID78K4 Integrated Debugger Windows Base | Reference | U10440J | U10440E |
| ID78K4 Integrated Debugger HP-UX, SunOS, NEWS-OS Base | Reference | U11960J | U11960E |

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

• Documents Related to Software to Be Incorporated into the Product (User's Manual)

| Document name | | Document No. | |
|-----------------------------|--------------|--------------|---------|
| | | Japanese | English |
| 78K/IV Series Real-Time OS | Basic | U10603J | U10603E |
| | Installation | U10604J | U10604E |
| | Debugger | U10364J | - |
| OS for 78K/IV Series MX78K4 | | U11779J | - |

• Other Documents

| Document name | Document No. | |
|--|--------------|---------|
| | Japanese | English |
| IC PACKAGE MANUAL | C10943X | |
| SMD Surface Mount Technology Manual | C10535J | C10535E |
| Quality Grades on NEC Semiconductor Device | C11531J | C11531E |
| NEC Semiconductor Device Reliability/Quality Control System | C10983J | C10983E |
| Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD) | C11892J | C11892E |
| Semiconductor Device Quality Control/Reliability Handbook | C12769J | _ |
| Guide for Products Related to Microcomputer: Other Companies | U11416J | _ |

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

[MEMO]

NOTES FOR CMOS DEVICES-

1 PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Preliminary Product Information

Regional Information

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- · Device availability
- Ordering information
- Product release schedule
- · Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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NEC Electronics (UK) Ltd. Milton Keynes, UK Tel: 01908-691-133 Fax: 01908-670-290

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NEC do Brasil S.A. Cumbica-Guarulhos-SP, Brasil Tel: 011-6465-6810 Fax: 011-6465-6829 Some related documents may be preliminary versions. Note that, however, what documents are preliminary is not indicated in this document.

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- Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
- Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.

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