

GENERAL DESCRIPTION

The XRK697H73 is a PLL based LVCMOS Clock Generator targeted for high performance and low skew clock distribution applications. The XRK697H73 can select between one of three reference inputs and provides 14 LVCMOS outputs -12 outputs (3 banks of 4) for clock distribution, 1 for feedback and 1 for synchronization.

The XRK697H73 is a highly flexible device. It has 3 selectable inputs, (one differential and two single-ended inputs) to support system clock redundancy. Up to three different clock frequencies can be generated and outputted on the three output banks. Switching the internal reference clock is controlled by the control input, CLK_SEL.

The XRK697H73 uses PLL technology to frequency lock its outputs to the input reference clock. The divider in the feedback path will determine the frequency of the VCO. Each of the separate output banks can individually divide down the VCO output frequency. This allows the XRK697H73 to generate a multitude of different bank frequency ratios and output-to-input frequency ratios.

The outputs of the XRK697H73 can individually be immobilized, in the low state, by use of the clock stop feature. All outputs except QC0 and QFB can be immobilized through a 2 pin serial interface. Global output disabling and reset can be achieved the control input MR/OE.

The XRK697H73 also has a QSYNC output which can be used for system synchronization purposes. It monitors Bank A and Bank C outputs and goes low one period of the

faster clock prior to coincident rising edges of Bank A and Bank C clocks. QSYNC then goes high again when the coincident rising edges of Bank A and Bank C occur. This feature is used primarily in applications where Bank A and Bank C are running at different frequencies, and is particularly useful when they are running at non-integer multiples of one another.

The XRK697H73 has an output frequency range of 8.33MHz to 240MHz and an input frequency range of 5MHz to 120MHz.

FEATURES

- Fully Integrated PLL
- Selectable Differential PECL or LVCMOS inputs for reference clock source
- 14 LVCMOS outputs
 - 3 banks with 4 outputs each. Frequencies can be individually controlled by bank
 - 1 dedicated feedback with frequency control
 - 1 Sync
- VCO Range 200MHz to 480MHz
- Output freq. range: 8.33MHz to 240MHz
- Max Output Skew of 250ps
- Cycle-to-cycle jitter: 150ps (typ)

APPLICATIONS

- System Clock generator
- Zero Delay Buffer

PRODUCT ORDERING INFORMATION

| PRODUCT NUMBER | PACKAGE TYPE | OPERATING TEMPERATURE RANGE |
|----------------|--------------|-----------------------------|
| XRK697H73CR | 52-LEAD LQFP | 0°C to +70°C |
| XRK697H73IR | 52-LEAD LQFP | -40°C to +85°C |

FIGURE 1. BLOCK DIAGRAM OF THE XRK697H73

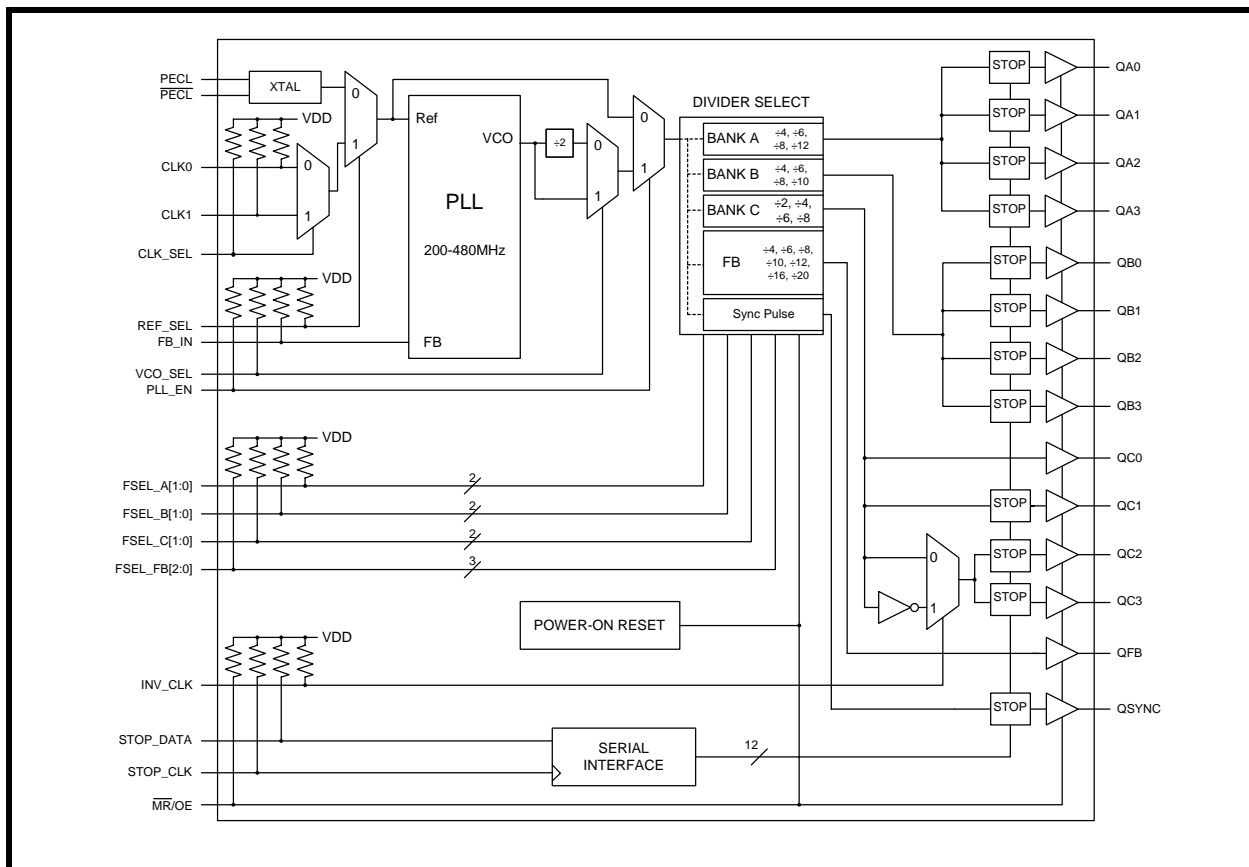
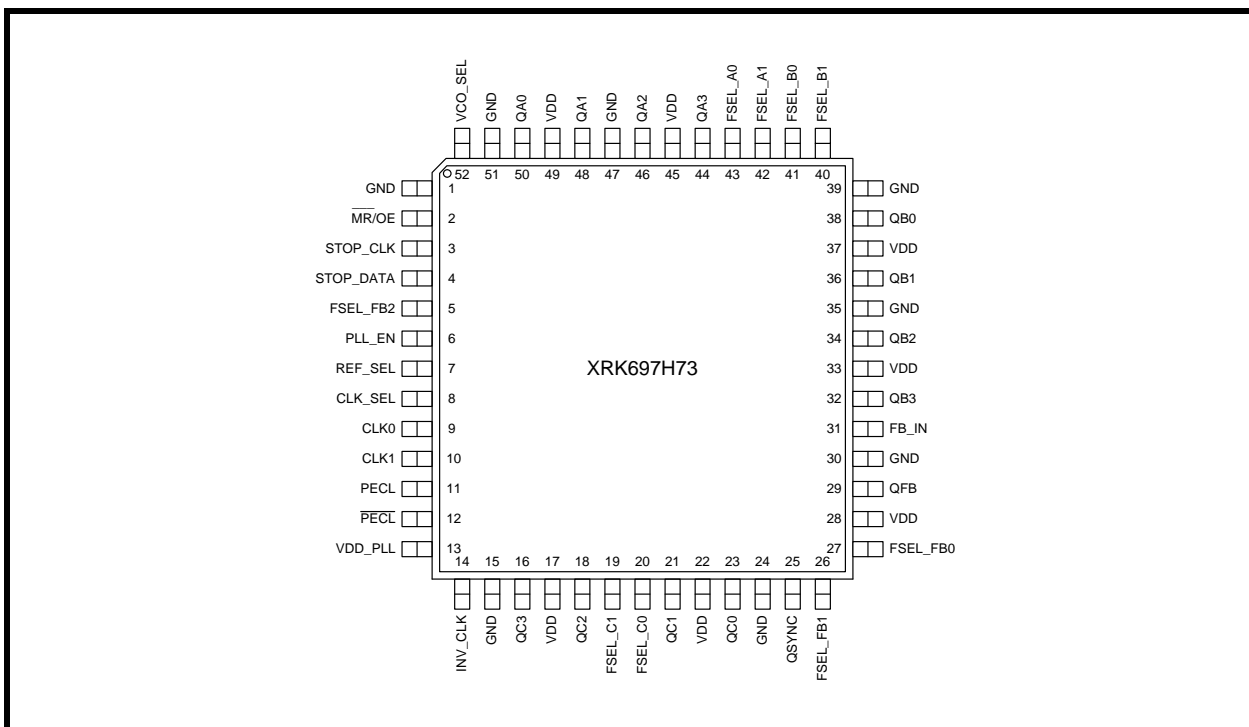


FIGURE 2. PIN OUT OF THE XRK697H73



PIN DESCRIPTIONS

| PIN # | NAME | TYPE | DESCRIPTION |
|-------------------------------|--------------|--------|--|
| 1, 15, 24, 30, 35, 39, 47, 51 | GND | POWER | Power supply ground |
| 2 | MR/OE | INPUT* | Master reset and output enable. High = output enabled, Low = device reset & outputs tri-stated |
| 3 | STOP_CLK | INPUT* | Clock input for serial control. |
| 4 | STOP_DATA | INPUT* | Data input for serial control |
| 5, 26, 27 | FSEL_FB[2:0] | INPUT* | Select inputs for control of feedback divide value. |
| 6 | PLL_EN | INPUT* | PLL bypass. High = PLL, Low = PLL bypass |
| 7 | REF_SEL | INPUT* | Xtal or CLK select. High = Xtal input selected, Low = CLK0 or CLK1 selected |
| 8 | CLK_SEL | INPUT* | CLK0 or CLK1 Select. High = CLK1 selected, Low = CLK0 selected |
| 9 | CLK0 | INPUT* | PLL Reference Clock Inputs |
| 10 | CLK1 | INPUT* | |
| 11 | PECL | INPUT | Differential LVPECL Clock Input |
| 12 | PECL | | |
| 13 | VDD_PLL | POWER | Analog supply for PLL |
| 14 | INV_CLK | INPUT* | Invert clock select for QC3 & QC2. High = invert, Low = normal operation |
| 17, 22, 28, 33, 37, 45, 49 | VDD | POWER | Power supply for outputs. |
| 19, 20 | FSEL_C[1:0] | INPUT* | Bank C divide select pins. |
| 25 | QSYNC | OUTPUT | Synchronization output for Bank A and Bank C. |
| 29 | QFB | OUTPUT | Feedback clock output |
| 31 | FB_IN | INPUT* | Feedback input |
| 32, 34, 36, 38 | QB[3:0] | OUTPUT | Clock outputs (Bank B) |
| 40, 41 | FSEL_B[1:0] | INPUT* | Bank B divide select pins. |
| 42, 43 | FSEL_A[1:0] | INPUT* | Bank A divide select pins. |
| 44, 46, 48, 50 | QA[3:0] | OUTPUT | Clock outputs (Bank A) |
| 52 | VCO_SEL | INPUT* | VCO select. High = VCO/1, Low = VCO/2. |

* 25KΩ pull-up resistor

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1.0 ELECTRICAL SPECIFICATIONS

TABLE 1: GENERAL SPECIFICATIONS

| SYMBOL | CHARACTERISTICS | CONDITION | MIN | TYP | MAX | UNIT |
|-------------|-----------------------------------|-----------|------|-----------------|-----|------|
| V_{TT} | Output Termination Voltage | | | $V_{DD} \div 2$ | | V |
| ESD_{MM} | ESD Protection (Machine model) | | 200 | | | V |
| ESD_{HBM} | ESD Protection (Human body model) | | 2000 | | | V |
| LU | Latch-up Immunity | | 200 | | | mA |
| C_{IN} | Input capacitance | per input | | 4 | | pf |

TABLE 2: ABSOLUTE MAXIMUM RATINGS

| SYMBOL | CHARACTERISTICS | CONDITION | MIN | TYP | MAX | UNIT |
|-----------|---------------------|-----------|------|-----|----------------|------|
| V_{DD} | Supply Voltage | | -0.3 | | 3.9 | V |
| V_{IN} | DC Input Voltage | | -0.3 | | $V_{DD} + 0.3$ | V |
| V_{OUT} | DC Output Voltage | | -0.3 | | $V_{DD} + 0.3$ | V |
| I_{IN} | DC Input Current | | | | +/-20 | mA |
| I_{OUT} | DC Output Current | | | | +/-50 | mA |
| T_S | Storage Temperature | | -65 | | 125 | °C |

TABLE 3: DC CHARACTERISTICS ($V_{DD} = 3.3V \pm 5\%$)

| SYMBOL | CHARACTERISTICS | CONDITION | MIN | TYP | MAX | UNIT |
|---------------|---|------------------------------|------|------|----------------|----------|
| V_{DD_PLL} | PLL Supply Voltage | | 3.0 | | V_{DD} | V |
| V_{IH} | Input High Voltage | | 2.0 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | | | 0.8 | V |
| V_{PP} | Peak to Peak Input Voltage PECL and \overline{PECL} | LVPECL | 250 | | | mV |
| V_{CMR} | Common Mode Range PECL and \overline{PECL} | LVPECL | 1.0 | | $V_{DD} - 0.6$ | V |
| V_{OH} | Output High Voltage | $IOH = -24mA$ | 2.4 | | | V |
| V_{OL} | Output Low Voltage | $IOL = 24mA$ $IOL = 12mA$ | | | 0.55 0.30 | V |
| Z_{OUT} | Output Impedance | | | 8-11 | | Ω |
| I_{PU} | Input Current | $V_{IN} = GND$ or V_{DD} | -100 | | 200 | μA |
| I_{DD_PLL} | PLL Supply Current | @ V_{DD_PLL} Pin | | 8 | 13.5 | mA |
| I_{DDQ} | Quiescent Supply Current | | | | 35 | mA |

TABLE 4: AC CHARACTERISTICS ($V_{DD} = 3.3V \pm 5\%$)

| SYMBOL | CHARACTERISTICS | CONDITION | MIN | TYP | MAX | UNIT |
|------------------|---|---|---|------------|---|--|
| f_{REF} | Input reference frequency ^a | <div>÷4 feedback</div> <div>÷6 feedback</div> <div>÷8 feedback</div> <div>÷10 feedback</div> <div>÷12 feedback</div> <div>÷16 feedback</div> <div>÷20 feedback</div> <div>÷24 feedback</div> <div>÷32 feedback</div> <div>÷40 feedback</div> <div>PLL bypass mode</div> | <div>50.0</div> <div>33.3</div> <div>25.0</div> <div>20.0</div> <div>16.6</div> <div>12.5</div> <div>10.0</div> <div>8.33</div> <div>6.25</div> <div>5.00</div> <div></div> | | <div>120</div> <div>80.0</div> <div>60.0</div> <div>48.0</div> <div>40.0</div> <div>30.0</div> <div>24.0</div> <div>20.0</div> <div>15.0</div> <div>12.0</div> <div>250</div> | <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> |
| f_{VCO} | VCO frequency range | | 200 | | 480 | MHz |
| f_{MAX} | Output frequency ^a | <div>÷2 output</div> <div>÷4 output</div> <div>÷6 output</div> <div>÷8 output</div> <div>÷10 output</div> <div>÷12 output</div> <div>÷16 output</div> <div>÷20 output</div> <div>÷24 output</div> | <div>100.0</div> <div>50.0</div> <div>33.3</div> <div>25.0</div> <div>20.0</div> <div>16.6</div> <div>12.5</div> <div>10.0</div> <div>8.33</div> | | <div>240.0</div> <div>120.0</div> <div>80.0</div> <div>60.0</div> <div>48.0</div> <div>40.0</div> <div>30.0</div> <div>24.0</div> <div>20.0</div> | <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> <div>MHz</div> |
| f_{STOP_CLK} | Serial interface frequency | | | | 20.0 | MHz |
| V_{PP} | Peak to Peak Input Voltage PECL and \overline{PECL} | LVPECL | 400 | | 1000 | mV |
| V_{CMR} | Common Mode Range PECL and \overline{PECL} | LVPECL | 1.2 | | $V_{DD} - 0.9$ | V |
| t_{PW} | CLKx pulse width | | 2.0 | | | ns |
| t_{tR}, t_{tF} | Input CLKx Rise/Fall time | 0.8V to 2.0V | | | 1 | ns |
| $t_{(\phi)}$ | Propagation Delay (static phase offset) CLKx to FB_IN ^b | <div>$6.25MHz < f_{REF} < 65.0MHz$</div> <div>$65.0MHz < f_{REF} < 125MHz$</div> <div>$f_{REF} = 50MHz \text{ \& } FB = \div 8$</div> | <div>-3</div> <div>-4</div> <div>-166</div> | | <div>+3</div> <div>+4</div> <div>+166</div> | <div>°</div> <div>°</div> <div>ps</div> |
| $t_{SK(O)}$ | Output to output skew | <div>Bank A (QAx to QAy)</div> <div>Bank B (QBx to QBy)</div> <div>Bank C (QCx to QCy)</div> <div>all outputs (QXy to QWz)^c</div> | | | <div>100</div> <div>100</div> <div>100</div> <div>250</div> | <div>ps</div> <div>ps</div> <div>ps</div> <div>ps</div> |
| DC | Output duty cycle ^d | | $(T \div 2) - 200$ | $T \div 2$ | $(T \div 2) + 200$ | ps |
| O_{tR}, O_{tF} | Output Rise/Fall time | 0.55 to 2.4V | 0.1 | | 1.0 | ns |

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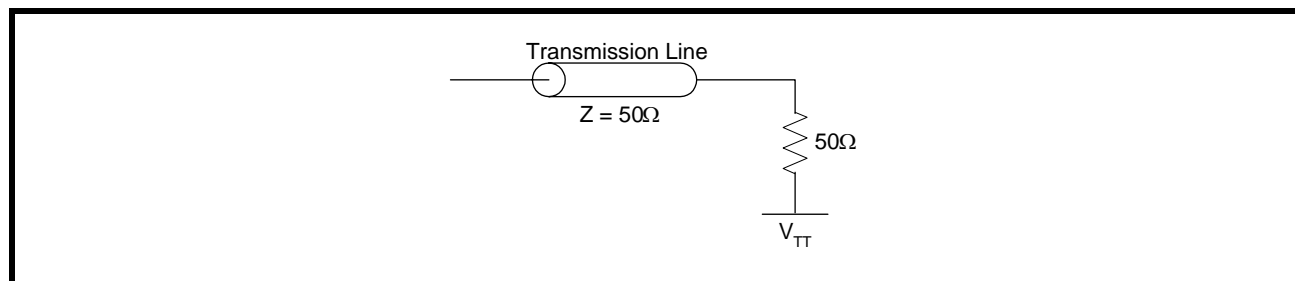
TABLE 5: AC CHARACTERISTICS (CON'T) ($V_{DD} = 3.3V \pm 5\%$)

| SYMBOL | CHARACTERISTICS | CONDITION | MIN | TYP | MAX | UNIT |
|----------------------|--|-------------------------------------|-----|-----------|-----|------|
| t_{PLZ}, t_{PHZ} | Output Disable Time | | | | 8 | ns |
| t_{PZL}, t_{PZH} | Output Enable Time | | | | 8 | ns |
| $t_{JIT(CC)}$ | Cycle-to-Cycle Jitter | All outputs in same divider config. | | 150 | 200 | ps |
| $t_{JIT(PER)}$ | Period Jitter | All outputs in same divider config. | | | 150 | ps |
| $t_{JIT(\emptyset)}$ | I/O Phase Jitter RMS (1σ) VCO = 400MHz | $\div 4$ feedback | | | 11 | ps |
| | | $\div 6$ feedback | | | 86 | ps |
| | | $\div 8$ feedback | | | 13 | ps |
| | | $\div 10$ feedback | | | 88 | ps |
| | | $\div 12$ feedback | | | 16 | ps |
| | | $\div 16$ feedback | | | 19 | ps |
| | | $\div 20$ feedback | | | 21 | ps |
| | | $\div 24$ feedback | | | 22 | ps |
| | | $\div 32$ feedback | | | 27 | ps |
| | | $\div 40$ feedback | | | 30 | ps |
| BW | PLL closed loop bandwidth | $\div 4$ feedback | | 1.20-3.5 | | MHz |
| | | $\div 6$ feedback | | 0.70-2.50 | | MHz |
| | | $\div 8$ feedback | | 0.50-1.80 | | MHz |
| | | $\div 10$ feedback | | 0.45-1.20 | | MHz |
| | | $\div 12$ feedback | | 0.30-1.00 | | MHz |
| | | $\div 16$ feedback | | 0.25-0.70 | | MHz |
| | | $\div 20$ feedback | | 0.20-0.55 | | MHz |
| | | $\div 24$ feedback | | 0.17-0.40 | | MHz |
| | | $\div 32$ feedback | | 0.12-0.30 | | MHz |
| | | $\div 40$ feedback | | 0.11-0.28 | | MHz |
| t_{LOCK} | PLL Lock Time | | | | 10 | ms |

NOTES:

- PLL locked, except when configured in bypass mode.
- $t_{(\emptyset)}[s] = t_{(\emptyset)}[^\circ] \div (\text{fref} \times 360^\circ)$
- Not including Qsync output
- T is the output period.

FIGURE 3. TEST LOAD



2.0 CONFIGURATION TABLES

TABLE 6: FUNCTION CONTROLS

| CONTROL PIN | Logic 0 | Logic 1 |
|-------------|---|--|
| MR/OE | Resets the output divide circuitry and serial interface, tri-states all outputs | Enables all outputs - normal operation |
| PLL_EN | PLL bypass mode enabled. This is a test mode in which the reference clock is provided to the output dividers in place of the VCO. | PLL enabled - normal operation |
| REF_SEL | CLKx selected as ref source to PLL | PECL & $\overline{\text{PECL}}$ inputs selected as ref source to PLL |
| CLK_SEL | CLK0 selected | CLK1 selected |
| INV_CLK | QC2 & QC3 are in phase with QC1 & QC4 | QC2 & QC3 are 180° out of phase with QC1 & QC4 |
| VCO_SEL | VCO \div 2 | no divide of VCO |

TABLE 7: BANK OUTPUT DIVIDER CONTROLS

| INPUT | | OUTPUT | INPUT | | OUTPUT | INPUT | | OUTPUT |
|---------|---------|-----------|---------|---------|-----------|---------|---------|----------|
| FSEL_A1 | FSEL_A0 | QA | FSEL_B1 | FSEL_B0 | QB | FSEL_C1 | FSEL_C0 | QC |
| 0 | 0 | \div 4 | 0 | 0 | \div 4 | 0 | 0 | \div 2 |
| 0 | 1 | \div 6 | 0 | 1 | \div 6 | 0 | 1 | \div 4 |
| 1 | 0 | \div 8 | 1 | 0 | \div 8 | 1 | 0 | \div 6 |
| 1 | 1 | \div 12 | 1 | 1 | \div 10 | 1 | 1 | \div 8 |

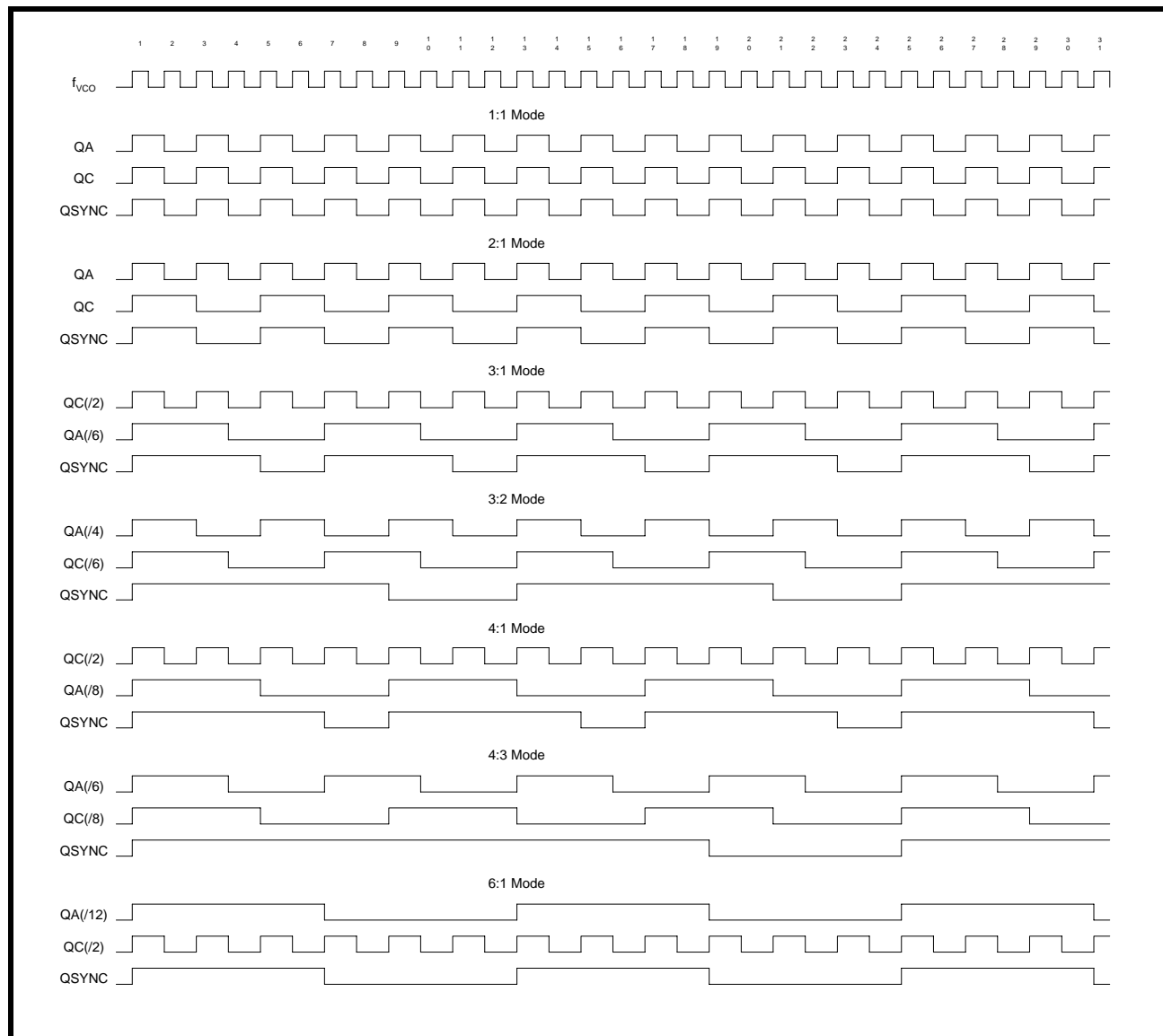
TABLE 8: FEEDBACK DIVIDER CONTROL

| FSEL_FB2 | FSEL_FB1 | FSEL_FB0 | QFB |
|----------|----------|----------|-----------|
| 0 | 0 | 0 | \div 4 |
| 0 | 0 | 1 | \div 6 |
| 0 | 1 | 0 | \div 8 |
| 0 | 1 | 1 | \div 10 |
| 1 | 0 | 0 | \div 8 |
| 1 | 0 | 1 | \div 12 |
| 1 | 1 | 0 | \div 16 |
| 1 | 1 | 1 | \div 20 |

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3.0 QSYNC TIMING

FIGURE 4. QSYNC TIMING DIAGRAM



XRK697H73 INDIVIDUAL OUTPUT DISABLE (STOP CLOCK) CIRCUITRY

The user can write to the serial input register through the STOP_DATA input by supplying a logic '0' start bit followed serially by 12 NRZ disable/enable bits. The period of each STOP_DATA bit equals the period of the free-running STOP_CLK signal. The STOP_DATA serial transmission should be timed so the XRK697H73 can sample each STOP_DATA bit with the rising edge of the free-running STOP_CLK signal. A logic "0" to any stop bit location will disable the corresponding device output while a logic "1" will enable. All outputs are by default, enabled.

FIGURE 5. STOP CLOCK CIRCUIT PROGRAMMING

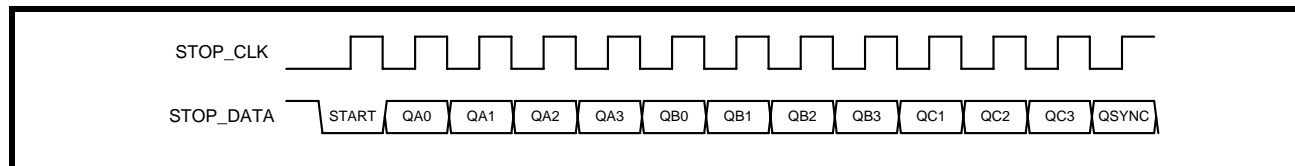


FIGURE 6. OUTPUT-TO-OUTPUT SKEW $t_{SK(O)}$

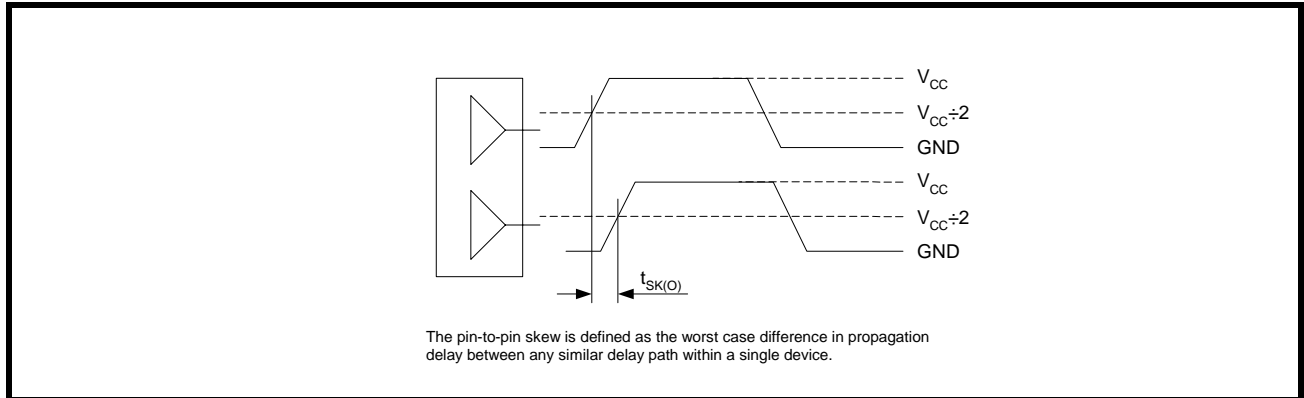


FIGURE 7. PROPOGATION DELAY (t_{ϕ} , STATIC PHASE OFFSET) TEST REFERENCE

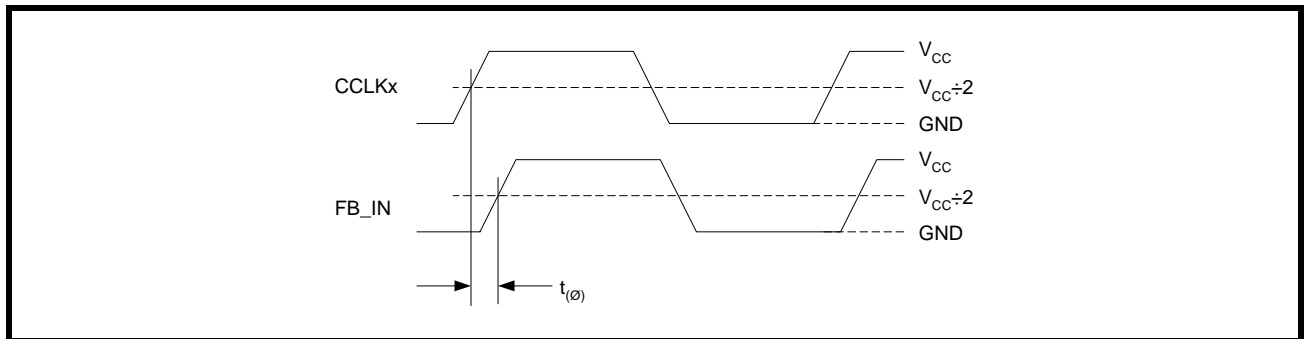


FIGURE 8. OUTPUT DUTY CYCLE (DC)

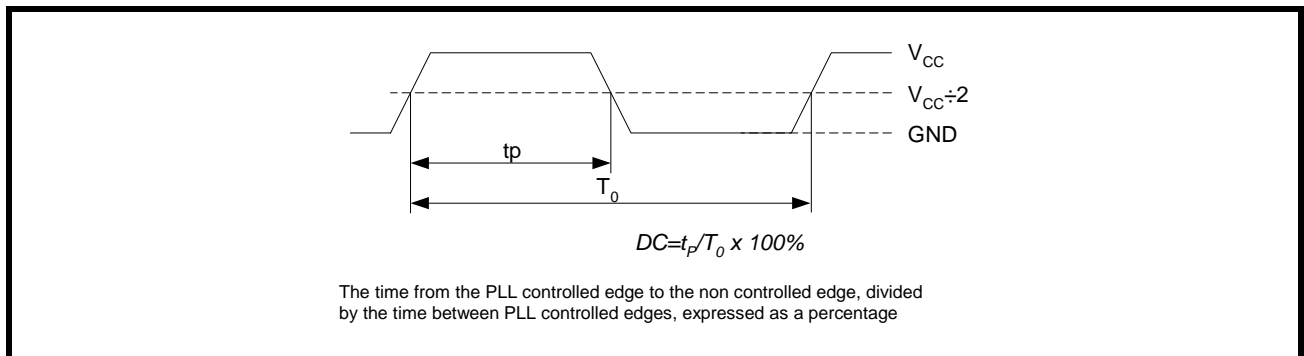


FIGURE 9. I/O JITTER

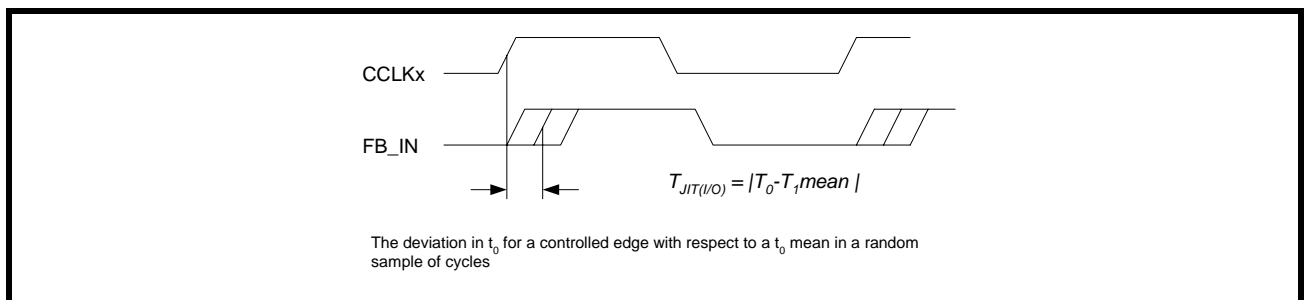


FIGURE 10. CYCLE-TO-CYCLE JITTER

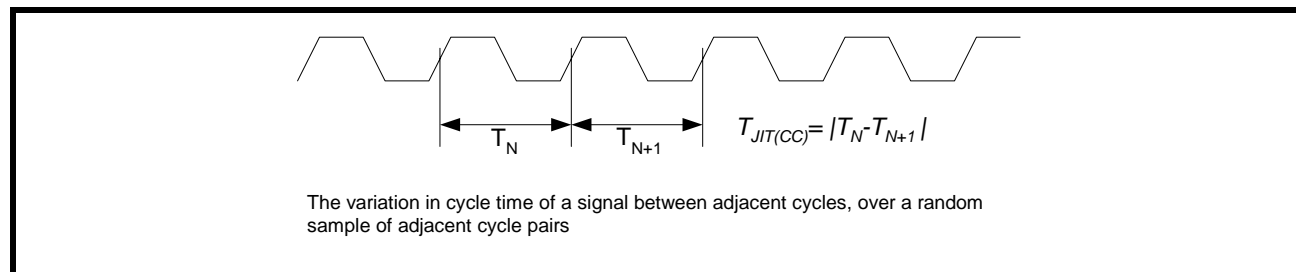


FIGURE 11. PERIOD JITTER

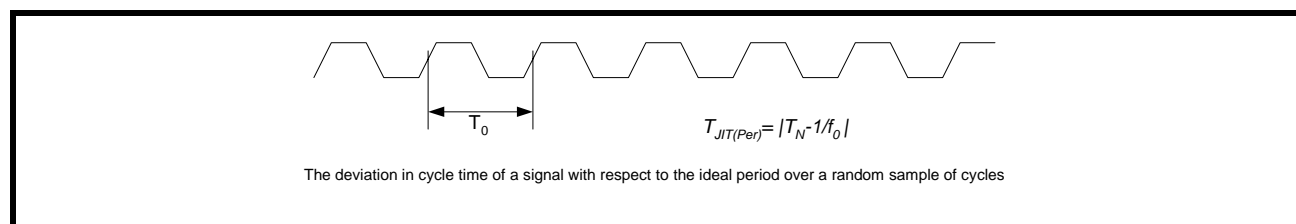
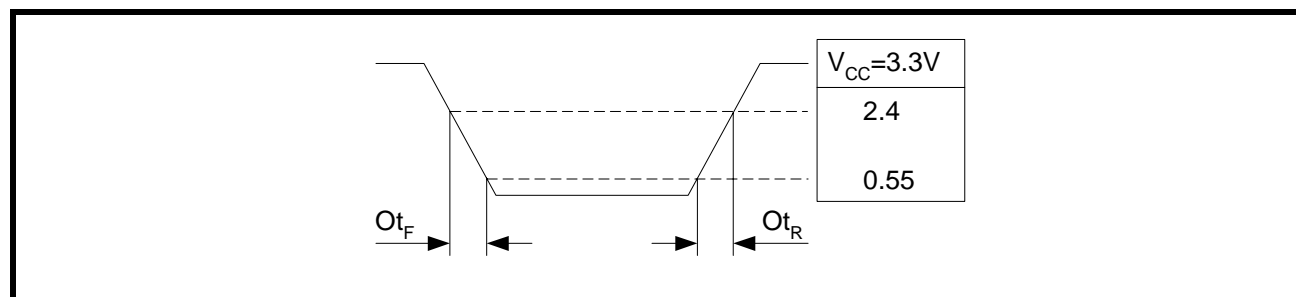


FIGURE 12. OUTPUT TRANSITION TIME TEST REFERENCE



PACKAGE DIMENSIONS

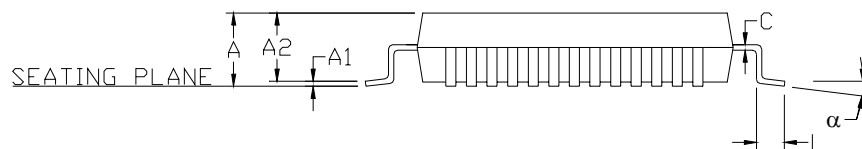
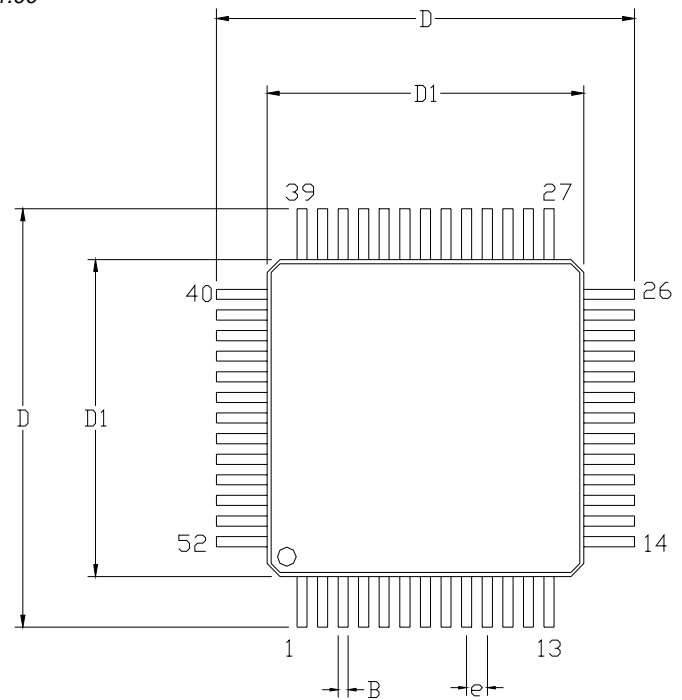
E

52 LEAD LOW-PROFILE QUAD FLAT PACK
(10 mm x 10 mm X 1.4 mm LQFP, 1.0 mm Form)

Rev. 1.00

Note: The control dimension is in millimeters.

| SYMBOL | INCHES | | MILLIMETERS | |
|----------|------------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.055 | 0.063 | 1.40 | 1.60 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.053 | 0.057 | 1.35 | 1.45 |
| B | 0.010 | 0.014 | 0.25 | 0.35 |
| C | 0.004 | 0.009 | 0.11 | 0.23 |
| D | 0.465 | 0.480 | 11.80 | 12.20 |
| D1 | 0.390 | 0.398 | 9.90 | 10.10 |
| e | 0.0256 BSC | | 0.65 BSC | |
| L | 0.029 | 0.041 | 0.73 | 1.03 |
| α | 0° | 7° | 0° | 7° |



1:12 LVCMOS PLL CLOCK GENERATOR**REVISION HISTORY**

| REVISION # | DATE | DESCRIPTION |
|------------|---------------|------------------|
| P1.0.0 | April 7, 2006 | Initial release. |
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