Z9951

3.3V, 180MHz, Multi-Output Zero Delay Buffer

Product Features

- 180MHz Clock Support
- Supports PowerPC™, Intel and RISC Processors
- 9 Clock Outputs: Frequency Configurable
- Two Reference Clock Inputs for Dynamic Toggling
- Oscillator or PECL Reference Input
- Output Disable Control
- Spread Spectrum Compatible
- 3.3V Power Supply
- Pin Compatible with MPC951
- Industrial Temp. Range: -40°C to +85°C
- 32-Pin TQFP Package

Block Diagram

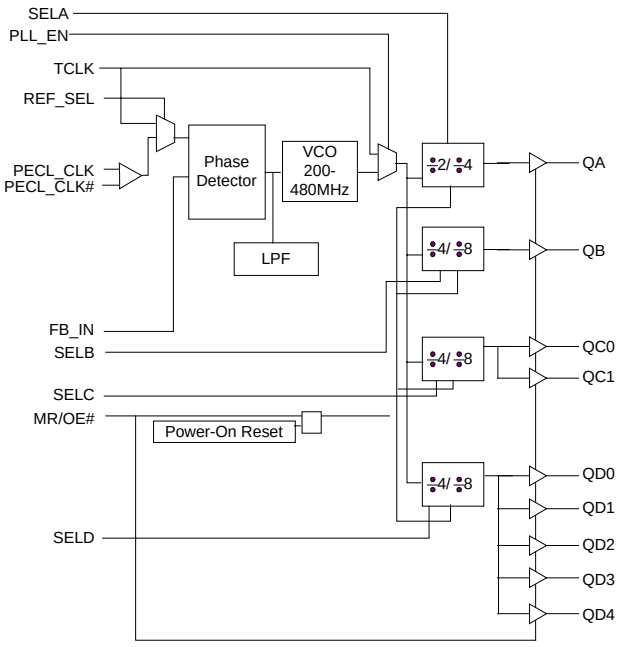


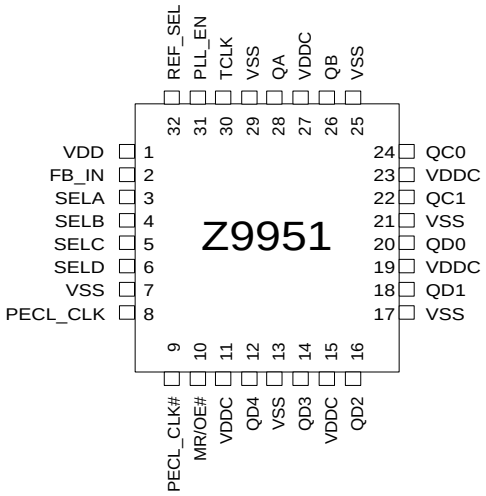
Figure 1

Frequency Table

SEL (A:D)	QA	QB	QC (0,1)	QD (0:4)
0000	VCO/2	VCO/4	VCO/4	VCO/4
0001	VCO/2	VCO/4	VCO/4	VCO/8
0010	VCO/2	VCO/4	VCO/8	VCO/4
0011	VCO/2	VCO/4	VCO/8	VCO/8
0100	VCO/2	VCO/8	VCO/4	VCO/4
0101	VCO/2	VCO/8	VCO/4	VCO/8
0110	VCO/2	VCO/8	VCO/8	VCO/4
0111	VCO/2	VCO/8	VCO/8	VCO/8
1000	VCO/4	VCO/4	VCO/4	VCO/4
1001	VCO/4	VCO/4	VCO/4	VCO/8
1010	VCO/4	VCO/4	VCO/8	VCO/4
1011	VCO/4	VCO/4	VCO/8	VCO/8
1100	VCO/4	VCO/8	VCO/4	VCO/4
1101	VCO/4	VCO/8	VCO/4	VCO/8
1110	VCO/4	VCO/8	VCO/8	VCO/4
1111	VCO/4	VCO/8	VCO/8	VCO/8

Table 1

Pin Configuration



Pin Description

PIN	NAME	PWR	I/O	TYPE	Description
8	**PECL_CLK**		I	PU	PECL Input Clock.
9	**PECL_CLK#**		I		PECL Input Clock.
30	**TCLK**		I		External Test Clock Input.
28	**QA**	VDDC	O		Clock Output. See Frequency Table.
26	**QB**	VDDC	O		Clock Output. See Frequency Table.
22, 24	**QC(1,0)**	VDDC	O		Clock Outputs. See Frequency Table.
12, 14, 16, 18, 20	**QD(4:0)**	VDDC	O		Clock Outputs. See Frequency Table.
2	**FB_IN**		I	PD	Feedback Clock Input. Connect to an output for normal operation.
10	**MR/OE#**		I		Master Reset/Output Enable Input. When asserted high, resets all of the internal flip-flops and also disables all of the outputs. When pulled low, releases the internal flip-flops from reset and enables all of the outputs.
31	**PLL_EN**		I		PLL Enable Input. When asserted high, PLL is enabled. And when set low, PLL is bypassed.
32	**REF_SEL**		I		Reference Select Input. When high, TCLK is the reference clock and when low, PECL clock is selected.
3, 4, 5, 6	**SEL(A:D)**		I		Frequency Select Inputs. See Frequency Table. If SEL_ = 1, then QA divider = ÷4, QB:D divider = ÷8 If SEL_ = 0, then QA divider = ÷2, QB:D divider = ÷4
11, 15, 19, 23, 27	**VDDC**				3.3V Power Supply for Output Clock Buffers.
1	**VDD**				3.3V Power Supply for PLL
7, 13, 17, 21, 25, 29	**VSS**				Common Ground

PD = Internal Pull-Down, PU = Internal Pull-Up.

Maximum Ratings[1]

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65°C to + 150°C
Operating Temperature: -40°C to +85°C
Maximum ESD protection 2KV
Maximum Power Supply: 5.5V
Maximum Input Current: ±20mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	VSS	-	0.8	V	
Input High Voltage	VIH	2.0	-	VDD	V	
Input Low Current (@VIL = VSS)	IIL			-120	µA	Note 2
Input High Current (@VIL =VDD)	IIH			120	µA	
Peak-to-Peak Input Voltage PECL_CLK	VPP	300		1000	mV	Note 3
Common Mode Range PECL_CLK	VCMR	VDD-2.0	-	VDD-0.6	V	
Output Low Voltage	VOL			0.5	V	IOL = 40mA, Note 4
Output High Voltage	VOH	2.4			V	IOH = -40mA, Note 4
Quiescent Supply Current	IDDC	-	15	20	mA	All VDDC and VDD
PLL Supply Current	IDD	-	15	20	mA	VDD only
Input Capacitance	Cin	-	-	4	pF	
VDD = VDDC = 3.3V ±5%, TA = -40°C to +85°C						

Note 1: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
Note 2: Inputs have pull-up, pull-down resistors that affect input current.
Note 3: The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the VCMR range and the input lies within the VPP specification.
Note 4: Driving series or parallel terminated 50Ω (or 50Ω to VDD/2) transmission lines. Output buffers are dual staged to control drive strength in order to reduce over / under shoot.

AC Parameters[1]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Tr / Tf	TCLK Input Rise / Fall			3.0	ns	
Fref	Reference Input Frequency	Note 2		Note 2	MHz	
FrefDC	Reference Input Duty Cycle	25		75	%	
Fvco	PLL VCO Lock Range	200		480	MHz	
Tlock	Maximum PLL lock Time			10	ms	
Tr / Tf	Output Clocks Rise / Fall Time[4,5]	0.10		1.0	ns	0.8V to 2.0V
Fout	Maximum Output Frequency	-		180	MHz	QA = (÷2)
				120		QA/QB = (÷4)
				60		QB = (÷8)
FoutDC	Output Duty Cycle[4,5]	TCYCLE/2 – 1		TCYCLE/2 + 1	ns	
tpZL, tpZH	Output enable time (all outputs)			6	ns	
tpLZ, tpHZ	Output disable time (all outputs)			7	ns	
TCCJ	Cycle to Cycle Jitter (peak to peak)[4,5]		+/- 100		ps	
Tpd	TCLK to FB_IN Delay[3]	50	250	400	ps	Fref = 50MHz, Feedback = VCO/8
	PECL_CLK to FB_IN Delay[3]	-950	-770	-600	ps	
TSKEW0	Any Output to Any Output Skew[4,5]	-	200	350	ps	
VDD = VDDC = 3.3V +/- 5%, TA = -40°C to +85°C						

Note 1: Parameters are guaranteed by design and characterization. Not 100% tested in production.
Note 2: Maximum and minimum input reference is limited by the VCO lock range.
Note 3: The Tpd window is specified for a 50MHz input reference clock. The window will enlarge/reduce proportionally from the minimum limits with an increase/decrease of the input reference clock period.
Note 4: Driving series or parallel terminator 50Ω (or 50Ω to VDD/2) transmission lines.
Note 5: Outputs loaded with 30pF each

Description

The Z9951 has an integrated PLL that provides low skew and low jitter clock outputs for high performance microprocessors. The PLL is ensured stable operation given that the VCO is configured to run between 200 MHz to 480 MHz. This allows a wide range of output frequencies from 25MHz to 180MHz.

The phase detector compares the input reference clock to the external feedback input. For normal operation, the external feedback input, FB_IN, is connected to one of the outputs. The internal VCO is running at multiples of the input reference clock set by SEL(A:D) select inputs, see Table 2. The VCO frequency is then divided down to provide the required output frequencies. The use of even dividers ensures that the output duty cycle remains at 50%.

SELA	QA	SELB	QB	SELC	QC	SELD	QD
0	÷2	0	÷4	0	÷4	0	÷4
1	÷4	1	÷8	1	÷8	1	÷8

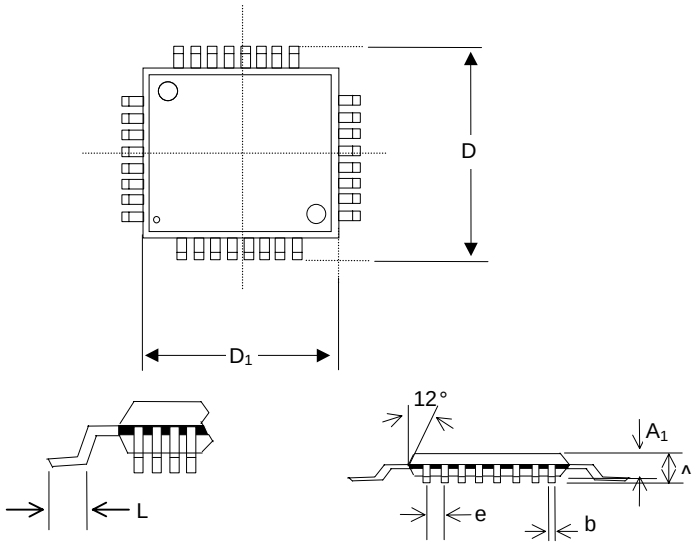
Table 2

Zero Delay Buffer

When used as a zero delay buffer the Z9951 will likely be in a nested clock tree application. For these applications the Z9951 offers a low voltage PECL clock input as a PLL reference. This allows the user to use LVPECL as the primary clock distribution device to take advantage of its far superior skew performance. The Z9951 then can lock onto the LVPECL reference and translate with near zero delay to low skew outputs.

By using one of the outputs as a feedback to the PLL the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs. Because the static phase offset is a function of the reference clock the Tpd of the Z9951 is a function of the configuration used.

Package Drawing and Dimensions



32 Pin TQFP Outline Dimensions

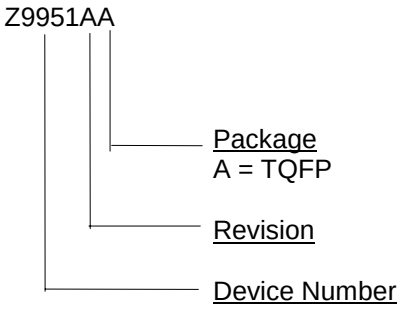
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.037	-	0.041	0.95	-	1.05
D	-	0.354	-	-	9.00	-
D_1	-	0.276	-	-	7.00	-
b	0.012	-	0.018	0.30	-	0.45
e	0.031 BSC			0.80 BSC		
L	0.018	-	0.030	0.45	-	0.75

Ordering Information

Part Number	Package Type	Production Flow
Z9951AA	32 PIN TQFP	Industrial, -40°C to +85°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
Z9951AA
Date Code, Lot #



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Document Title: Z9951 3.3V, 180 MHz, Multi-Output Zero Delay Buffer
Document Number: 38-07084

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	107120	06/12/01	IKA	Convert from IMI to Cypress
*A	108063	07/03/01	NDP	Changed Commercial to Industrial (See page 7) Delete Pull down in pin 9,10,30& 32; Delete Pull up in pin 3,4,5,6, & 31 (See page 2)
*B	122769	12/22/02	RBI	Add power up requirements to maximum ratings information