Z9953

3.3V, 180MHz, Multi-Output Zero Delay Buffer

Product Features

- 110MHz Clock Support
- Supports PowerPC™, Intel and RISC Processors
- 9 Clock Outputs: drive up to 18 loads
- LVPECL Reference Input Clock
- Output Disable Control
- Spread Spectrum Compatible
- 3.3V Power Supply
- Pin Compatible with MPC953
- Industrial Temp. Range: -40°C to +85°C
- 32-Pin TQFP Package

Frequency Table

BYPASS#	PLL_EN	VCO_SEL	Q(0:7)	FB_OUT
0	0	0	REF	REF
0	0	1	REF	REF
0	1	0	REF	REF
0	1	1	REF	REF
1	0	0	REF/4	REF/4
1	0	1	REF/8	REF/8
1	1	0	VCO/4	VCO/4
1	1	1	VCO/8	VCO/8

Table 1

Function Table

BYPASS#	'**1**' = PLL Enabled '**0**' = PLL Bypass
MR/OE#	'**1**' = Outputs Disabled HiZ '**0**' = Outputs Enabled
VCO_SEL	'**1**' = VCO/2 '**0**' = VCO
PLL_EN	'**1**' = Select VCO '**0**' = Select PECL_CLK

Table 2

Block Diagram

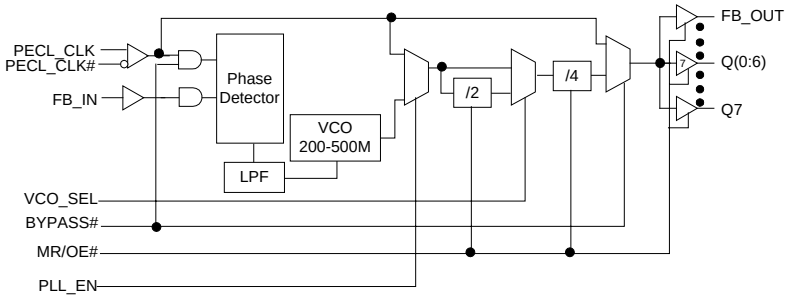
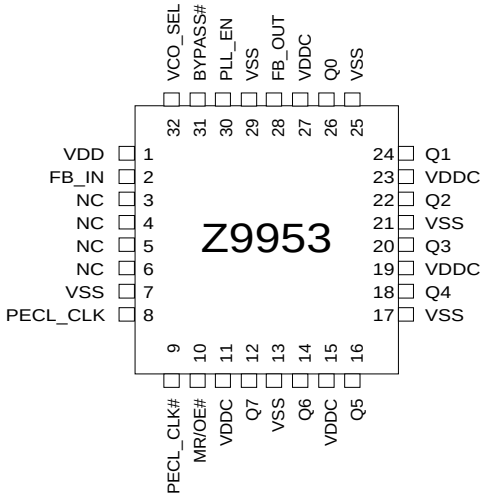


Figure 1

Pin Configuration



Pin Description

PIN	NAME	PWR	I/O	Description
8	**PECL_CLK**		I	PECL Input Clock.
9	**PECL_CLK#**		I	PECL Input Clock.
12, 14, 16, 18, 20, 22, 24, 26	**Q(7:0)**	VDDC	O	Clock Output.
28	**FB_OUT**	VDDC	O	Feedback Clock Output. Connect to FB_IN for normal operation. A bypass delay capacitor at this output will control Input Reference / Output phase relationships.
2	**FB_IN**		I	Feedback Clock Input. Connect to FB_OUT for accessing the PLL.
10	**MR/OE#**		I	Master Reset/Output Enable Input. When asserted high, resets all of the internal flip-flops and also disables all of the outputs. When pulled low, releases the internal flip-flops from reset and enables all of the outputs.
30	**PLL_EN**		I	PLL Select Input. When asserted high, VCO output is selected. And when set low, PECL_CLK is the input to the output dividers.
31	**BYPASS#**		I	PLL Enable Input. When high, PLL is enabled and when low, PLL is bypassed.
32	**VCO_SEL**		I	VCO Divider Select Input. When set high, VCO output is divided by 2. When set low, the divider is bypassed.
11, 15, 19, 23, 27	**VDDC**			3.3V Power Supply for Output Clock Buffers.
1	**VDD**			3.3V Power Supply for PLL
7, 13, 17, 21, 25, 29	**VSS**			Common Ground
3, 4, 5, 6	**NC**			No Connection

PD = Internal Pull-Down, PU = Internal Pull-Up.

Maximum Ratings[1]

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65°C to + 150°C
Operating Temperature: -40°C to +85°C
Maximum ESD protection 2KV
Maximum Power Supply: 5.5V
Maximum Input Current: ±20mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	VSS	-	0.8	V	
Input High Voltage	VIH	2.0	-	VDD	V	
Input Low Current (@VIL = VSS)	IIL			-120	µA	Note 2
Input High Current (@VIL =VDD)	IIH			120	µA	
Peak-to-Peak Input Voltage PECL_CLK	VPP	300		1000	mV	Note 3
Common Mode Range PECL_CLK	VCMR	VDD-1.5	-	VDD-0.6	V	
Output Low Voltage	VOL			0.6	V	IOL = 20mA, Note 4
Output High Voltage	VOH	VDD-0.6			V	IOH = -20mA, Note 4
Quiescent Supply Current	IDDC	-	-	20	mA	All VDDC and VDD
PLL Supply Current	IDD	-	15	20	mA	VDD only
Input Capacitance	Cin	-	-	4	pF	
VDD = VDDC = 3.3V ±5%, TA = -40°C to +85°C						

Note 1: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
Note 2: Inputs have pull-up, pull-down resistors that affect input current.
Note 3: The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the VCMR range and the input lies within the VPP specification.
Note 4: Driving series or parallel terminated 50Ω (or 50Ω to VDD/2) transmission lines. Output buffers are dual staged to control drive strength in order to reduce over/under shoot.

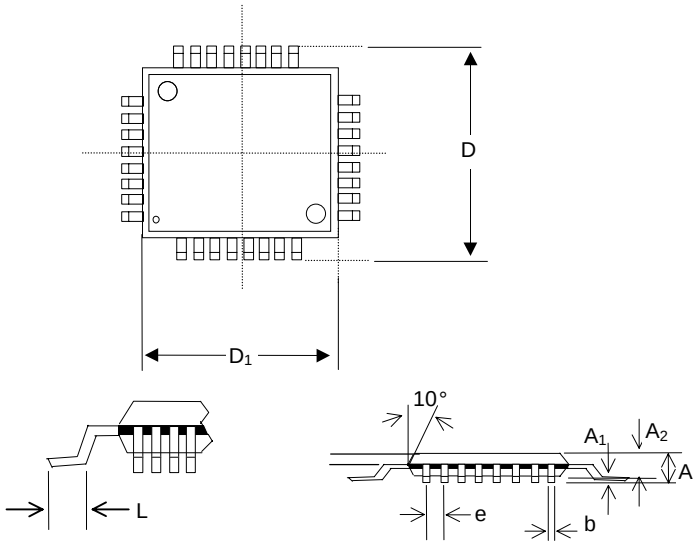
AC Parameters[1]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Tr / Tf	TCLK Input Rise / Fall			3.0	ns	
Fref	Reference Input Frequency[2]	25		110	MHz	
FrefDC	Reference Input Duty Cycle	25		75	%	
Fvco	PLL VCO Lock Range	200		500	MHz	
Tlock	Maximum PLL lock Time			10	ms	
Tr / Tf	Output Clocks Rise / Fall Time[4,5]	0.10		1.0	ns	0.8V to 2.0V
Fout	Maximum Output Frequency	50		110	MHz	VCO_SEL = '0'
		25		62.5		VCO_SEL = '1'
				200		Bypass Mode
FoutDC	Output Duty Cycle[4,5]	45	50	55	%	
TCCJ	Cycle to Cycle Jitter (peak to peak)[4,5]			100	ps	
TSKEW	Any Output to Any Output Skew[4,5]	-	-	250	ps	
Tpd	Input to FB_IN Delay (PLL locked)[3,4,5]	-75	-	125	ps	
tpZL, tpZH	Output enable time (all outputs)			6	ns	
tpLZ, tpHZ	Output disable time (all outputs)			7	ns	
Tpd	Input to Q Delay (PLL bypassed)	3		7	ns	
VDD = VDDC = 3.3V +/- 5%, TA = -40°C to +85°C						

Note 1: Parameters are guaranteed by design and characterization. Not 100% tested in production.
Note 2: Maximum and minimum input reference is limited by the VCO lock range.
Note 3: The Tpd (PLL locked) is input reference frequency dependent.
Note 4: Driving series or parallel terminator 50Ω (or 50Ω to VDD/2) transmission lines.
Note 5: Outputs loaded with 30pF each

Description

The Z9953 is a PLL based clock generator that provides low skew and low jitter clock outputs for high performance systems. The Z9953 features a differential PLL to minimize cycle-to-cycle and phase jitter. The PLL is ensured stable operation given that the VCO is configured to run between 200MHz and 500MHz.
The input reference is a differential LVPECL clock. All other control inputs are LVCMOS/LVTTL compatible The Z9953 features 9 LVCMOS/LVTTL compatible outputs each capable of driving two series terminated 50Ω transmission lines. With this capability the Z9953 has an effective fan-out of 1:18. The outputs can also be tri-stated when MR/OE# is set high.
When used as a zero-delay buffer any of the 9 outputs can be used as the feedback input to the PLL. The PLL works to align the output edge with the input reference edge thus producing a near zero delay.



32 Pin TQFP Outline Dimensions

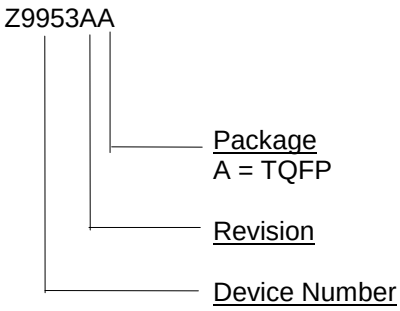
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.037	-	0.041	0.95	-	1.05
D	-	0.354	-	-	9.00	-
D_1	-	0.276	-	-	7.00	-
b	0.012	-	0.018	0.30	-	0.45
e	0.031 BSC			0.80 BSC		
L	0.018	-	0.030	0.45	-	0.75

Ordering Information

Part Number	Package Type	Production Flow
Z9953AA	32 PIN TQFP	Industrial, -40°C to +85°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
Z9953AA
Date Code, Lot #



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Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	107122	06/05/01	IKA	Convert from IMI to Cypress
*A	108065	07/03/01	NDP	Changed Commercial to Industrial (See page 5)
*B	122771	12/26/02	RBI	Add power up requirements to maximum ratings information