Dual, 12-/14-/16-Bit *nano*DACs® with 5ppm/°C On-Chip Ref, I²C Interface

AD5627R/AD5647R/AD5667R AD5627/AD5667

Preliminary Technical Data

FEATURES

Low power, smallest pin-compatible, dual *nano*DACs
AD5627R/AD5647R/AD5667R
- **12-/14-/16- bit**
- **On-chip 1.25 V/2.5 V, 5 ppm/°C reference**

AD5625/AD5665
- **12-/16- bit**
- **External reference only**

3 mm x 3 mm LFCSP and 10-lead MSOP
2.7 V to 5.5 V power supply
Guaranteed monotonic by design
Power-on reset to zero scale
Per channel power-down
I²C-compatible serial interface supports standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) modes

APPLICATIONS

Process control
Data acquisition systems
Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators

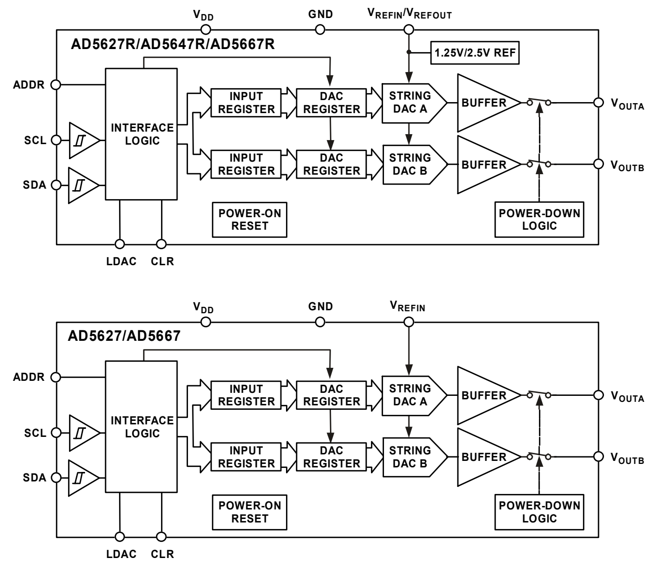

Figure 1. Functional Block Diagrams

GENERAL DESCRIPTION

The AD5627R/AD5647R/AD5667R, AD5627/AD5667, members of the *nano*DAC family, are low power, dual, 12-, 14-, 16-bit buffered voltage-out DACs with/without on-chip reference. All devices operate from a single 2.7 V to 5.5 V supply, are guaranteed monotonic by design and have an I²C-compatible serial interface .

The AD5627R/AD5647R/AD5667R have an on-chip reference. The AD56x7RBCPZ have a 1.25 V, 5 ppm/°C reference, giving a full-scale output range of 2.5 V; the AD56x7RBRUZ have a 2.5 V, 5 ppm/°C reference giving a full-scale output range of 5 V. The on-chip reference is off at power-up, allowing the use of an external reference. The internal reference is enabled via a software write. The AD5667 and AD5627 require an external reference voltage to set the output range of the DAC

The part incorporates a power-on reset circuit that ensures the DAC output powers up to 0 V and remains there until a valid write takes place. The part contains a per-channel power-down feature that reduces the current consumption of the device to 480 nA at 5 V and provides software-selectable output loads while in power-down mode. The low power consumption of this part in normal operation makes it ideally suited to portable battery-operated equipment. The on-chip precision output amplifier enables rail-to-rail output swing.

The AD5627R/AD5647R/AD5667R, AD5627/AD5667 use a 2-wire I²C-compatible serial interface that operates in standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) modes.

Table 1. Related Devices

Part No.	Description
AD5663	2.7 V to 5.5 V, Dual 16-bit DAC, external reference, SPI interface
AD5623R/AD5643R/AD5663R	2.7 V to 5.5 V, Dual 12-, 14-, 16-bit DACs, internal reference, SPI interface
AD5625R/AD5645R/AD5665R AD5625/AD5665	2.7 V to 5.5 V, quad 12-, 14- 16-bit DACs, with/without internal reference, I²C interface

Rev. PrA

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REVISION HISTORY

4/06—Revision 0: Initial Version

Specifications: AD5627R/AD5647R/AD5667R, AD5627/AD5667

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; V_{REFIN} = V_{DD}; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	B Grade[1] Min	Typ	Max	Unit	Conditions/Comments
STATIC PERFORMANCE[2]					
AD5667R/AD5667					
Resolution	16			Bits	
Relative Accuracy		±8	±16	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic by design
AD5647R					
Resolution	14			Bits	
Relative Accuracy		±2	±4	LSB	
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic by design
AD5627R/AD5627					
Resolution	12			Bits	
Relative Accuracy		±0.5	±1	LSB	
Differential Nonlinearity			±0.25	LSB	Guaranteed monotonic by design
Zero-Code Error		2	10	mV	All zeroes loaded to DAC register
Offset Error		±1	±10	mV	
Full-Scale Error		−0.1	±1	% of FSR	All ones loaded to DAC register
Gain Error			±1.5	% of FSR	
Zero-Code Error Drift		±2		μV/°C	
Gain Temperature		±2.5		ppm	Of FSR/°C
DC Power Supply Rejection		−100		dB	DAC code = midscale ; V_{DD} = 5V ± 10%
DC Crosstalk (External Reference)		10		μV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10		μV/mA	Due to load current change
		5		μV	Due to powering down (per channel)
DC Crosstalk (Inernal Reference)		25		μV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		20		μV/mA	Due to load current change
		10		μV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Capacitive Load Stability		2		nF	$R_L = \infty$
		10		nF	R_L = 2 kΩ
DC Output Impedance		0.5		Ω	
Short-Circuit Current		30		mA	V_{DD} = 5 V
Power-Up Time		4		μs	Coming out of power-down mode; V_{DD} = +5 V
REFERENCE INPUTS					
Reference Current		170	200	μA	V_{REF} = V_{DD} = 5.5 V
Reference Input Range	0.75		V_{DD}	V	
Reference Input Impedance		26		kΩ	
REFERENCE OUTPUT (LFCSP PACKAGE)					
Output Voltage	1.247		1.253	V	At ambient
Reference TC[3]		±10		ppm/°C	
Output Impedance		7.5		kΩ	
REFERENCE OUTPUT (MSOP PACKAGE)					
Output Voltage	2.495		2.505	V	At ambient
Reference TC[3]		±5	±10	ppm/°C	
Output Impedance		7.5		kΩ	

Parameter	B Grade[1] Min	Typ	Max	Unit	Conditions/Comments
LOGIC INPUTS (SDA, SCL)					
I_{IN}, Input Current			±1	µA	
V_{INL}, Input Low Voltage			0.3 × V_{DD}	V	
V_{INH}, Input High Voltage	0.7 × V_{DD}			V	
C_{IN}, Pin Capacitance		2		pF	
V_{HYST}, Input Hysteresis	0.1 × V_{DD}			V	
LOGIC OUTPUTS (OPEN DRAIN)					
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA
Floating-State Leakage Current			±1	µA	
Floating-State Output		2		pF	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD} (Normal Mode)[4]					V_{IH} = V_{DD}, V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		0.45	0.55	mA	Internal reference off
V_{DD} = 2.7 V to 3.6 V		0.44	0.5	mA	Internal reference off
V_{DD} = 4.5 V to 5.5 V		0.95	1.2	mA	Internal reference on
V_{DD} = 2.7 V to 3.6 V		0.95	1.15	mA	Internal reference on
I_{DD} (All Power-Down Modes)[5]		0.48	1	µA	V_{IH} = V_{DD}, V_{IL} = GND

[1] Temperature range: B grade: −40°C to +105°C.
[2] Linearity calculated using a reduced code range: AD5667 (Code 512 to Code 65,024); AD5647 (Code 128 to Code 16,256); AD5627 (Code 32 to Code 4064). Output unloaded.
[3] Guaranteed by design and characterization, not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; V_{REFIN} = V_{DD}; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 4.

Parameter[2]	Min	Typ	Max	Unit	Conditions/Comments[3]
Output Voltage Settling Time					
AD5627R/AD5627		3	4.5	µs	¼ to ¾ scale settling to ±0.5 LSB
AD5647R		3.5	5	µs	¼ to ¾ scale settling to ±0.5 LSB
AD5667R/AD5667		4	7	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		1.8		V/µs	
Digital-to-Analog Glitch Impulse		10		nV-s	1 LSB change around major carry
Digital Feedthrough		0.1		nV-s	
Reference Feedthrough		−90		dBs	V_{REF} = 2 V ± 0.1 V p-p, frequency 10 Hz to 20 MHz
Digital Crosstalk		0.1		nV-s	
Analog Crosstalk		1		nV-s	External reference
		4		nV-s	Internal reference
DAC-to-DAC Crosstalk		1		nV-s	External reference
		4		nV-s	Internal reference
Multiplying Bandwidth		340		kHz	V_{REF} = 2 V ± 0.1 V p-p
Total Harmonic Distortion		−80		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density		120		nV/√Hz	DAC code = midscale, 1 kHz
		100		nV/√Hz	DAC code = midscale, 10 kHz
Output Noise		15		µV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization, not production tested.
[2] See the Terminology section.

[3] Temperature range is −40°C to +105°C, typical at 25°C.

I²C TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, f_{SCL} = 3.4 MHz, unless otherwise noted.[1]

Table 5.

Parameter	Conditions[2]	Limit at T_{MIN}, T_{MAX} Min	Max	Unit	Description
f_{SCL}[3]	Standard mode		100	KHz	Serial clock frequency
	Fast mode		400	KHz	
	High speed mode, C_B = 100 pF		3.4	MHz	
	High speed mode, C_B = 400 pF		1.7	MHz	
t_1	Standard mode	4		µs	t_{HIGH}, SCL high time
	Fast mode	0.6		µs	
	High speed mode, C_B = 100 pF	60			ns
	High speed mode, C_B = 400 pF	120			ns
t_2	Standard mode	4.7		µs	t_{LOW}, SCL low time
	Fast mode	1.3		µs	
	High speed mode, C_B = 100 pF	160		ns	
	High speed mode, C_B = 400 pF	320		ns	
t_3	Standard mode	250		ns	$t_{SU;DAT}$, data setup time
	Fast mode	100		ns	
	High speed mode	10		ns	
t_4	Standard mode	0	3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0	0.9	µs	
	High speed mode, C_B = 100 pF	0	70	ns	
	High speed mode, C_B = 400 pF	0	150	ns	
t_5	Standard mode	4.7		µs	$t_{SU;STA}$, set-up time for a repeated start condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_6	Standard mode	4		µs	$t_{HD;STA}$, hold time (repeated) start condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_7	Standard mode	4.7		µs	t_{BUF}, bus free time between a stop and a start condition
	Fast mode	1.3		µs	
t_8	Standard mode	4		µs	$t_{SU;STO}$, setup time for a stop condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_9	Standard mode		1000	ns	t_{RDA}, rise time of SDA signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	
t_{10}	Standard mode		300	ns	t_{FDA}, fall time of SDA signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	
t_{11}	Standard mode		1000	ns	t_{RCL}, rise time of SCL signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	40	ns	
	High speed mode, C_B = 400 pF	20	80	ns	
t_{11A}	Standard mode		1000	ns	t_{RCL1}, rise time of SCL signal after a repeated start condition and after an acknowledge bit
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	80	ns	
	High speed mode, C_B = 400 pF	20	160	ns	

Parameter	Conditions[2]	Limit at T_{MIN}, T_{MAX} Min	Max	Unit	Description
t_{12}	Standard mode		300	ns	t_{FCL}, fall time of SCL signal
	Fast mode		300	ns	
	High speed mode, C_B = 100 pF	10	40	ns	
	High speed mode, C_B = 400 pF	20	80	ns	
t_{SP}[4]	Fast mode	0	50	ns	Pulse width of spike suppressed
	High speed mode	0	10	ns	

[1]See Figure 2. High speed mode timing specification applies only to the AD5627BRUZ-2 and AD5667BRUZ-2.
[2]CB refers to the capacitance on the bus line.
[3]The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on EMC behavior of the part.
[4] Input filtering on the SCL and SDA inputs suppress noise spikes that are less than 50 ns for fast mode or 10 ns for high speed mode.

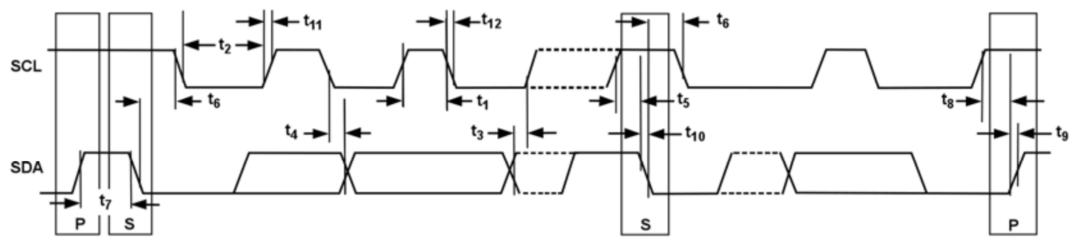


Figure 2. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

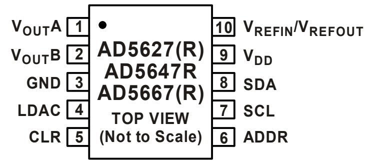
Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REFIN}/V_{REFOUT} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Power Dissipation	$(T_J \max - T_A)/\theta_{JA}$
LFCSP_WD Package (4-Layer Board)	
θ_{JA} Thermal Impedance	61°C/W
MSOP Package	
θ_{JA} Thermal Impedance	150.4°C/W
Reflow Soldering Peak Temperature	
Pb-Free	260°C ± 5°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTE. V_{REFOUT} IS AVAILABLE ONLY ON -R VERSIONS

Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No. (10-pin)	Mnemonic	Description
1	$V_{OUT}A$	Analog output voltage from DAC C. The output amplifier has rail-to-rail operation.
2	$V_{OUT}B$	Analog output voltage from DAC B. The output amplifier has rail-to-rail operation.
3	GND	Ground reference point for all circuitry on the part.
4	$\overline{\text{LDAC}}$	Active low load DAC pin.
5	$\overline{\text{CLR}}$	Asynchronous clear input. The $\overline{\text{CLR}}$ input is falling edge sensitive. While $\overline{\text{CLR}}$ is low, all LDAC pulses are ignored. When $\overline{\text{CLR}}$ is activated, zero scale is loaded to all input and DAC registers. This clears the output to 0 V. The part exits clear code mode on the 24th falling edge of the next write to the part. If $\overline{\text{CLR}}$ is activated during a write sequence, the write is aborted.
6	ADDR	Three-state address input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address.
7	SCL	Serial clock line. This is used in conjunction with the SDA line to clock data into or out of the 16-bit input register.
8	SDA	Serial data line. This is used in conjunction with the SCL line to clock data into or out of the 16-bit input register. It is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor.
9	V_{DD}	Power supply input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
10	V_{REFIN}/V_{REFOUT}	The AD5627R/AD5647R/AD5667R, AD5627/AD5667 have a common pin for reference input and reference output. The internal reference and reference output are only available on suffix –R versions. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input.

TYPICAL PERFORMANCE CHARACTERISTICS

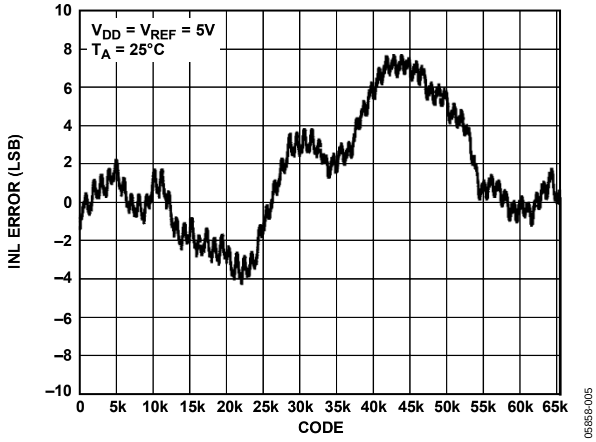


Figure 4. INL AD5667, External Reference

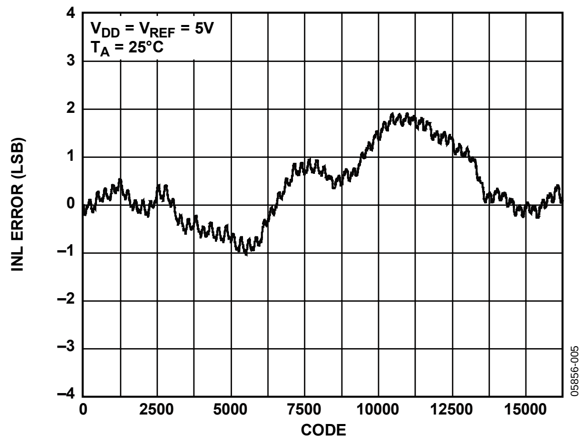


Figure 5. INL AD5647, External Reference

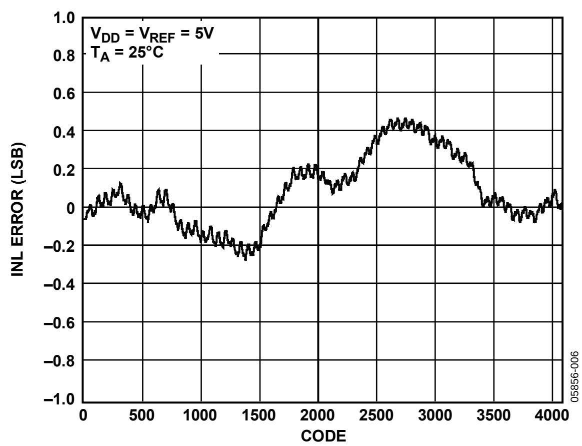


Figure 6. INL AD5627, External Reference

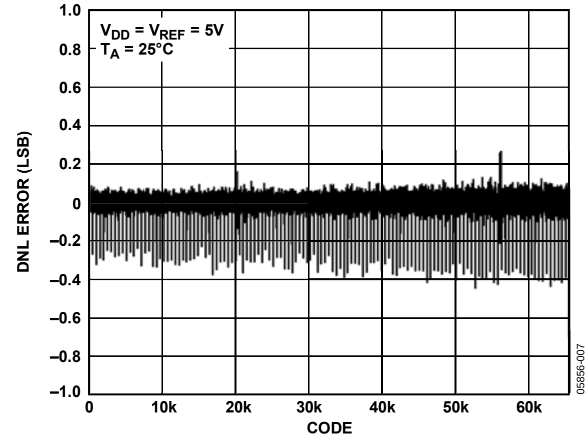


Figure 7. DNL AD5667, External Reference

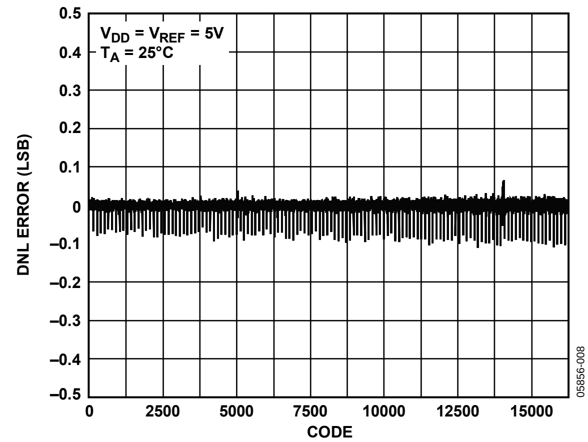


Figure 8. DNL AD5647, External Reference

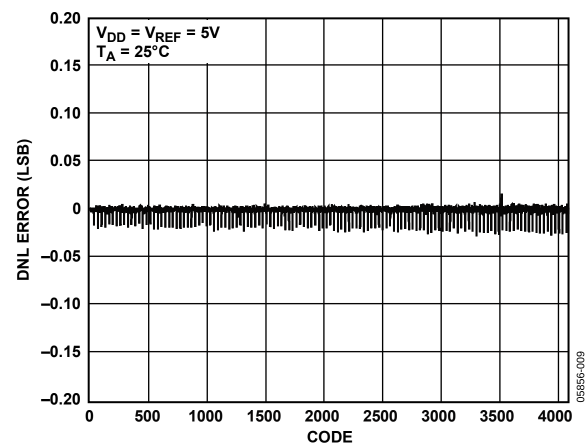


Figure 9. DNL AD5627, External Reference

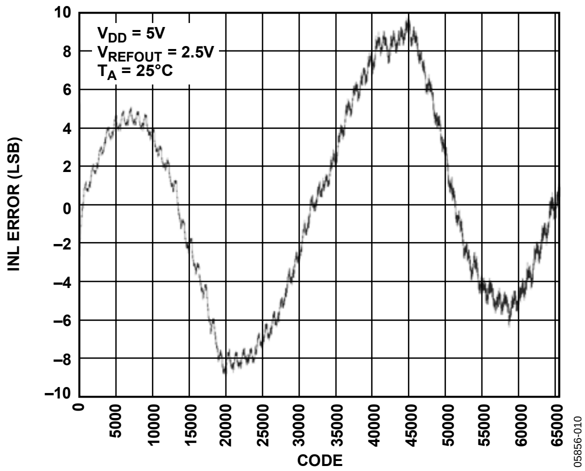


Figure 10. INL AD5667R, 2.5V Internal Reference

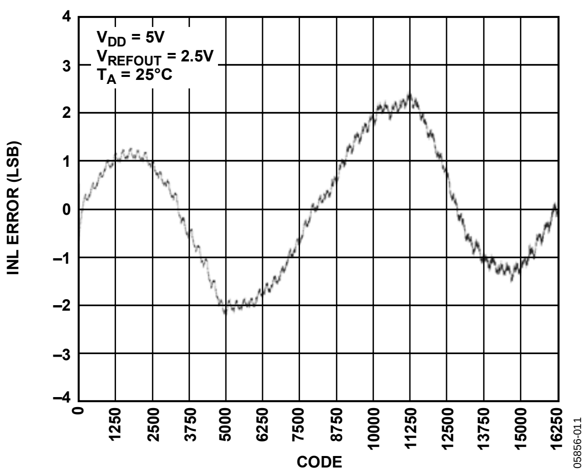


Figure 11. INL AD5647R, 2.5V Internal Reference

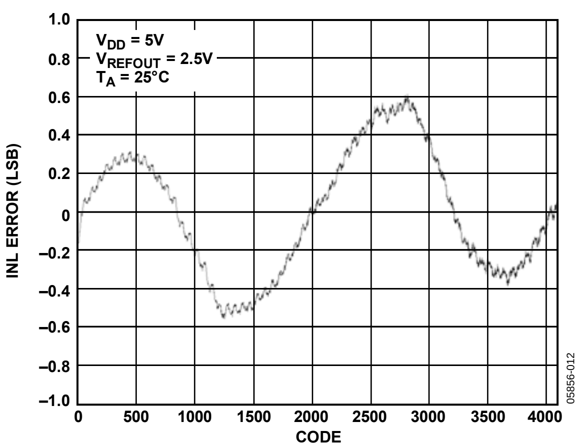


Figure 12. INL AD5627R, 2.V5 Internal Reference

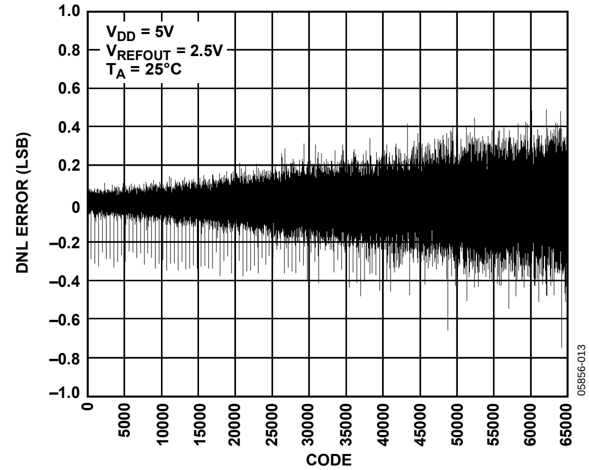


Figure 13. DNL AD5667R, 2.5V Internal Reference

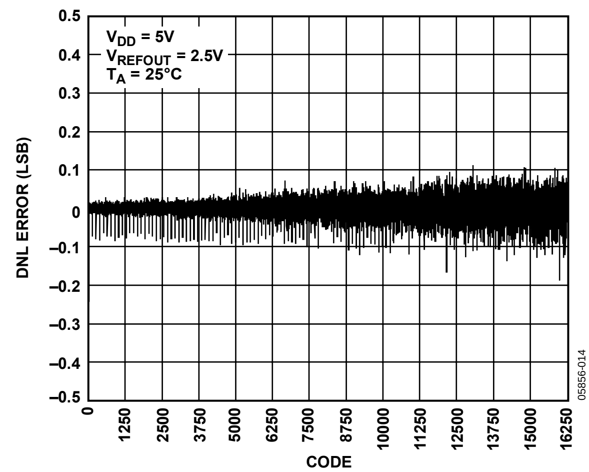


Figure 14. DNL AD5647R, 2.5V Internal Reference

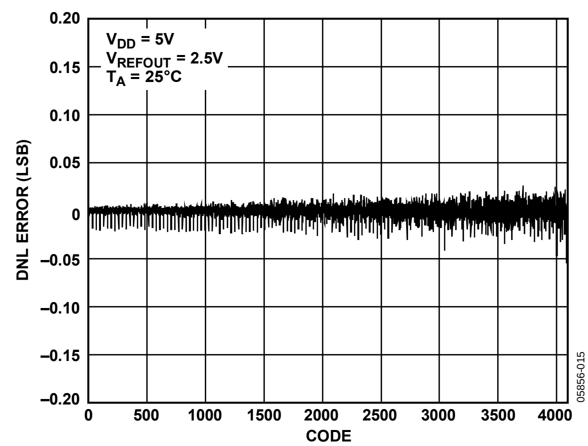


Figure 15. DNL AD5627R, 2.5V Internal Reference

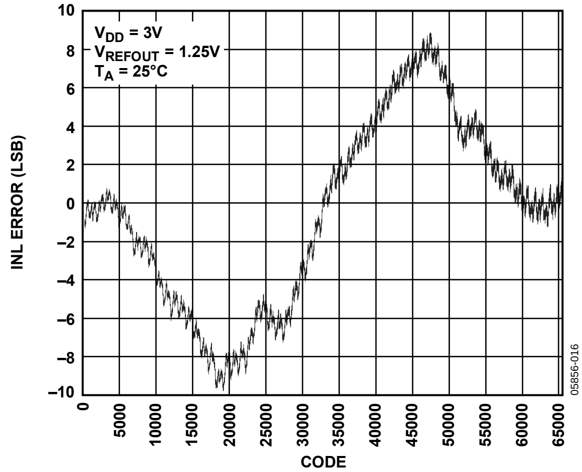


Figure 16. INL AD5667R,1.25V Internal Reference

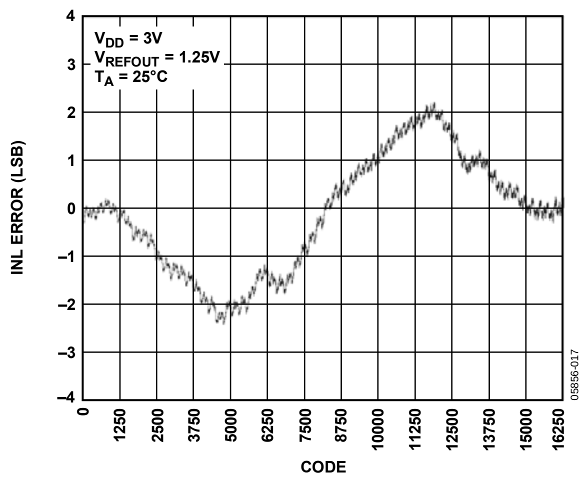


Figure 17. INL AD5647R, 1.25V Internal Reference

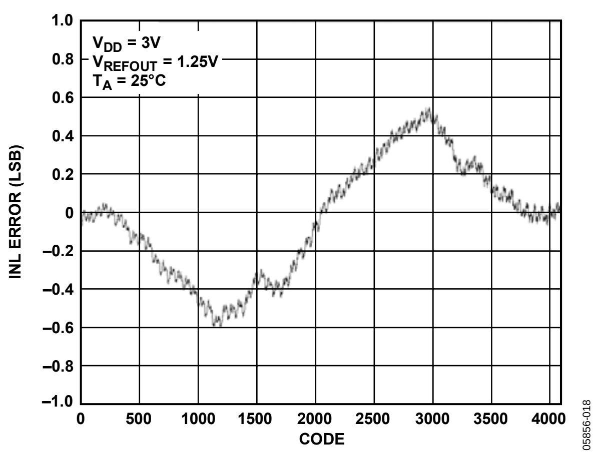


Figure 18. INL AD5627R,1.25V Internal Reference

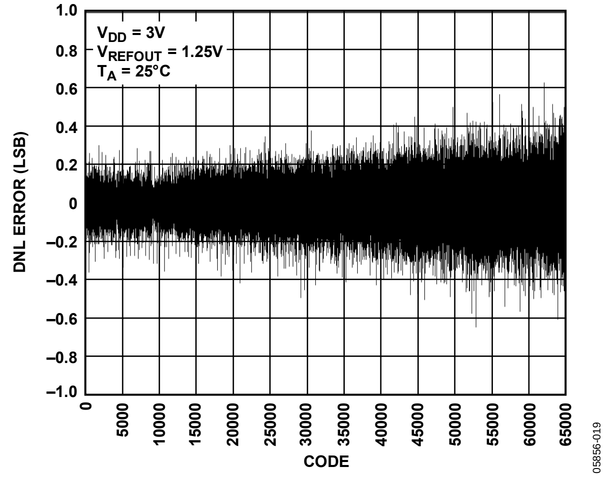


Figure 19. DNL AD5667R,1.25V Internal Reference

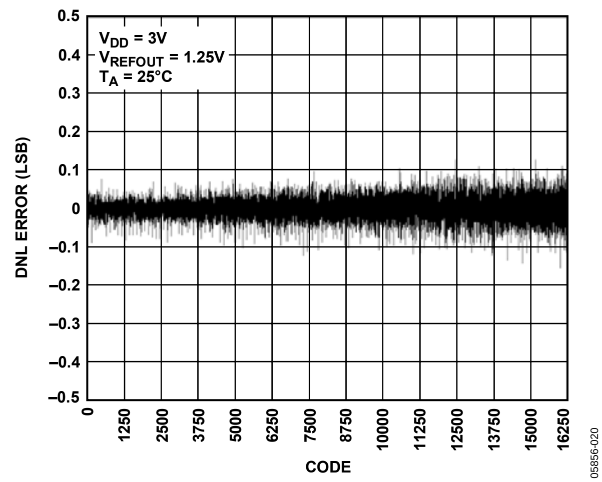


Figure 20. DNL AD5647R,1.25V Internal Reference

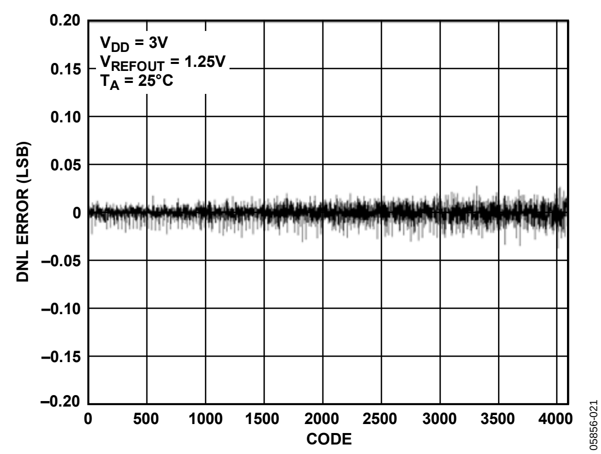


Figure 21. DNL AD5627R, 1.25V Internal Reference

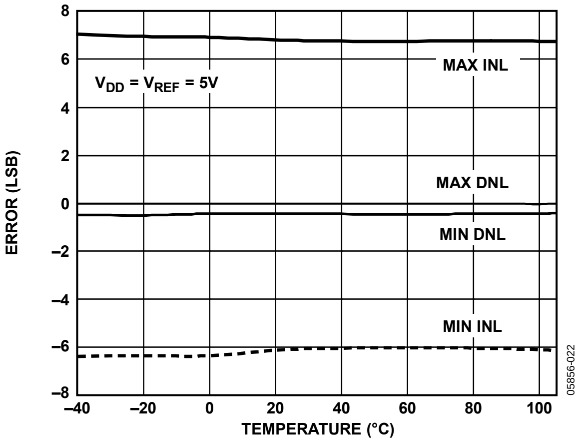


Figure 22. INL Error and DNL Error vs. Temperature

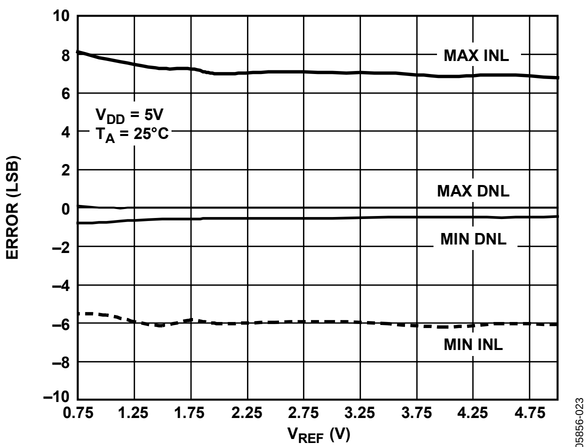


Figure 23. INL and DNL Error vs. V_{REF}

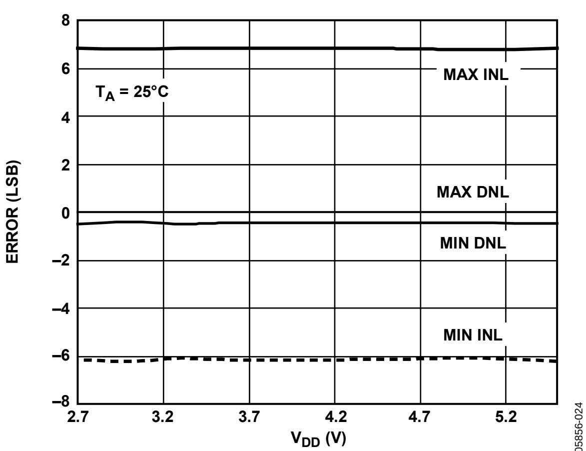


Figure 24. INL and DNL Error vs. Supply

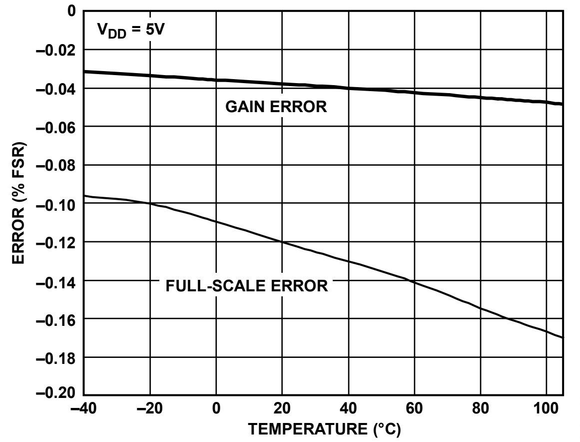


Figure 25. Gain Error and Full-Scale Error vs. Temperature

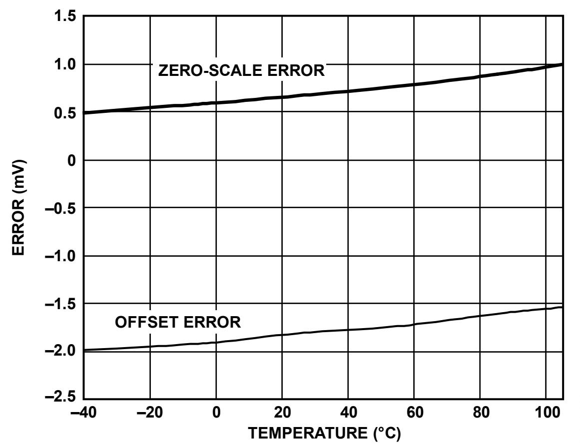


Figure 26. Zero-Scale Error and Offset Error vs. Temperature

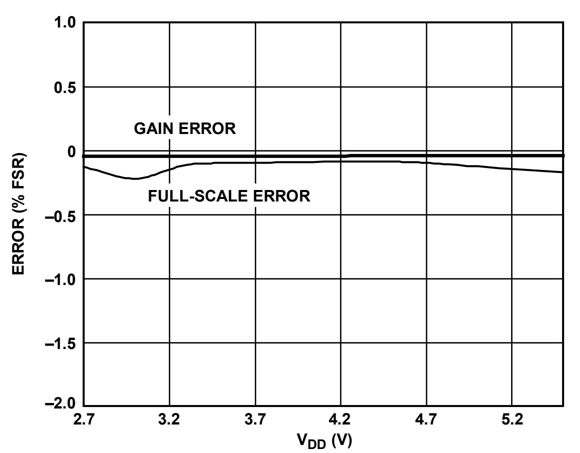


Figure 27. Gain Error and Full-Scale Error vs. Supply

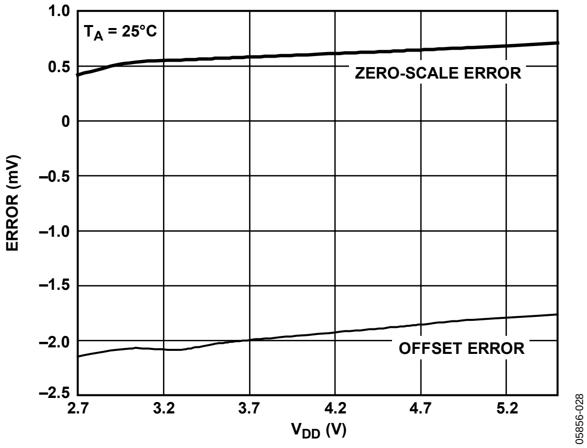


Figure 28. Zero-Scale Error and Offset Error vs. Supply

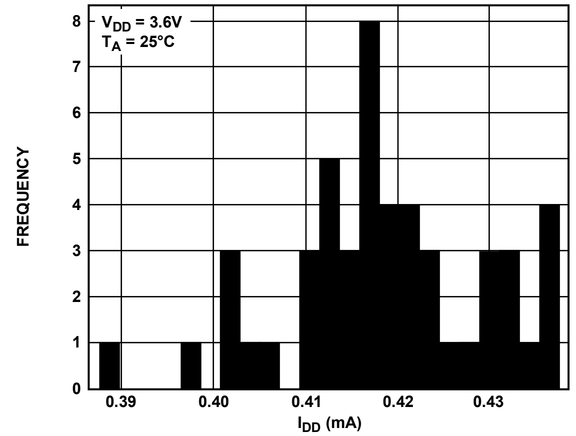


Figure 31. I_{DD} Histogram with External Reference, 3.6 V

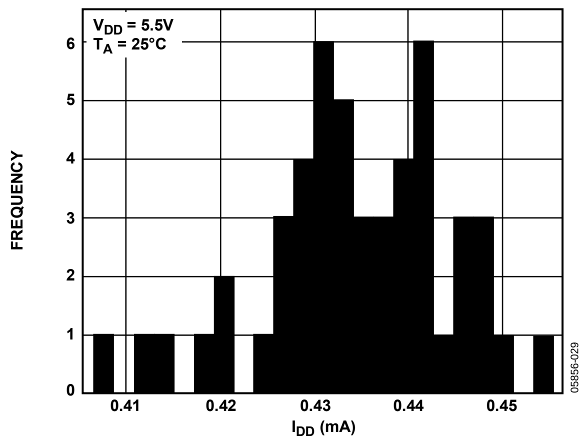


Figure 29. I_{DD} Histogram with External Reference, 5.5 V

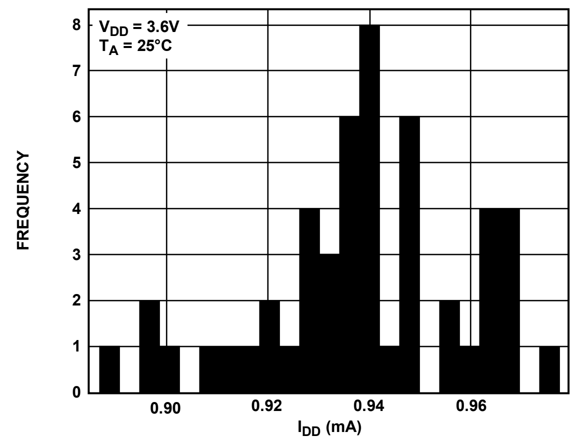


Figure 32. I_{DD} Histogram with Internal Reference, V_{REFOUT} = 1.25 V

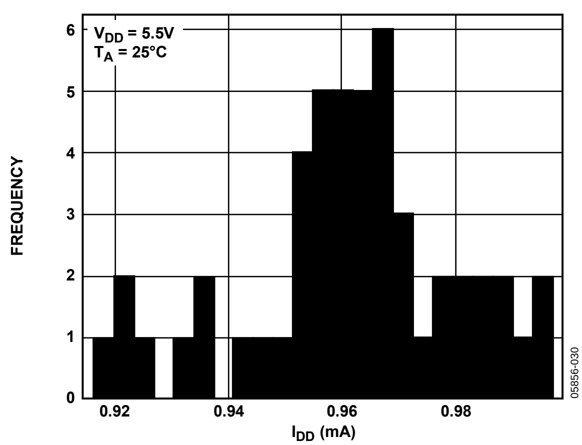


Figure 30. I_{DD} Histogram with Internal Reference, V_{REFOUT} = 2.5 V

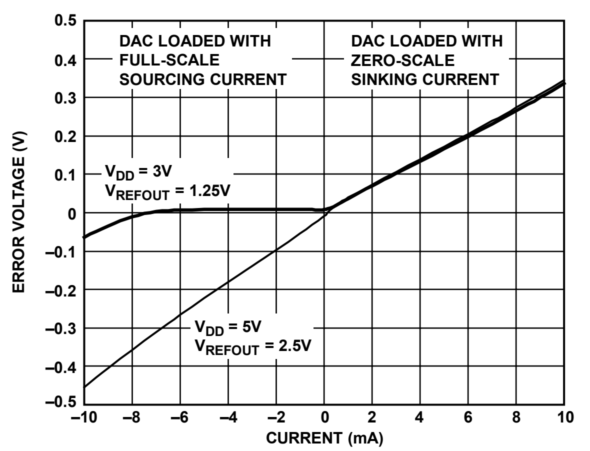


Figure 33. Headroom at Rails vs. Source and Sink

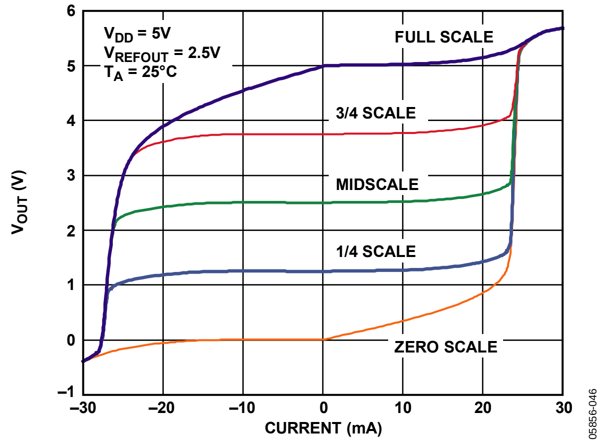


Figure 34. AD56x7R with 2.5V Reference, Source and Sink Capability

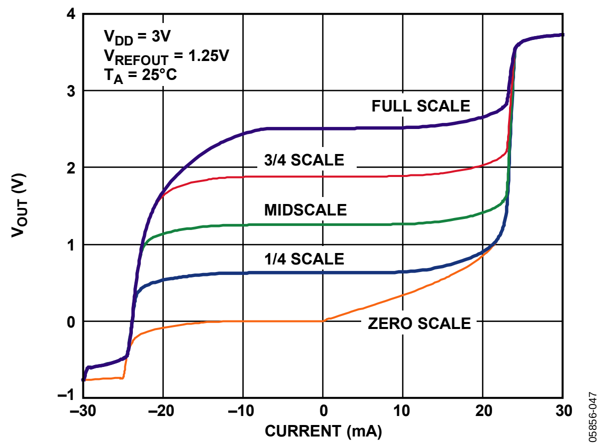


Figure 35. AD56x7 with 1.25V Reference, Source and Sink Capability

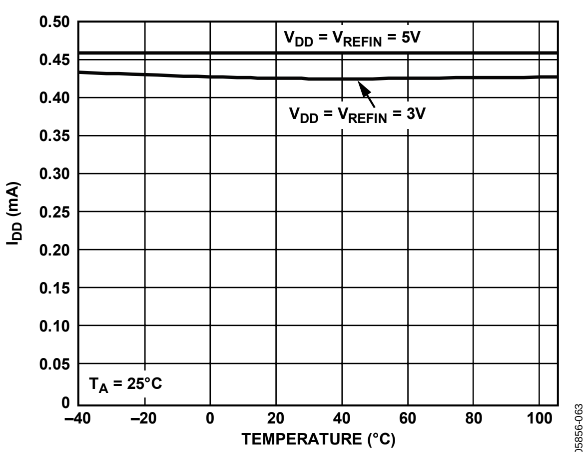


Figure 36. Supply Current vs. Temperature

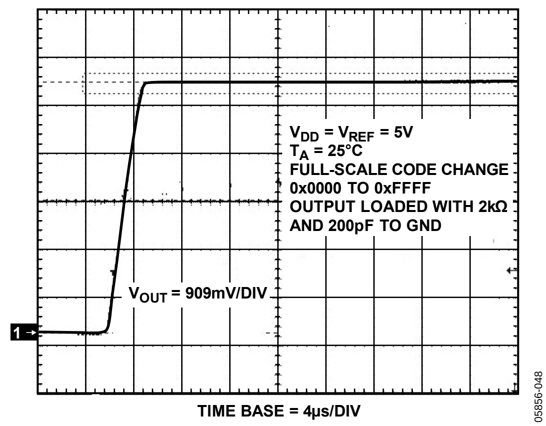


Figure 37. Full-Scale Settling Time, 5 V

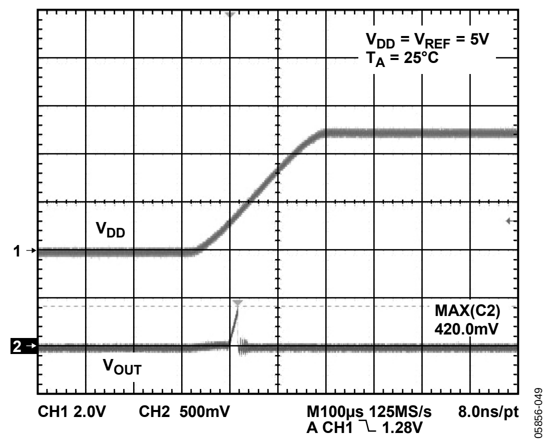


Figure 38. Power-On Reset to 0 V

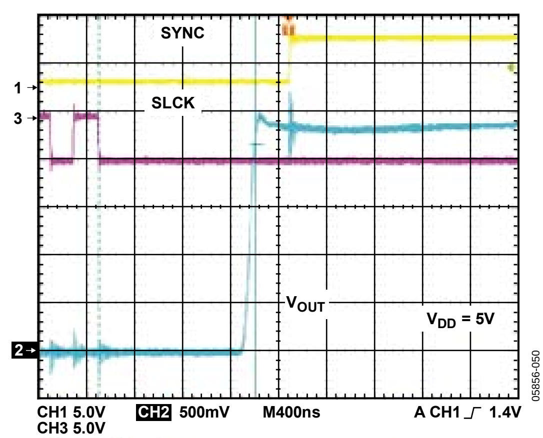


Figure 39. Exiting Power-Down to Midscale

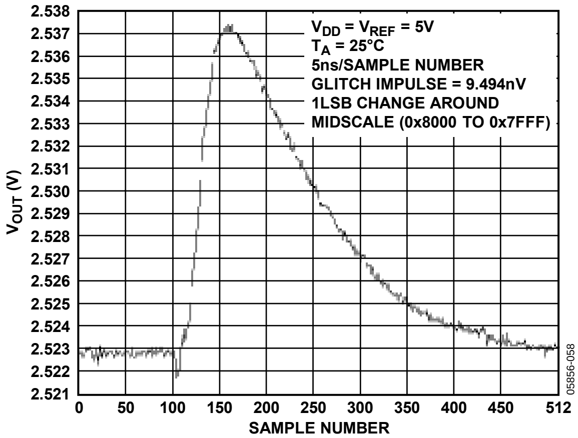


Figure 40. Digital-to-Analog Glitch Impulse (Negative)

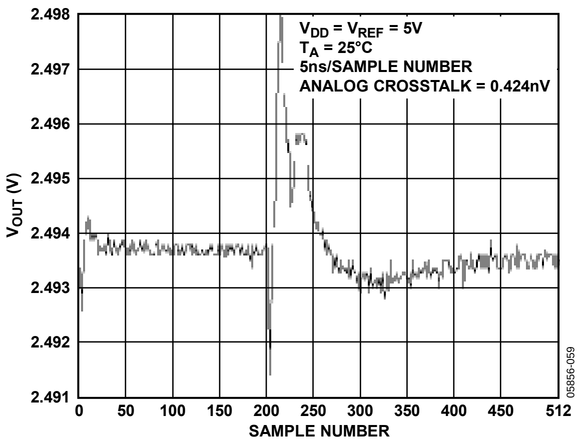


Figure 41. Analog Crosstalk, External Reference

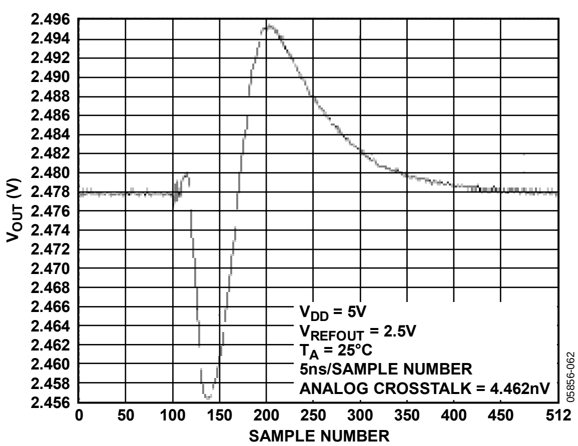


Figure 42. Analog Crosstalk, Internal Reference

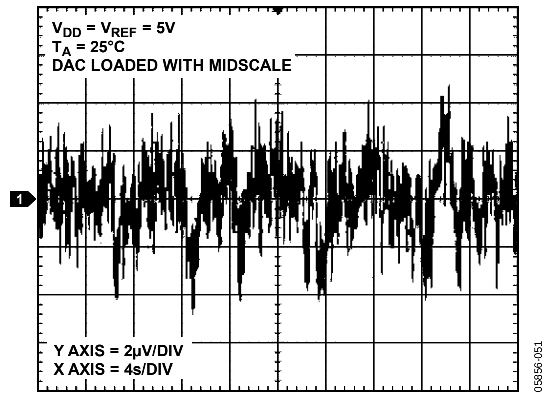


Figure 43. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

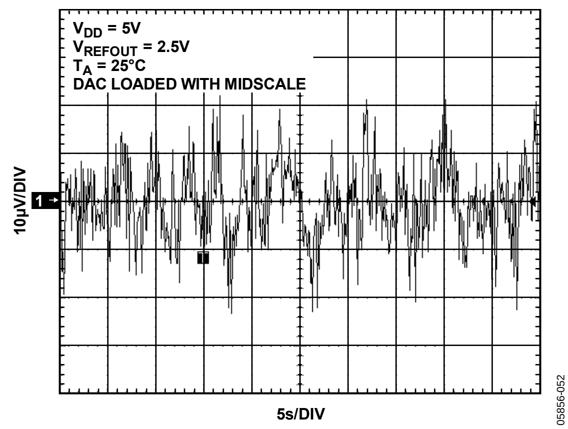


Figure 44. 0.1 Hz to 10 Hz Output Noise Plot, 2.5 V Internal Reference

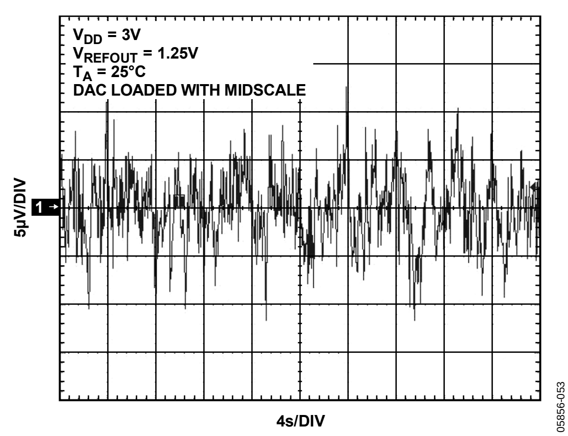


Figure 45. 0.1 Hz to 10 Hz Output Noise Plot,1.25 V Internal Reference

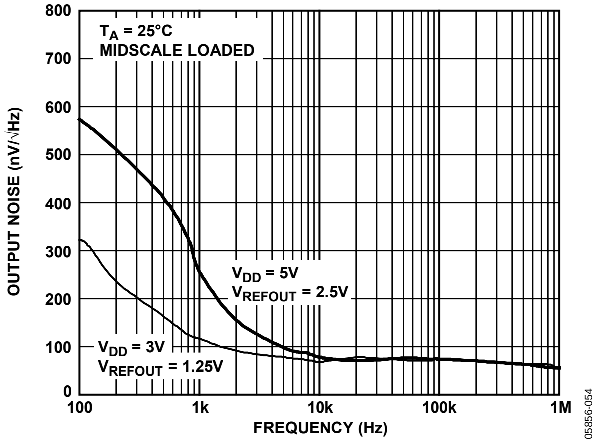


Figure 46. Noise Spectral Density, Internal Reference

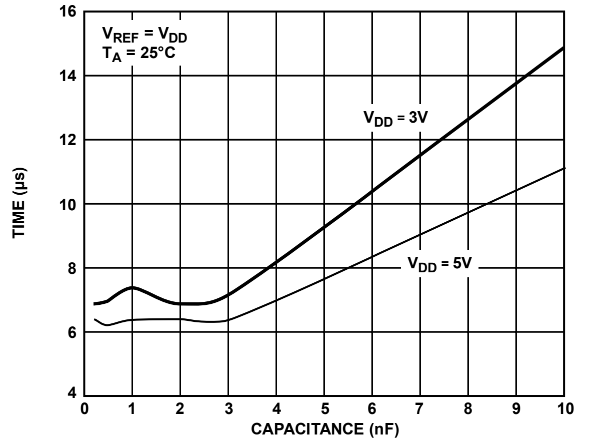


Figure 48. Settling Time vs. Capacitive Load

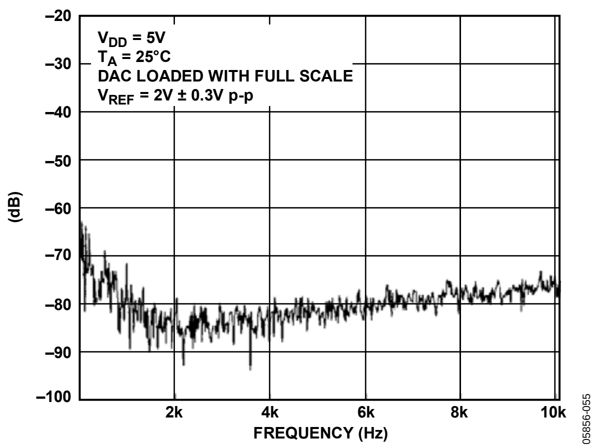


Figure 47. Total Harmonic Distortion

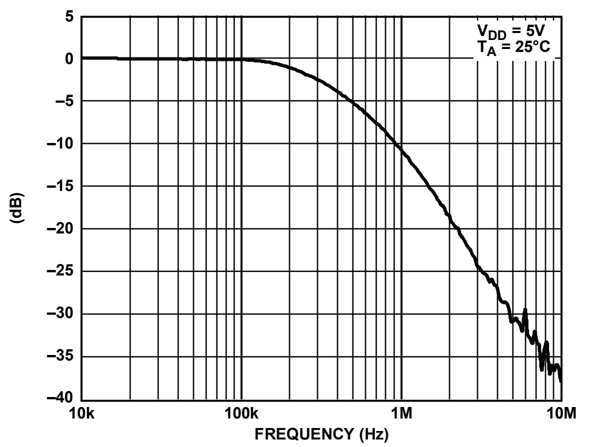


Figure 49. Multiplying Bandwidth

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design.

Zero-Code Error
Zero-code error is a measurement of the output error when zero scale (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5667R because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in mV.

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed in percent of full-scale range.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as % of FSR.

Zero-Code Error Drift
This is a measurement of the change in zero-code error with a change in temperature. It is expressed in μV/°C.

Gain Temperature Coefficient
This is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5667R with code 512 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
This is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the rising edge of the STOP condition.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000) (see Figure).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dB.

Noise Spectral Density
This is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz. A plot of noise spectral density can be seen in Figure .

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in μV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in μV/mA.

Digital Crosstalk
This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk

This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa). Then execute a software LDAC and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk

This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa) using the command write to and update while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)

This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

THEORY OF OPERATION

D/A SECTION

The AD5627R/AD5647R/AD5667R, AD5627/AD5667 DACs are fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Figure 50 shows a block diagram of the DAC architecture.

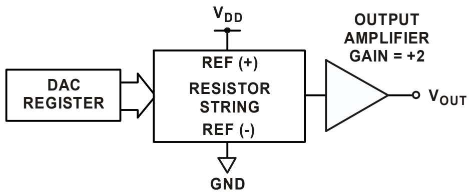


Figure 50. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N}\right)$$

The ideal output voltage when using the internal reference is given by

$$V_{OUT} = 2 \times V_{REFOUT} \times \left(\frac{D}{2^N}\right)$$

where:

D is the decimal equivalent of the binary code that is loaded to the DAC register:

0 to 4095 for AD5627R/AD5627 (12 bit).
0 to 16,383 for AD5647R (14 bit).
0 to 65,535 for AD5667R/AD5667 (16 bit).

N is the DAC resolution.

RESISTOR STRING

The resistor string is shown in Figure 51. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. It can drive a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure and Figure. The slew rate is 1.8 V/µs with a ¼ to ¾ full-scale settling time of 7 µs.

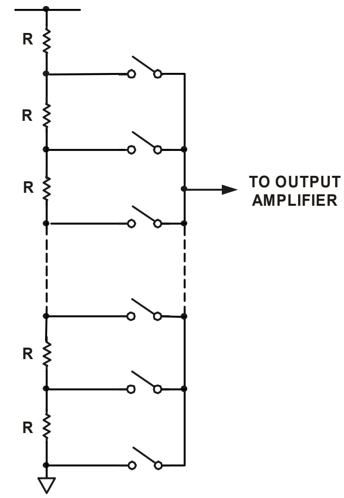


Figure 51. Resistor String

INTERNAL REFERENCE

The AD5627R/AD5647R/AD5667R feature an on-chip reference. Versions without the –R suffix require an external reference. The on-chip reference is off at power-up and is enabled via a write to a control register. See the Internal Reference Setup section for details.

Versions packaged in 10-lead LFCSP package have a 1.25 V reference, giving a full scale output of 2.5 V. These parts can be operated with a V_{DD} supply of 2.7V to 5.5V. Versions packaged in 10-lead MSOP package have a 2.5 V reference, giving a full-scale output of 5 V. Parts are functional with a V_{DD} supply of 2.7V to 5.5V but for V_{DD} supply of less than 5V, the output will be clamped to V_{DD}. See the Ordering Information on the back page for a full list of models. The internal reference associated with each part is available at the V_{REFOUT} pin.
A buffer is required if the reference output is used to drive external loads. When using the internal reference, it is recommended that a 100 nF capacitor is placed between reference output and GND for reference stability.

EXTERNAL REFERENCE

The V_{REFIN} pin on the AD56x7R allows the use of an external reference if the application requires it. The default condition of the on-chip reference is off at power-up. All devices can be operated from a single 2.7 V to 5.5 V supply.

SERIAL INTERFACE

The AD5627R/AD5647R/AD5667R, AD5627/AD5667 have 2-wire I^2C-compatible serial interfaces (refer to *I^2C-Bus Specification*, Version 2.1, January 2000, available from Philips Semiconductor). The AD5627R/AD5647R/AD5667R, AD5627/AD5667 can be connected to an I^2C bus as a slave device, under the control of a master device. See Figure 2 for a timing diagram of a typical write sequence.

The AD5627R/AD5647R/AD5667R, AD5627/AD5667 support standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) data transfer modes. High-speed operation is only available on selected models. See the Ordering Information on the back page for a full list of models. Support is not provided for 10-bit addressing and general call addressing.

The AD5627R/AD5647R/AD5667R, AD5627/AD5667 each have a 7-bit slave address. The two LSBs are set by the state of the ADDR address pin, which determines the state of the A0 and A1 address bits.

The ADDR pin is three-state, and can be set as shown in Table 8 to give three different addresses.

Table 8. ADDR Pin Settings

ADDR PIN CONNECTION	A1	A0
VDD	0	0
No Connection	1	0
GND	1	1

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address. The slave address corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its shift register.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, and then high during the 10th clock pulse to establish a stop condition.

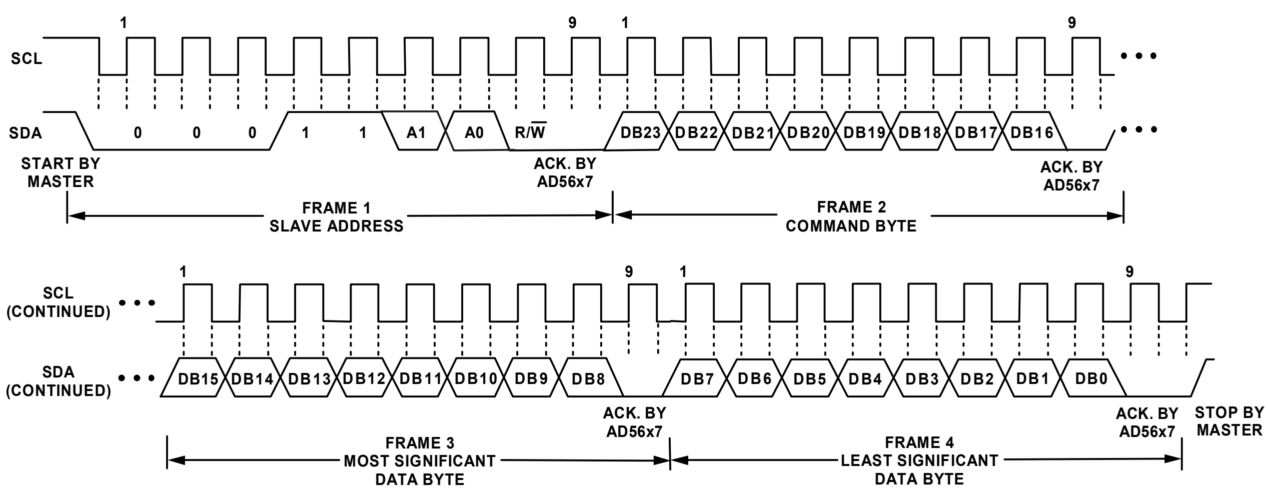


Figure 52. I²C Write Operation

WRITE OPERATION

When writing to the AD5627R/AD5647R/AD5667R, AD5627/AD5667, the user must begin with a start command followed by an address byte (R/W = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The AD5667 requires two bytes of data for the DAC and a command byte that controls various DAC functions. Three bytes of data must therefore written to the DAC, the command byte followed by the most significant data byte and the least significant data byte, as shown in Figure 52. All these data bytes are acknowledged by the AD5627R/AD5647R/AD5667R, AD5627/AD5667. A stop condition follows.

READ OPERATION

When reading data back from the AD5627R/AD5647R/AD5667R, AD5627/AD5667, the user begins with a start command followed by an address byte (R/W = 1), after which the DAC acknowledges that it is prepared to transmit data by pulling SDA low. Two bytes of data are then read from the DAC, which are both acknowledged by the master as shown in Figure 53. A stop condition follows.

Note that the only data that can be read back from the AD56x7 is the contents of the input shift register (see section on Control Register).

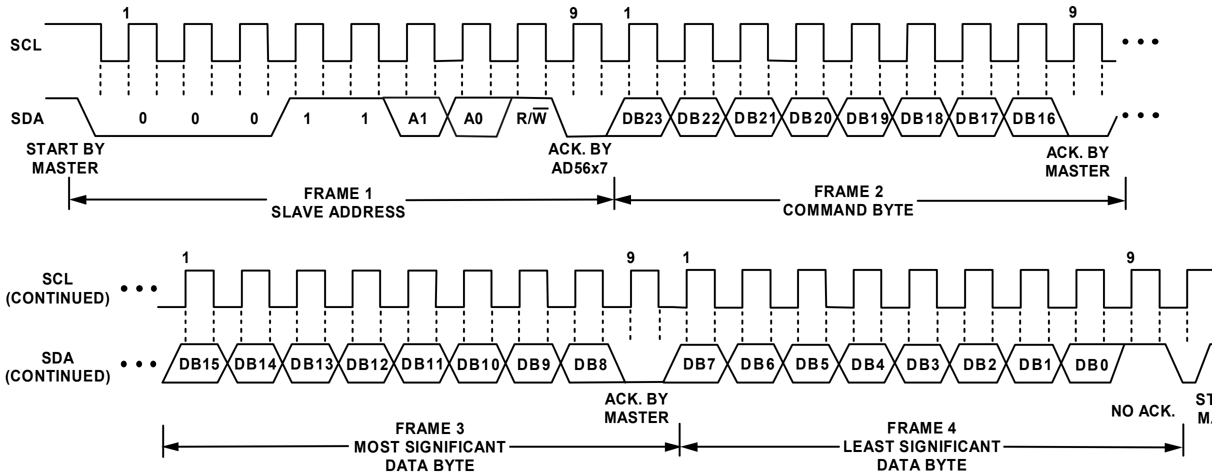


Figure 53. I²C Read Operation

HIGH SPEED MODE

Some models offer high-speed serial communication with a clock frequency of 3.4 MHz. See the Ordering Information on the back page for a full list of models.

High speed mode communication commences after the master addresses all devices connected to the bus with the Master Code 00001XXX to indicate that a high speed mode transfer is to begin. No device connected to the bus is permitted to acknowledge the high speed master code, therefore, the code is followed by a no acknowledge. The master must then issue a repeated start followed by the device address. The selected device then acknowledges its address. All devices continue to operate in high speed mode until the master issues a stop condition. When the stop condition is issued, the devices return to standard/fast mode. The part will also exit high speed mode when $\overline{CLR}$ is activated.

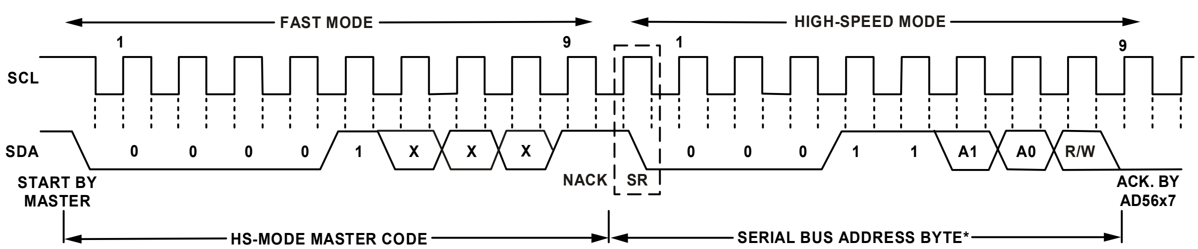


Figure 54. Placing the AD56x7 in High-Speed Mode

MULTIPLE BYTE WRITE

Once an AD56x7 has been addressed, one or more three-byte blocks of command and data can be sent to the device, until a stop condition is received. The device must then be re-addressed. For this type of operation, the "S" bit in the command byte is set to zero.

For some types of application such as waveform generation, it may be required to update a DAC or DACs as fast as possible without changing the command byte. In this case the "S" bit in the initial command byte is set to 1. This sets the command parameters for all subsequent data. Thereafter, multiple two-byte blocks of data high byte and data low byte can be sent, without sending a further command byte, until a stop condition is received.

The "S" bit is only active in the first command byte following the device slave address. Therefore, even if the "S" bit is 0 and three-byte blocks of command and data are being sent, it is not possible to alter the multi-byte mode by changing the "S" bit to 1 "on-the-fly" during any subsequent command byte.

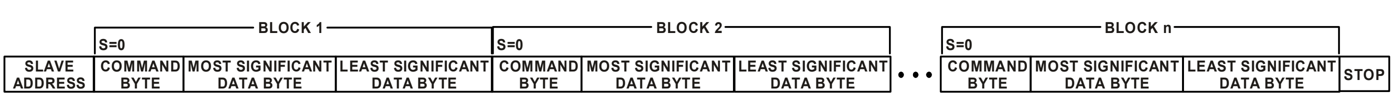


Figure 55. Multiple Block Write With Command Byte in Each Block (S=0)

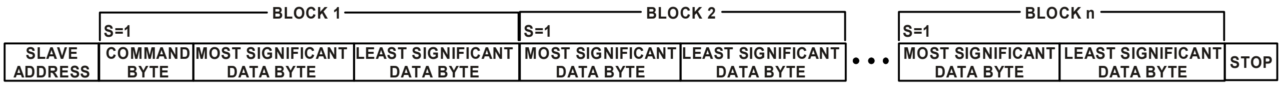


Figure 56. Multiple Block Write With Initial Command Byte Only (S=1)

BROADCAST MODE

In addition to the unique slave address for each device, which is set by the address pin(s), The AD56x7 has a broadcast address to which any AD56x7 will respond, irrespective of the state of the address pin(s). This address is 0001000(Write). Where several AD56x7 devices are connected to a bus, they can all be sent the same data using the broadcast address. The broadcast address only works for write operations. It is not possible to read back data from several devices at the same time, due to bus contention.

INPUT SHIFT REGISTER

The input shift register is 24 bits wide to store the 3 data bytes written to the device of the serial interface. Data written to the device is split into four sections:

- One bit to select multiple byte operation.
- a three bit command that tells the device what operation to perform.
- a three-bit address that tells the device to which DAC or DACs the command applies.
- 16 bits of data, which, depending on the command may be written to a DAC or used to define the parameters of a command operation.

Bit 23 of the input shift register is reserved, and should always be set to 0 when writing to the device.

The command and address are contained in the command byte, the 8 MSBs of the input register. The middle 8 bits are the high byte of the DAC data, while the 8 least significant bits are the low byte of the DAC data or command data. DAC data is left justified, so the two LSBs are unused for the 14 bit AD5647R, and the four LSBs are unused for the 12-bit AD5627R (but they are still used for command data in these devices.

The AD56x7 has seven different commands that can be written to it.

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	S	C2	C1	C0	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RESERVED	BYTE SELECTION	COMMAND			DAC ADDRESS			DAC DATA								DAC OR COMMAND DATA							
COMMAND BYTE								DATA HIGH BYTE								DATA LOW BYTE							

Figure 57. AD5667R/AD5667 Input Shift Register (16-Bit DAC)

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	S	C2	C1	C0	A2	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X
RESERVED	BYTE SELECTION	COMMAND			DAC ADDRESS			DAC DATA								DAC OR COMMAND DATA							
COMMAND BYTE								DATA HIGH BYTE								DATA LOW BYTE							

Figure 58. AD5647R Input Shift Register (14-Bit DAC)

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	S	C2	C1	C0	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
RESERVED	BYTE SELECTION	COMMAND			DAC ADDRESS			DAC DATA								DAC OR COMMAND DATA							
COMMAND BYTE								DATA HIGH BYTE								DATA LOW BYTE							

Figure59. AD5627R/AD5627 Input Shift Register (12-Bit DAC)

WRITE COMMANDS AND LDAC

Table 9.

Command Definition

C2	C1	C0	Command
0	0	0	Write to input register *n*
0	0	1	Update DAC register *n*
0	1	0	Write to input register n, update all (software LDAC)
0	1	1	Write to and update DAC channel *n*
1	0	0	Power up/power down
1	0	1	Reset
1	1	0	LDAC register setup
1	1	1	Internal reference setup (on/off)

Table 9 is the truth table for the command bits. The DAC or DACs on which a command is performed is/are defined by n, which is the DAC address shown in table 10. Some commands required additional data which is defined in the low data byte.

Table 11. DAC Address Command

A2	A1	A0	ADDRESS (*n*)
0	0	0	DAC A
0	0	1	DAC B
1	1	1	Both DACs

The AD5627R/AD5647R/AD5667R, AD5627/AD5667 DACs have double-buffered interfaces consisting of two banks of registers: input registers and DAC registers. The input registers are connected directly to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC registers contain the digital code used by the resistor strings.

The double-buffered interface is useful if the user requires simultaneous updating of all DAC outputs. For example, the user could write to three of the input registers individually and then write to the remaining input register and, updating both DAC registers, the outputs will update simultaneously.

The AD56x7 has a powerful set of commands for writing to and updating the DACs. There is also has a hardware load DAC ($\overline{\text{LDAC}}$) pin. It is important to understand how these commands and the $\overline{\text{LDAC}}$ pin operate and interact with each other, in order to ensure that the desired result is obtained.

The first four commands are used for writing to and updating the DACs.

Command 000 writes to input register n, without updating the DAC registers, where n is the input register defined by the A2 – A0 bits in the command byte. Depending on the value of A2 – A0, this can be any one of the input registers or both input registers, as defined b y the DAC address.

Command 001 does not write to the input registers, but (depending on the value of A2 – A0) updates a DAC register or both DAC registers.

Command 010 writes to input register n, and updates both DAC registers.

Command 011 writes to input register n and updates DAC register n. Since n can be all DACs (A2 – A0 = 111) commands 010 and 011 are equivalent if A2 – A0 = 111.

LDAC SETUP

In addition to the write commands, the LDAC setup command (110) can also determine which DACs are updated at the end of a write operation (this command does not update the DACs when it is implemented). It also affects the operation of the $\overline{\text{LDAC}}$ pin on the 14-pin device (see below). When this command is sent to the device, data bits DB1 and DB0 determine which of DAC registers B and A are updated at the end of write. If a bit is set to 1, the corresponding DAC is updated. Note that, during the LDAC setup command, the DAC address bits A2 – A0 are ignored. It is only DB1 and DB0 that determine which DAC will be updated.

As far as DAC updating is concerned, the write command and the LDAC setup command are combined (OR'd together).

For example, if the LDAC setup command is set to update DACs B, and command 011 is sent to write to and update DAC A, then DAC A will be written to, but DACs A and B will be updated.

R	S	C2	C1	C0	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	X	1	1	0	A2	A1	A0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DACB	DACA
RES	DON'T CARE	COMMAND			DAC ADDRESS (DON'T CARE)			DON'T CARE								DON'T CARE							

DAC SELECT
(0 = LDAC PIN ENABLED)

Figure 60. LDAC Setup Command

$\overline{\text{LDAC}}$ PIN

Updating of the DAC registers may also be controlled by the $\overline{\text{LDAC}}$ pin. This can operate either synchronously or asynchronously. Whenever $\overline{\text{LDAC}}$ is brought low, the DAC registers are updated with the contents of the input registers. If $\overline{\text{LDAC}}$ is held low, update takes place synchronously at the end of every write operation.

Which DAC registers are updated when $\overline{\text{LDAC}}$ is brought low is determined by the LDAC setup command. It is the inverse of those registers that are set to update at the end of write. If one of bits DB1 or DB0 is a 0, then the corresponding DAC is updated when $\overline{\text{LDAC}}$ is taken low. If it is a 1, the DAC is updated at the end of a write operation. This allows one DACs to be updated automatically at the end of write, and the other to be updated asynchronously using the $\overline{\text{LDAC}}$ pin.

If $\overline{\text{LDAC}}$ is permanently held low for synchronous update, then both DACs will be updated irrespective of the DAC address in the write command or the bit settings in the LDAC setup command.

This is because the DAC whose bit is 0 in LDAC setup will be updated due to the $\overline{\text{LDAC}}$ pin being low, and the DACs whose bit is 1 will be updated due to the LDAC setup command.

If DAC update is to be controlled solely by the write and LDAC setup commands, the $\overline{\text{LDAC}}$ pin must be tied high (or use the 10-pin device which does not have this pin). If DAC update is to be controlled solely by the $\overline{\text{LDAC}}$ pin, then use only command 000 and set DB3 to DB0 to 0 in the LDAC setup command.

These parts each contain an extra feature whereby a DAC register is not updated unless its input register has been updated since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD56X7, the DAC register updates only if the input register has changed since the last time the DAC register was updated, thereby removing unnecessary digital crosstalk.

POWER-DOWN MODES

R	S	C2	C1	C0	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	X	1	0	0	A2	A1	A0	X	X	X	X	X	X	X	X	X	X	PD1	PD0	X	X	DACB	DACA
RES	DON'T CARE	COMMAND			DAC ADDRESS (DON'T CARE)			DON'T CARE								DON'T CARE		POWER DOWN MODE		DON'T CARE			

DAC SELECT
(1 = DAC SELECTED)

Figure 61. Power Up/down Command

Command 100 is the power up/down function. The parameters of the power up/down function are programmed by bits DB5 and DB4. This defines the output state of the DAC amplifier, as shown in Table 11. Bits DB3 to DB0 determine to which DAC or DACs the power up/down command is applied. Setting the one of these bits to 1 applies the power up/down state defined by DB5 and DB4 to the corresponding DAC. If a bit is 0, the state of the DAC is unchanged.

In power-down mode, the amplifier is disconnected from the output pin, and the output pin is either open-circuit or connected ground via a 10kΩ or 100kΩ resistor, depending on the setting of DB5 and DB4.

Table 11. Modes of Operation for the AD5627R/AD5647R/AD5667R, AD5627/AD5667

DB5	DB4	Operating Mode
0	0	Normal operation
		Power-down modes
0	1	1 kΩ pulldown to GND
1	0	100 kΩ pulldown to GND
1	1	Three-state, high impedance

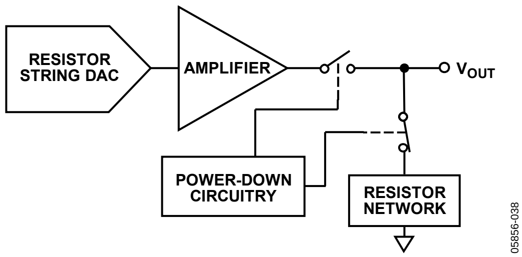


Figure 62. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string, and other associated linear circuitry are shutdown when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 4 µs for V_{DD} = 5 V and for V_{DD} = 3 V. Figure 61 shows the format of the power up/down command. Note that, during the power up/down command, the DAC address bits A2 – A0 are ignored.

POWER-ON-RESET AND SOFTWARE RESET

The AD56x7 contains a power-on reset circuit that controls the output voltage during power-up. The device powers up to 0V and the output remains powered up at this level until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. Any events on $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ during power-on reset are ignored.

There is also a software reset function. Command 101 is the software reset command. The software reset command contains two reset modes that are software programmable by setting bit DB0 in the input shift register.

Table 12 shows how the state of the bit corresponds to the software reset modes of operation of the devices. Figure 64 shows the contents of the input shift register during the software reset mode of operation.

Table 12. Software Reset Modes for the AD5627R/AD5647R/AD5667R, AD5627/AD5667

DB0	Registers reset to zero
0	DAC register Input shift register
1 (Power-On Reset)	DAC register Input shift register LDAC register Power-down register Internal reference setup register

CLEAR PIN ($\overline{\text{CLR}}$)

The AD56x7 has an asynchronous clear input. The $\overline{\text{CLR}}$ input is falling edge sensitive. While $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, zero scale is loaded to all input and DAC registers. This clears the output to 0 V. The part exits clear code mode on the 24th falling edge of the next write to the part. If $\overline{\text{CLR}}$ is activated during a write sequence, the write is aborted. If $\overline{\text{CLR}}$ is activated during high speed mode the part will exit high speed mode to fast mode.

X	S	C2	C1	C0	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	X	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	RST
RES	DON'T CARE	COMMAND			DAC ADDRESS (DON'T CARE)			DON'T CARE								DON'T CARE							RESET MODE

Figure 63. Reset Command

INTERNAL REFERENCE SETUP (-R VERSIONS)

The on-chip reference is off at power-up by default. It can be turned on by sending the reference setup command (111) and setting DB0 in the input shift register. Table 14 shows how the state of the bit corresponds to the mode of operation.

Table 14. Reference Setup Command

(DB0)	Action
0	Internal reference off (default)
1	Internal reference on

R	S	C2	C1	C0	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	X	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	REF
RES	DON'T CARE	COMMAND			DAC ADDRESS (DON'T CARE)			DON'T CARE								DON'T CARE							REF. MODE

Figure 64. Reference Setup Command

APPLICATIONS

USING A REFERENCE AS A POWER SUPPLY FOR THE AD5627R/AD5647R/AD5667R, AD5627/AD5667

Because the supply current required by the AD5627R/AD5647R/AD5667R, AD5627/AD5667is extremely low, an alternative option is to use a voltage reference to supply the required voltage to the part (see Figure). This is especially useful if the power supply is quite noisy, or if the system supply voltages are at some value other than 5 V or 3 V, for example, 15 V. The voltage reference outputs a steady supply voltage for the AD5627R/AD5647R/AD5667R, AD5627/AD5667. If the low dropout REF195 is used, it must supply 450 μA of current to the AD5627R/AD5647R/AD5667R, AD5627/AD5667 with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is

450 μA + (5 V/5 kΩ) = 1.45 mA

The load regulation of the REF195 is typically 2 ppm/mA, resulting in a 2.9 ppm (14.5 μV) error for the 1.45 mA current drawn from it. This corresponds to a 0.191 LSB error.

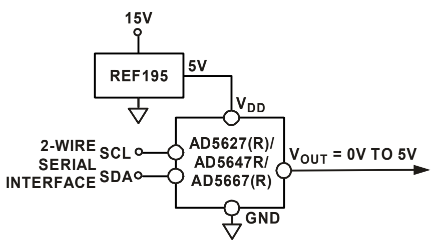


Figure 65. REF195 as Power Supply to the AD5627R/AD5647R/AD5667R, AD5627/AD5667

BIPOLAR OPERATION USING THE AD5627R/AD5647R/AD5667R, AD5627/AD5667

The AD5627R/AD5647R/AD5667R, AD5627/AD5667 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 67. The circuit gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{65{,}536} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 to 65535). With V_{DD} = 5 V, $R1 = R2$ = 10 kΩ,

$$V_O = \left(\frac{10 \times D}{65{,}536} \right) - 5\text{ V}$$

This is an output voltage range of ±5 V, with 0x0000 corresponding to a −5 V output, and 0xFFFF corresponding to a +5 V output.

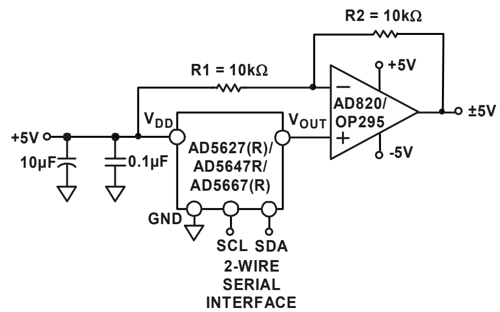


Figure 66. Bipolar Operation with the AD5627R/AD5647R/AD5667R, AD5627/AD5667

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5627R/AD5647R/AD5667R, AD5627/AD5667 should have separate analog and digital sections, each having its own area of the board. If the AD5627R/AD5647R/AD5667R, AD5627/AD5667 are in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5627R/AD5647R/AD5667R, AD5627/AD5667.

The power supply to the AD5627R/AD5647R/AD5667R, AD5627/AD5667 should be bypassed with 10 μF and 0.1 μF capacitors. The capacitors should be located as close as possible to the device, with the 0.1 μF capacitor ideally right up against the device. The 10 μF capacitor is the tantalum bead type. It is important that the 0.1 μF capacitor have low effective series resistance (ESR) and effective series inductance (ESI), for example, common ceramic types of capacitors. This 0.1 μF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and to reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS

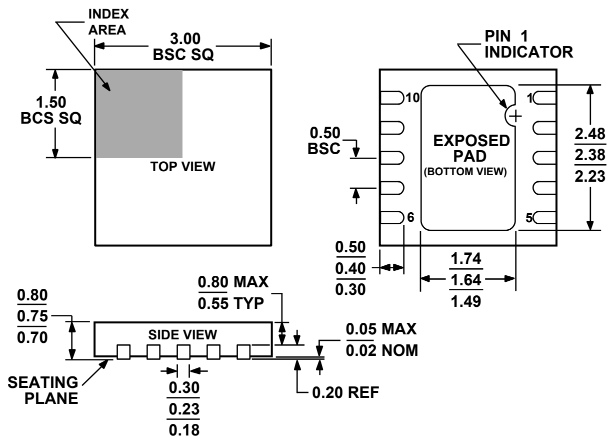


Figure 67. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm x 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

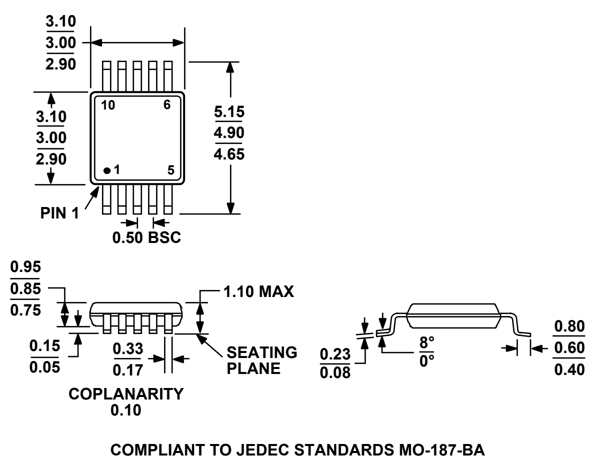


Figure68. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Accuracy	On-Chip Reference	Max I²C Speed	Package Description	Package Option	Branding
AD5627BCPZ-250RL7[1]	−40°C to +105°C	±1 LSB INL	None	400 kHz	10-Lead LFCSP_WD	CP-10 -9	DA1
AD5627BCPZ-REEL7[1]	−40°C to +105°C	±1 LSB INL	None	400 kHz	10-Lead LFCSP_WD	CP-10-9	DA1
AD5627BRMZ[1]	−40°C to +105°C	±1 LSB INL	None	400 kHz	10-Lead MSOP	RM-10	DA1
AD5627BRMZ-REEL7[1]	−40°C to +105°C	±1 LSB INL	None	400 kHz	10-Lead MSOP	RM-10	DA1
AD5627RBCPZ-250RL7[1]	−40°C to +105°C	±1 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	CP-10-9	D9J
AD5627RBCPZ-REEL7[1]	−40°C to +105°C	±1 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	CP-10-9	D9J
AD5627RBRMZ-1[1]	−40°C to +105°C	±1 LSB INL	2.5 V	400 kHz	10-Lead MSOP	RM-10	DA1
AD5627RBRMZ-1REEL7[1]	−40°C to +105°C	±1 LSB INL	2.5 V	400 kHz	10-Lead MSOP	RM-10	DA1
AD5627RBRMZ-2[1]	−40°C to +105°C	±1 LSB INL	2.5 V	3.4 MHz	10-Lead MSOP	RM-10	DA1
AD5627RBRMZ-2REEL7[1]	−40°C to +105°C	±1 LSB INL	2.5 V	3.4 MHz	10-Lead MSOP	RM-10	DA1
AD5647RBCPZ-250RL7[1]	−40°C to +105°C	±4 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	RU-14	D9G
AD5647RBCPZ-REEL7[1]	−40°C to +105°C	±4 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	RU-14	D9G
AD5647RBRMZ[1]	−40°C to +105°C	±4 LSB INL	2.5 V	400 kHz	10-Lead MSOP	RM-10	D9G
AD5647RBRMZ-REEL7[1]	−40°C to +105°C	±4 LSB INL	2.5 V	400 kHz	10-Lead MSOP	RM-10	D9G
AD5667BCPZ-250RL7[1]	−40°C to +105°C	±16 LSB INL	None	400 kHz	10-Lead LFCSP_WD	CP-10-9	D9Z
AD5667BCPZ-REEL7[1]	−40°C to +105°C	±16 LSB INL	None	400 kHz	10-Lead LFCSP_WD	CP-10-9	D9Z
AD5667BRMZ[1]	−40°C to +105°C	±16 LSB INL	None	400 kHz	10-Lead MSOP	RM-10	D9Z
AD5667BRMZ-REEL7[1]	−40°C to +105°C	±16 LSB INL	None	400 kHz	10-Lead MSOP	RM-10	D9Z
AD5667RBCPZ-250RL7[1]	−40°C to +105°C	±16 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	CP-10-9	D8X
AD5667RBCPZ-REEL7[1]	−40°C to +105°C	±16 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	CP-10-9	D8X
AD5667RBRMZ-1[1]	−40°C to +105°C	±16 LSB INL	2.5 V	400 kHz	10-Lead MSOP	RM-10	DA5
AD5667RBRMZ-1REEL7[1]	−40°C to +105°C	±16 LSB INL	2.5 V	400 kHz	10-Lead MSOP	RM-10	DA5
AD5667-RBRMZ-2[1]	−40°C to +105°C	±16 LSB INL	2.5 V	3.4 MHz	10-Lead MSOP	RM-10	DA5
AD5667RBRMZ-2REEL7[1]	−40°C to +105°C	±16 LSB INL	2.5 V	3.4 MHz	10-Lead MSOP	RM-10	DA5

[1] Z = Pb-free part.

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