



512MB – 2x32Mx64 DDR SDRAM UNBUFFERED

FEATURES

- DDR200, DDR266, DDR333 and DDR400
 - JEDEC design specifications
- Double-data-rate architecture
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh
- Serial presence detect
- Dual Rank
- Power supply: 2.5V $\pm$ 0.20V
- 200 pin SO-DIMM package
 - Package height options
 - D4: 35.5mm (1.38")

NOTE: Consult factory for availability of:

- RoHS compliant products
- Vendor source control options
- Industrial temperature option

DESCRIPTION

The W3EG6467S is a 2x32Mx64 Double Data Rate SDRAM memory module based on 512Mb DDR SDRAM component. The module consists of eight 32Mx16 DDR SDRAMs in 66 pin TSOP packages mounted on a 200 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data 1/0 transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

OPERATING FREQUENCIES

	DDR400@CL=3	DDR333@CL=2.5	DDR266@CL=2	DDR266@CL=2.5	DDR200@CL=2
Clock Speed	200MHz	166MHz	133MHz	133MHz	100MHz
CL-tRCD-tRP	3-3-3	2.5-3-3	2-2-2	2.5-3-3	2-2-2



PIN CONFIGURATION

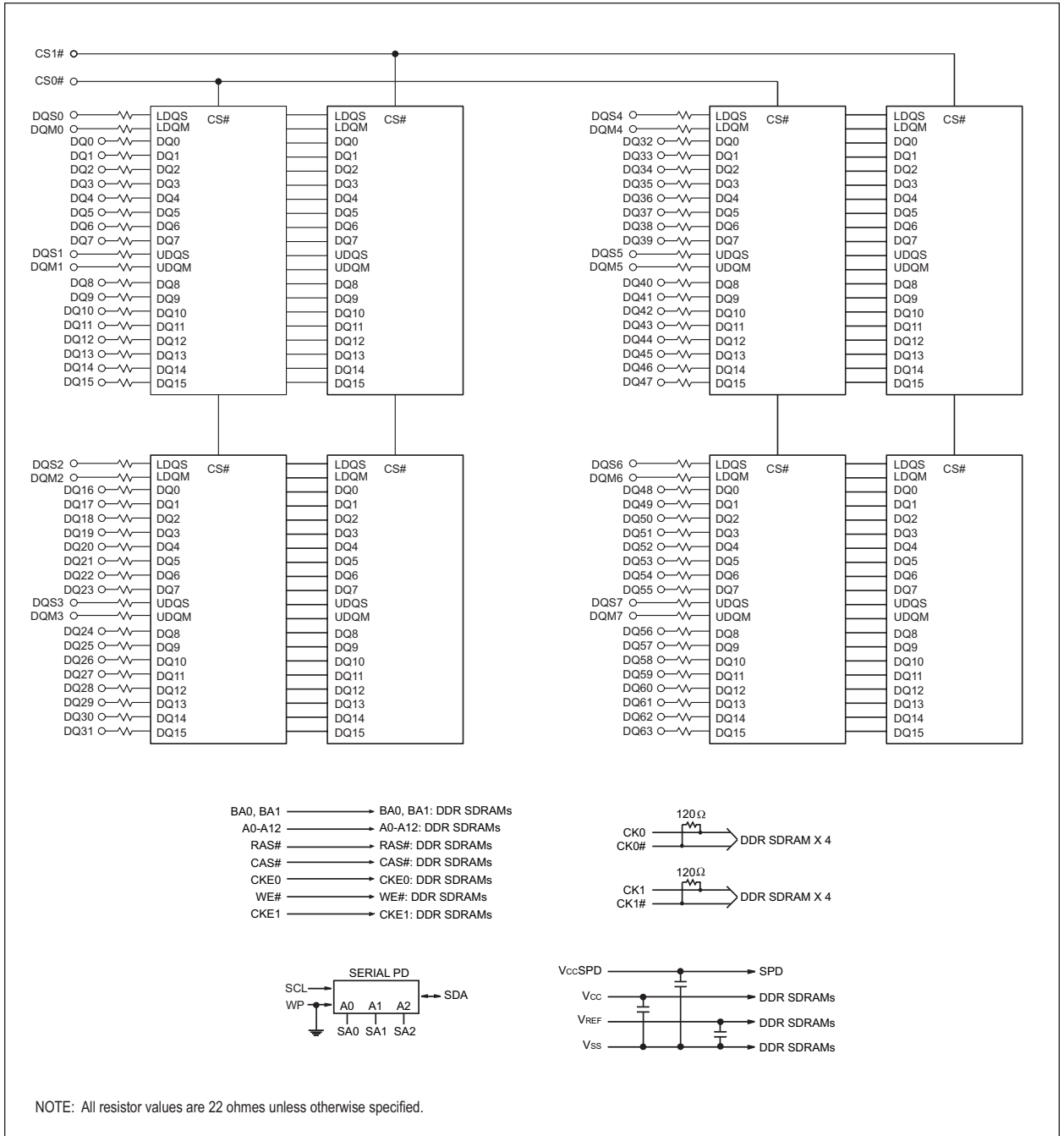
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V _{REF}	51	V _{SS}	101	A9	151	DQ42
2	V _{REF}	52	V _{SS}	102	A8	152	DQ46
3	V _{SS}	53	DQ19	103	V _{SS}	153	DQ43
4	V _{SS}	54	DQ23	104	V _{SS}	154	DQ47
5	DQ0	55	DQ24	105	A7	155	V _{CC}
6	DQ4	56	DQ28	106	A6	156	V _{CC}
7	DQ1	57	V _{CC}	107	A5	157	V _{CC}
8	DQ5	58	V _{CC}	108	A4	158	CK1#
9	V _{CC}	59	DQ25	109	A3	159	V _{SS}
10	V _{CC}	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	V _{SS}
12	DQM0	62	DQM3	112	A0	162	V _{SS}
13	DQ2	63	V _{SS}	113	V _{CC}	163	DQ48
14	DQ6	64	V _{SS}	114	V _{CC}	164	DQ52
15	V _{SS}	65	DQ26	115	A10/AP	165	DQ49
16	V _{SS}	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	V _{CC}
18	DQ7	68	DQ31	118	RAS#	168	V _{CC}
19	DQ8	69	V _{CC}	119	WE#	169	DQS6
20	DQ12	70	V _{CC}	120	CAS#	170	DQM6
21	V _{CC}	71	NC	121	CS0	171	DQ50
22	V _{CC}	72	NC	122	CS1	172	DQ54
23	DQ9	73	NC	123	NC	173	V _{SS}
24	DQ13	74	NC	124	NC	174	V _{SS}
25	DQS1	75	V _{SS}	125	V _{SS}	175	DQ51
26	DQM1	76	V _{SS}	126	V _{SS}	176	DQ55
27	V _{SS}	77	NC	127	DQ32	177	DQ56
28	V _{SS}	78	NC	128	DQ36	178	DQ60
29	DQ10	79	NC	129	DQ33	179	V _{CC}
30	DQ14	80	NC	130	DQ37	180	V _{CC}
31	DQ11	81	V _{CC}	131	V _{CC}	181	DQ57
32	DQ15	82	V _{CC}	132	V _{CC}	182	DQ61
33	V _{CC}	83	NC	133	DQS4	183	DQS7
34	V _{CC}	84	NC	134	DQM4	184	DQM7
35	CK0	85	NC	135	DQ34	185	V _{SS}
36	V _{CC}	86	NC	136	DQ38	186	V _{SS}
37	CK0#	87	V _{SS}	137	V _{SS}	187	DQ58
38	V _{SS}	88	V _{SS}	138	V _{SS}	188	DQ62
39	V _{SS}	89	NC	139	DQ35	189	DQ59
40	V _{SS}	90	V _{SS}	140	DQ39	190	DQ63
41	DQ16	91	NC	141	DQ40	191	V _{CC}
42	DQ20	92	V _{CC}	142	DQ44	192	V _{CC}
43	DQ17	93	V _{CC}	143	V _{CC}	193	SDA
44	DQ21	94	V _{CC}	144	V _{CC}	194	SA0
45	V _{CC}	95	CKE1	145	DQ41	195	SCL
46	V _{CC}	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	V _{CC} SPD
48	DQM2	98	NC	148	DQM5	198	SA2
49	DQ18	99	A12	149	V _{SS}	199	V _{CC} ID
50	DQ22	100	A11	150	V _{SS}	200	NC

PIN NAMES

AO -A12	Address input (Multiplexed)
BA0-BA1	Bank SelectAddress
DQ0-DQ63	Data Input/Output
DQSO-DQS7	Data Strobe Input/Output
CK0, CK1	Clock Input
CK0#, CK1#	Clock input
CKE0, CKE1	Clock Enable input
CS0#, CS1#	Chip select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-DQM7	Data-In Mask
V _{CC}	Power Supply
V _{CC} Q	Power Supply for DQS
V _{SS}	Ground
V _{REF}	Power Supply for Reference
V _{CC} SPD	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
V _{CC} ID	V _{CC} Identification Flag
NC	No Connect



FUNCTIONAL BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to 3.6	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC} , V _{CCQ}	-1.0 to 3.6	V
Storage Temperature	T _{STG}	-55 to +150	°C
Power Dissipation	P _D	8	W
Short Circuit Current	I _{OS}	50	mA

Note:

- Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
- Functional operation should be restricted to recommended operating condition.
- Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC CHARACTERISTICS

 $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, V_{CC} = 2.5V $\pm$ 0.2V

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	2.3	2.7	V
Supply Voltage	V _{CCQ}	2.3	2.7	V
Reference Voltage	V _{REF}	V _{CCQ} /2 - 50mV	V _{CCQ} /2 + 50mV	V
Termination Voltage	V _{TT}	V _{REF} - 0.04	V _{REF} + 0.04	V
Input High Voltage	V _{IH}	V _{REF} + 0.15	V _{CCQ} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	V _{REF} - 0.15	V
Output High Voltage	V _{OH}	V _{TT} + 0.76	—	V
Output Low Voltage	V _{OL}	—	V _{TT} - 0.76	V

CAPACITANCE

T_A = 25°C, f = 1MHz, V_{CC} = 2.5V $\pm$ 0.2V, V_{REF} = 1.4V $\pm$ 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C _{IN1}	50	pF
Input Capacitance (RAS#, CAS#, WE#)	C _{IN2}	50	pF
Input Capacitance (CKE0, CKE1)	C _{IN3}	26	pF
Input Capacitance (CK0,CK0#, CK1, CK1#)	C _{IN4}	5.5	pF
Input Capacitance (CS0#, CS1#)	C _{IN5}	26	pF
Input Capacitance (DQM0-DQM8)	C _{IN6}	13	pF
Input Capacitance (BA0-BA1)	C _{IN7}	50	pF
Data input/output capacitance (DQ0-DQ63)(DQS)	C _{OUT}	13	pF



I_{DD} SPECIFICATIONS AND TEST CONDITIONS

0°C ≤ T_A ≤ 70°C, V_{CCQ} = 2.5V ±0.2V, V_{CC} = 2.5V ±0.2V

Parameter	Symbol	Conditions	DDR403 @CL=3 Max	DDR333 @CL=2.5 Max	DDR266 @CL=2, 2.5 Max	DDR200 @CL=2 Max	Units
Operating Current	I _{DD0}	One device bank; Active - Precharge; t _{RC} =t _{RC} (MIN); t _{CK} =t _{CK} (MIN); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.		1600	1440	1360	mA
Operating Current	I _{DD1}	One device bank; Active-Read-Precharge; Burst = 2; t _{RC} =t _{RC} (MIN);t _{CK} =t _{CK} (MIN); I _{out} = 0mA; Address and control inputs changing once per clock cycle.		1800	1640	1560	mA
Precharge Power- Down Standby Current	I _{DD2P}	All device banks idle; Power- down mode; t _{CK} =t _{CK} (MIN); CKE=(low)		48	48	48	mA
Idle Standby Current	I _{DD2F}	CS# = High; All device banks idle; t _{CK} =t _{CK} (MIN); CKE = high; Address and other control inputs changing once per clock cycle. V _{in} = V _{ref} for DQ, DQS and DM.		400	320	320	mA
Active Power-Down Standby Current	I _{DD3P}	One device bank active; Power-down mode; t _{CK} (MIN); CKE=(low)		560	480	480	mA
Active Standby Current	I _{DD3N}	CS# = High; CKE = High; One device bank; Active-Precharge; t _{RC} =t _{RAS} (MAX); t _{CK} =t _{CK} (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.		880	720	720	mA
Operating Current	I _{DD4R}	Burst = 2; Reads; Continuous burst; One device bank active;Address and control inputs changing once per clock cycle; t _{CK} =t _{CK} (MIN); I _{out} = 0mA.		2160	1840	1840	mA
Operating Current	I _{DD4W}	Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} =t _{CK} (MIN); DQ,DM and DQS inputs changing twice per clock cycle.		2160	1800	1800	mA
Auto Refresh Current	I _{DD5}	t _{RC} =t _{RC} (MIN)		2240	2000	2000	mA
Self Refresh Current	I _{DD6}	CKE ≤ 0.2V		48	48	48	mA
Operating Current	I _{DD7A}	Four bank interleaving Reads (BL=4) with auto precharge with t _{RC} =t _{RC} (MIN); t _{CK} =t _{CK} (MIN); Address and control inputs change only during Active Read or Write commands.		3120	2960	2720	mA

**DETAILED TEST CONDITIONS FOR DDR SDRAM I_{DD1} & I_{DD7A}****I_{DD1} : OPERATING CURRENT : ONE BANK**

1. Typical Case : $V_{CC}=2.5V$, $T=25^{\circ}C$
2. Worst Case : $V_{CC}=2.7V$, $T=10^{\circ}C$
3. Only one bank is accessed with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. $I_{OUT} = 0mA$
4. Timing Patterns :
 - DDR200 (100 MHz, CL=2) : $t_{CK}=10ns$, CL2, BL=4, $t_{RCD}=2*t_{CK}$, $t_{RAS}=5*t_{CK}$
Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR266 (133MHz, CL=2.5) : $t_{CK}=7.5ns$, CL=2.5, BL=4, $t_{RCD}=3*t_{CK}$, $t_{RC}=9*t_{CK}$, $t_{RAS}=5*t_{CK}$
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR266 (133MHz, CL=2) : $t_{CK}=7.5ns$, CL=2, BL=4, $t_{RCD}=3*t_{CK}$, $t_{RC}=9*t_{CK}$, $t_{RAS}=5*t_{CK}$
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR333 (166MHz, CL=2.5) : $t_{CK}=6ns$, BL=4, $t_{RCD}=10*t_{CK}$, $t_{RAS}=7*t_{CK}$
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR400 (200MHz, CL=3) : $t_{CK}=5ns$, BL=4, $t_{RCD}=15*t_{CK}$, $t_{RAS}=7*t_{CK}$
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

Legend : A = Activate, R = Read, W = Write, P = Precharge,
N = NOP

A (0-3) = Activate Bank 0-3

R (0-3) = Read Bank 0-3

I_{DD7A} : OPERATING CURRENT : FOUR BANKS

1. Typical Case : $V_{CC}=2.5V$, $T=25^{\circ}C$
2. Worst Case : $V_{CC}=2.7V$, $T=10^{\circ}C$
3. Four banks are being interleaved with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are not changing. $I_{OUT}=0mA$
4. Timing Patterns :
 - DDR200 (100 MHz, CL=2) : $t_{CK}=10ns$, CL2, BL=4, $t_{RRD}=2*t_{CK}$, $t_{RCD}=3*t_{CK}$, Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR266 (133MHz, CL=2.5) : $t_{CK}=7.5ns$, CL=2.5, BL=4, $t_{RRD}=3*t_{CK}$, $t_{RCD}=3*t_{CK}$
Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR266 (133MHz, CL=2) : $t_{CK}=7.5ns$, CL2=2, BL=4, $t_{RRD}=2*t_{CK}$, $t_{RCD}=2*t_{CK}$
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR333 (166MHz, CL=2.5) : $t_{CK}=6ns$, BL=4, $t_{RRD}=3*t_{CK}$, $t_{RCD}=3*t_{CK}$, Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR400 (200MHz, CL=3) : $t_{CK}=5ns$, BL=4, $t_{RRD}=10*t_{CK}$, $t_{RCD}=15*t_{CK}$, Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst



DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

DDR400: $V_{CC} = V_{CCQ} = +2.6V \pm 0.1V$

AC CHARACTERISTICS			403		335		262		265		202			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access window of DQs from CK/CK#		t _{AC}	-0.7	+0.7	-0.7	+0.7	-0.75	+0.75	-0.75	0.75	-0.8	0.8	ns	
CK high-level width		t _{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	25
CK low-level width		t _{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	25
Clock cycle time	CL = 3	t _{CK(3)}	5	7.5	6	13	7.5	13	7.5	13	8	13	ns	38, 43
	CL = 2.5	t _{CK(2.5)}	6	13	7.5	13	7.5	13	7.5/10	13	10	13	ns	38, 43
	CL = 2	t _{CK(2)}	7.5	13									ns	37, 42
DQ and DM input hold time relative to DQS		t _{DH}	0.4		0.45		0.5			0.6			ns	22, 26
DQ and DM input setup time relative to DQS		t _{DS}	0.4		0.45		0.5			0.6			ns	22, 26
DQ and DM input pulse width (for each input)		t _{DIPW}	1.75		1.75		1.75			2			ns	26
Access window of DQS from CK/CK#		t _{DQSCK}	-0.6	+0.6	-0.60	+0.60	-0.75	+0.75	+0.75	-0.8	+0.8		ns	
DQS input high pulse width		t _{DQSH}	0.35		0.35		0.35			0.35			t _{CK}	
DQS input low pulse width		t _{DQSL}	0.35		0.35		0.35			0.35			t _{CK}	
DQS-DQ skew, DQS to last DQ valid, per group, per access		t _{DQSQ}		0.40		0.45		0.5		0.5		0.6	ns	22
Write command to first DQS latching transition		t _{DQSS}	0.72	1.28	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t _{CK}	
DQS falling edge to CK rising - setup time		t _{DSS}	0.2		0.2		0.2		0.2		0.2		t _{CK}	
DQS falling edge from CK rising - hold time		t _{DSH}	0.2		0.2		0.2		0.2		0.2		t _{CK}	
Half clock period		t _{HP}	t _{CH} , t _{CL}		t _{CH} , t _{CL}		t _{CH} , t _{CL}		t _{CH} , t _{CL}		t _{CH} , t _{CL}		ns	29
Data-out high-impedance window from CK/CK#		t _{HZ}		+0.70		+0.70		+0.75		+0.75		+0.8	ns	16, 35
Data-out low-impedance window from CK/CK#		t _{LZ}	-0.70		-0.70		-0.75		-0.75		-0.8		ns	16, 35
Address and control input hold time (1 V/ns)		t _{HF}	0.6		0.75		0.90		0.90	1.1	ns	12	ns	12
Address and control input setup time (1 V/ns)		t _{SF}	0.6		0.75		0.90		0.90		1.1		ns	12
Address and control input hold time (0.5 V/ns)		t _{HS}	0.6		0.80		1		1		1.1		ns	12
Address and control input setup time (0.5 V/ns)		t _{SS}	0.6		0.80		1		1		1.1		ns	12
Address and Control input pulse width (for each input)		t _{IPW}	2.20		2.2		2.2		2.2		2.2		ns	
LOAD MODE REGISTER command cycle time		t _{MRD}	2		12		15		15		16		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t _{QH}	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ns	22
Data hold skew factor		t _{QHS}		0.50		0.60		0.75		0.75		1	ns	
ACTIVE to PRECHARGE command		t _{RAS}	40	70,000	42	70,000	40	120,000	40	120,000	40	120,000	ns	30
ACTIVE to READ with Auto precharge command		t _{RAP}	15		15		15		20		20		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		t _{RC}	55		60		60		65		70		ns	
AUTO REFRESH command period		t _{RFC}	70		72		75		72		75		ns	41
ACTIVE to READ or WRITE delay		t _{RCD}	15		15		15		20		20		ns	
PRECHARGE command period		t _{RP}	15		15		15		20		20		ns	
DQS read preamble		t _{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}	36
DQS read postamble		t _{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	36
ACTIVE bank a to ACTIVE bank b command		t _{RRD}	10		12		15		15		15		ns	
DQS write preamble		t _{WPRE}	0.25		0.25		0.25		0.25		0.25		t _{CK}	
DQS write preamble setup time		t _{WPRES}	0		0		0		0		0		ns	17, 19

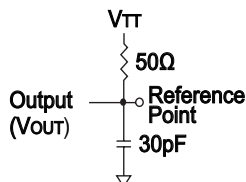
**DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND
RECOMMENDED AC OPERATING CONDITIONS (Continued)**DDR400: $V_{CC} = V_{CCQ} = +2.6V \pm 0.1V$

AC CHARACTERISTICS		403		355		262		265		202			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
DQS write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tck	17
Write recovery time	tWR	15		15		15		15		15		ns	
Internal WRITE to READ command delay	tWTR	2		1		1		1		1		tck	
Data valid output window	na	tqH - tDQSQ		tqH - tDQSQ		tqH - tDQSQ		tqH - tDQSQ		tqH - tDQSQ		ns	22
REFRESH to REFRESH command interval	tREFC		70.3		70.3		70.3		70.3		70.3	μs	21
Average periodic refresh interval	tREFI		7.8		7.8		7.8		7.8		7.8	μs	21
Terminating voltage delay to V_{CC}	tVTD	0		0		0		0		0		ns	
Exit SELF REFRESH to non-READ command	tXSNR	75		75		75		75		80		ns	
Exit SELF REFRESH to READ command	tXSRD	200		200		200		200		200		tck	



Notes

1. All voltages referenced to V_{SS} .
2. Tests for AC timing, I_{DD} , and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL} -to- V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The mini-mum slew rate for the input signals used to test the device is 1V/ns in the range between $V_{IL}(AC)$ and $V_{IH}(AC)$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal V_{CCQ2} of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ± 2 percent of the DC value. Thus, from V_{CCQ2} , V_{REF} is allowed $\pm 25mV$ for DC error and an additional $\pm 25mV$ for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF} .
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with mini-mum cycle time at CL = 2 for 262 and 202, CL = 2.5 for 265, 335 and CL = 3 for 403 with the outputs open.
9. Enables on-chip refresh and address counters.
10. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. $V_{CC} = +2.5V \pm 0.2V$, $V_{CCQ} = +2.5V \pm 0.2V$, $V_{REF} = V_{SS}$, $f = 100$ MHz, $T_A = 25^\circ C$, $V_{OUT}(DC) = V_{CCQ2}$, $V_{OUT}(\text{peak to peak}) = 0.2V$. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. For slew rates < 1 V/ns and ≥ 0.5 V/ns. If the slew rate is $< 0.5V/ns$, timing must be derated: t_{IS} has an additional 50ps per each 100 mV/ns reduction in slew rate from 500 mV/ns, while t_{IH} is unaffected. If the slew rate exceeds 4.5 V/ns, functionality is uncertain.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF} .
14. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, $CKE < 0.3 \times V_{CCQ}$ is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT} .
16. t_{HZ} and t_{LZ} transitions occur in the same access time windows as data valid transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. The intent of the Don't Care state after completion of the postamble is the DQS-driven signal should either be high, low, or high-Z and that any signal transition

within the input switching region must follow valid input requirements. That is, if DQS transitions high [above V_{IHDC} (MIN)] then it must not transition low (below V_{IHDC}) prior to t_{DOSS} (MIN).

18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on t_{DOSS} .
20. MIN (t_{RC} or t_{RFC}) for I_{DD} measurements is the smallest multiple of t_{CK} that meets the minimum absolute value for the respective parameter. t_{RAS} (MAX) for I_{DD} measurements is the largest multiple of t_{CK} that meets the maximum absolute value for t_{RAS} .
21. The refresh period 64ms. This equates to an average refresh rate of 15.625 μs or 7.8125 μs . However, an AUTO REFRESH command must be asserted at least once every 140.6 μs or 70.3 μs ; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
22. The data valid window is derived by achieving other specifications: t_{HP} ($t_{CK}/2$), t_{DOSS} , and t_{QH} ($t_{QH} = t_{HP} - t_{QHS}$). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, beyond which functionality is uncertain. Figure 7, Derating Data Valid Window, shows derating curves are provided below for duty cycles ranging between 50/50 and 45/55.
23. Each byte lane has a corresponding DQS.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (t_{RFC} [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
 - a. Sustain a constant slew rate from the current AC level through to the target AC level, $V_{IL}(AC)$ or $V_{IH}(AC)$.
 - b. Reach at least the target AC level.
 - c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL}(DC)$ or $V_{IH}(DC)$.
26. JEDEC specifies CK and CK# input slew rate must be $\geq 1V/ns$ (2V/ns differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/ DM/DQS slew rate is less than 0.5 V/ns, timing must be derated: 50ps must be added to t_{DS} and t_{DH} for each 100 mV/ns reduction in slew rate. If slew rate exceeds 4 V/ns, functionality is uncertain. For -335, slew rates must be ≥ 0.5 V/ns.
28. V_{CC} must not vary more than 4 percent if CKE is not active while any bank is active.
29. The clock is allowed up to $\pm 150ps$ of jitter. Each timing parameter is allowed to vary by the same amount.
30. t_{HP} min is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CK and CK/ inputs, collectively during bank active.
31. READs and WRITEs with auto precharge are not allowed to be issued until $t_{RAS}(MIN)$ can be satisfied prior to the internal precharge command being issued.
32. Any positive glitch in the nominal voltage must be less than 1/3 of the clock and not more than +400mV or 2.9V maximum, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2V mini-mum, whichever is more positive.



33. The voltage levels used are derived from a minimum V_{CC} level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
34. V_{IH} overshoot: $V_{IH} (MAX) = V_{CCQ} + 1.5V$ for a pulse width $< 3ns$ and the pulse width can not be greater than 1/3 of the cycle rate. V_{IL} undershoot: $V_{IL} (MIN) = -1.5V$ for a pulse width $\leq 3ns$ and the pulse width can not be greater than 1/3 of the cycle rate.
35. V_{CC} and V_{CCQ} must track each other.
36. $t_{HZ} (MAX)$ will prevail over $t_{DQSK} (MAX) + t_{RPST} (MAX)$ condition. $t_{LZ} (MIN)$ will prevail over $t_{DQSK} (MIN) + t_{RPRE} (MAX)$ condition.
37. t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}).
38. During initialization, V_{CCQ} , V_{TT} , and V_{REF} must be equal to or less than $V_{CC} + 0.3V$. Alternatively, V_{TT} may be 1.35V maximum during power up, even if V_{CC}/V_{CCQ} are 0V, provided a minimum of 42 Ω of series resistance is used between the V_{TT} supply and the input pin.
39. The current part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
40. Random addressing changing and 50 percent of data changing at every transfer.
41. Random addressing changing and 100 percent of data changing at every transfer.
42. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until t_{REF} later.
43. l_{DD2N} specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. l_{DD2Q} is similar to l_{DD2F} except l_{DD2Q} specifies the address and control inputs to remain stable. Although l_{DD2F} , l_{DD2N} , and l_{DD2Q} are similar, l_{DD2F} is "worst case."
44. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles (before READ commands).
45. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
46. When an input signal is HIGH or LOW, it is defined as a steady state logic HIGH or LOW.



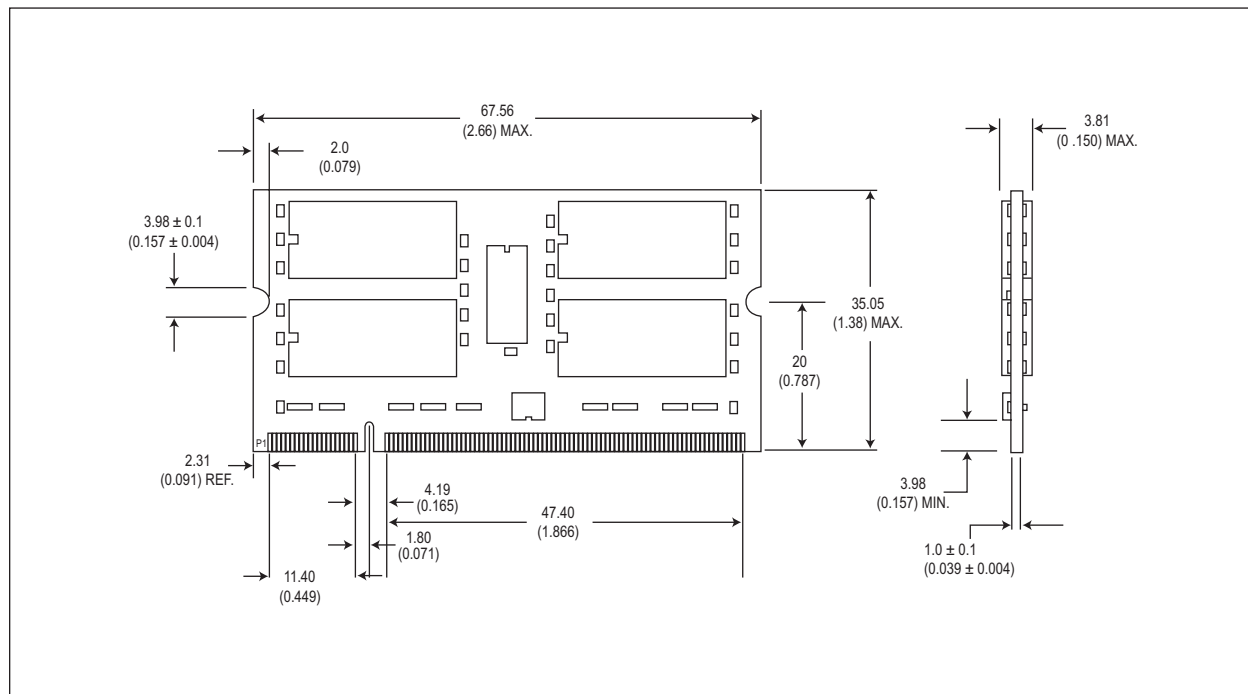
ORDERING INFORMATION FOR D4

Part Number	Speed	Height*	Commercial Operating Range
W3EG6467S403D4	200MHz/400Mbps, CL=3	35.05 (1.38") MAX	0°C to 70°C
W3EG6467S335D4	166MHz/333Mbps, CL=2.5	35.05 (1.38") MAX	0°C to 70°C
W3EG6467S262D4	133MHz/266Mbps, CL=2	35.05 (1.38") MAX	0°C to 70°C
W3EG6467S265D4	133MHz/266Mbps, CL=2.5	35.05 (1.38") MAX	0°C to 70°C
W3EG6467S202D4	100MHz/200Mbps, CL=2	35.05 (1.38") MAX	0°C to 70°C

NOTES:

- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D4



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



Document Title

512MB – 2x32Mx64, DDR SDRAM UNBUFFERED

Revision History

Rev #	History	Release Date	Status
Rev A	Created	6-17-03	Advanced
Rev 0	0.1 Updated all specs (AC, DC, I _{DD}) 0.2 Added DDR400 0.3 Added AC specs 0.4 Added D4 and BD4 package options 0.5 Added RoHS notes 0.6 Changed from Advanced to Preliminary 0.7 Removed "ED" from part number	12-04	Advanced
Rev 1	1.1 Added source control notes 1.2 Added industrial temperature notes	1-05	Advanced