

256MB – 2x16Mx64 DDR SDRAM SO-DIMM, UNBUFFERED

FEATURES

- Unbuffered Double-data-rate architecture
- DDR300 and DDR400
 - JEDEC design specifications
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2.5, 3
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh, (8K/64ms Refresh)
- Serial presence detect with EEPROM
- Dual Rank
- Power Supply: $V_{CC} = V_{CC}: 2.5V \pm 0.2V$ (DDR300)
 $V_{CC} = V_{CCQ}: 2.6V \pm 0.1V$ (DDR400)
- JEDEC standard 200 pin SO-DIMM package
 - Package height options:
D4: 31.75mm (1.25") TYP

NOTE: Consult factory for availability of:

- RoHS compliant products
- Vendor source control options
- Industrial temperature option

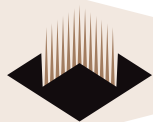
DESCRIPTION

The WV3EG6437S is a 2x16Mx64 Double Data Rate SDRAM memory module based on 256Mb DDR SDRAM components. The module consists of eight 16Mx16 DDR SDRAMs in 66 pin TSOP package mounted on a 200 Pin FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change without notice.

OPERATING FREQUENCIES

	DDR400@CL=3	DDR333@CL=2.5
Clock Speed	200MHz	166MHz
CL-tRCD-tRP	3-3-3	2.5-3-3



PIN CONFIGURATIONS

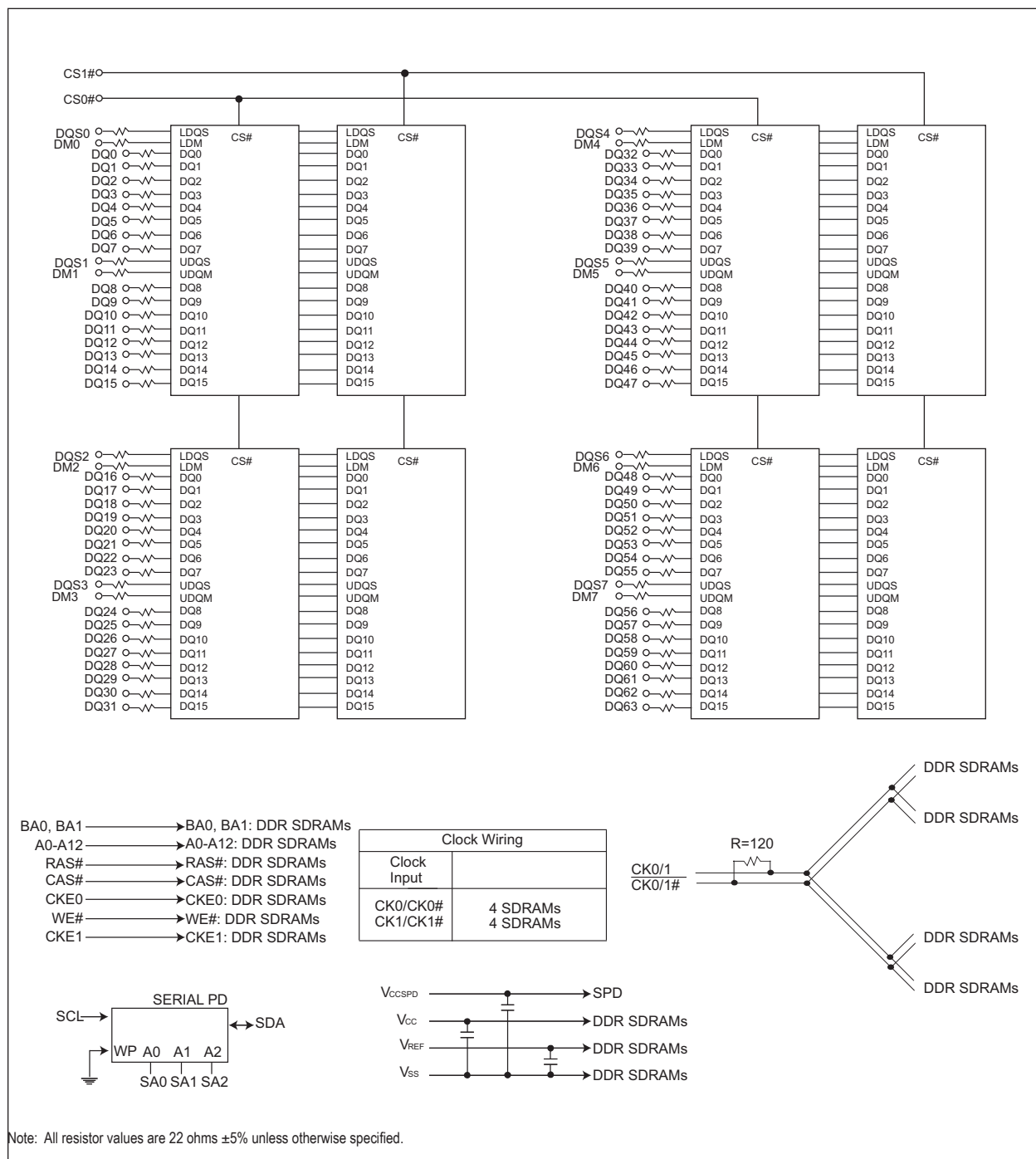
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{REF}	51	V _{SS}	101	A9	151	DQ42
2	V _{REF}	52	V _{SS}	102	A8	152	DQ46
3	V _{SS}	53	DQ19	103	V _{SS}	153	DQ43
4	V _{SS}	54	DQ23	104	V _{SS}	154	DQ47
5	DQ0	55	DQ24	105	A7	155	V _{CC}
6	DQ4	56	DQ28	106	A6	156	V _{CC}
7	DQ1	57	V _{CC}	107	A5	157	V _{CC}
8	DQ5	58	V _{CC}	108	A4	158	CK1#
9	V _{CC}	59	DQ25	109	A3	159	V _{SS}
10	V _{CC}	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	V _{SS}
12	DM0	62	DM3	112	A0	162	V _{SS}
13	DQ2	63	V _{SS}	113	V _{CC}	163	DQ48
14	DQ6	64	V _{SS}	114	V _{CC}	164	DQ52
15	V _{SS}	65	DQ26	115	A10	165	DQ49
16	V _{SS}	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	V _{CC}
18	DQ7	68	DQ31	118	RAS#	168	V _{CC}
19	DQ8	69	V _{CC}	119	WE#	169	DQS6
20	DQ12	70	V _{CC}	120	CAS#	170	DM6
21	V _{CC}	71	NC	121	CS0#	171	DQ50
22	V _{CC}	72	NC	122	CS1#	172	DQ54
23	DQ9	73	NC	123	NC	173	V _{SS}
24	DQ13	74	NC	124	NC	174	V _{SS}
25	DQ31	75	V _{SS}	125	V _{SS}	175	DQ51
26	DM1	76	V _{SS}	126	V _{SS}	176	DQ55
27	V _{SS}	77	NC	127	DQ32	177	DQ56
28	V _{SS}	78	NC	128	DQ36	178	DQ60
29	DQ10	79	NC	129	DQ33	179	V _{CC}
30	DQ14	80	NC	130	DQ37	180	V _{CC}
31	DQ11	81	V _{CC}	131	V _{CC}	181	DQ57
32	DQ15	82	V _{CC}	132	V _{CC}	182	DQ61
33	V _{CC}	83	NC	133	DQS4	183	DQS7
34	V _{CC}	84	NC	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	V _{SS}
36	V _{CC}	86	NC	136	DQ38	186	V _{SS}
37	CK0#	87	V _{SS}	137	V _{SS}	187	DQ58
38	V _{SS}	88	V _{SS}	138	V _{SS}	188	DQ62
39	V _{SS}	89	NC	139	DQ35	189	DQ59
40	V _{SS}	90	V _{SS}	140	DQ39	190	DQ63
41	DQ16	91	NC	141	DQ40	191	V _{CC}
42	DQ20	92	V _{CC}	142	DQ44	192	V _{CC}
43	DQ17	93	V _{CC}	143	V _{CC}	193	SDA
44	DQ21	94	V _{CC}	144	V _{CC}	194	SA0
45	V _{CC}	95	CKE1	145	DQ41	195	SCL
46	V _{CC}	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	V _{CCSPD}
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	V _{SS}	199	NC
50	DQ22	100	A11	150	V _{SS}	200	NC

PIN NAMES

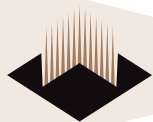
A0 – A12	Address input
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
DQS0-DQS7	Data Strobe Input/Output
CK0, CK1	Clock Inputs
CK0#, CK1#	
CKE0, CKE1	Clock Enable Inputs
CS0#, CS1#	Chip select Inputs
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DM0-DM7	Data Mask
V _{CC}	Power Supply
V _{SS}	Ground
V _{REF}	Reference Power Supply
V _{CCSPD}	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	SPD clock input
SA0-SA2	SPD address
NC	No Connect



FUNCTIONAL BLOCK DIAGRAM



Note: All resistor values are 22 ohms ±5% unless otherwise specified.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to 3.6	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC} , V _{CCQ}	-0.5 to 3.6	V
Storage Temperature	T _{STG}	-55 to +150	°C
Operating Temperature	T _A	0 - 70	°C
Power Dissipation	P _D	8	W
Short Circuit Current	I _{OS}	50	mA

Note:

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC CHARACTERISTICS

0°C ≤ T_A ≤ 70°C

Parameter		Symbol	Min	Max	Unit
Supply voltage DDR333		V _{CC}	2.3	2.7	V
I/O Supply voltage DDR333		V _{CCQ}	2.3	2.7	V
Supply Voltage DDR400		V _{CC}	2.5	2.7	V
I/O Supply Voltage DDR400		V _{CCQ}	2.5	2.7	V
I/O Reference voltage		V _{REF}	0.49 + V _{CC}	0.51 + V _{CC}	V
I/O Termination voltage		V _{TT}	V _{REF} - 0.04	V _{REF} + 0.04	V
Input logic high voltage		V _{IH} (DC)	V _{REF} + 0.15	V _{CC} + 0.30	V
Input logic low voltage		V _{IL} (DC)	-0.3	V _{REF} - 0.15	V
Input voltage level, CK and CK#		V _{In} (DC)	-0.3	V _{CC} + 0.30	V
Input differential voltage, CK and CK#		V _{ID} (DC)	0.36	V _{CC} + 0.60	V
Input crossing point voltage, CK and CK#		V _{IX} (DC)	0.3	V _{CC} + 0.60	V
Input leakage current	Addr, CAS#, RAS#, WE#	I _I	-16	16	μA
	CS#, CKE		-8	8	μA
	CK, CK#		-8	8	μA
	DM		-4	4	μA
Output leackage current	DQ, DQS	I _{OZ}	-10	10	μA
Output high current (normal strength) V _{OUT} = V _{TT} + 0.84V		I _{OH}	-16.8	-	mA
Output high current (normal strength) V _{OUT} = V _{TT} - 0.84V		I _{OL}	16.8	-	mA
Output high current (half strength) V _{OUT} = V _{TT} + 0.45V		I _{OH}	-9	-	mA
Output high current (half strength) V _{OUT} = V _{TT} - 0.45V		I _{OL}	9	-	mA

Notes:

- V_{REF} is expected to equal 0.5*V_{CCQ} of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-2 percent of the DC value.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
- V_{ID} is the magnitude of the difference between the input level on CK and the input level of CK#.
- V_{CCQ} of all IC's are tied to V_{CC}.

White Electronic Designs Corp. reserves the right to change products or specifications without notice.

**AC OPERATING CONDITIONS**All voltages referenced to V_{SS}

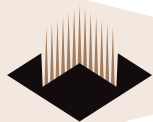
Parameter	Symbol	Min.	Max.	Units	Notes
Input High (Logic1) Voltage	$V_{IH(AC)}$	$V_{REF} + 0.31$		V	1
Input Low (Logic0) Voltage	$V_{IL(AC)}$		$V_{REF} - 0.31$	V	1
Input Differential Voltage, CK and CK# input	$V_{ID(AC)}$	0.7	$V_{CCQ} + 0.6$	V	
Input Crossing Point Voltage, CK and CK# input	$V_{IX(AC)}$	$0.5 \cdot V_{CC} - 0.2$	$0.5 \cdot V_{CC} + 0.2$	V	

Notes:

- V_{IH} overshoot: $V_{IN} = V_{CC} + 1.5V$ for a pulse width $\leq 3ns$ and the pulse can not be greater than 1/3 of the cycle rate.
 V_{IL} undershoot: $V_{IL} = -1.5V$ for a pulse width $\leq 3ns$ and the pulse can not be greater than 1/3 of the cycle rate.

INPUT/OUTPUT CAPACITANCE $T_A = 25^\circ C$, $f = 100MHz$

Parameter	Symbol	Min	Max	Units
Input Capacitance (A0~A12, BA0~BA1, RAS#, CAS#, WE#)	C_{IN1}	20	28	pF
Input Capacitance (CKE0, CKE1)	C_{IN2}	12	16	pF
Input Capacitance (CS0#, CS1#)	C_{IN3}	12	16	pF
Input Capacitance CK, CK0#, CK1, CK1#)	C_{IN4}	12	16	pF
Input Capacitance (DM0 ~ DM7), (DQS0 ~ DQS7)	C_{IN5}	12	14	pF
Input Capacitance (DQ0 ~ DQ63)	C_{OUT1}	12	14	pF



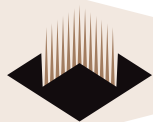
I_{CC} SPECIFICATIONS AND TEST CONDITIONS

Parameter	Symbol	Conditions	DDR403 @CL=3 Max	DDR333 @CL=2.5 Max	Units
Operating Current	I _{CC0*}	One device bank; Active - Precharge; t _{RC} =t _{RC} (MIN); t _{CK} =t _{CK} (MIN); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	456	372	mA
Operating Current	I _{CC1*}	One device bank; Active-Read-Precharge; Burst = 2; t _{RC} =t _{RC} (MIN);t _{CK} =t _{CK} (MIN) ; I _{out} = 0mA; Address and control inputs changing once per clock cycle.	616	512	mA
Precharge Power-Down Standby Current	I _{CC2P**}	All device banks idle; Power- down mode; t _{CK} =t _{CK} (MIN); CKE=(low)	32	24	mA
Idle Standby Current	I _{CC2F**}	CS# = High; All device banks idle; t _{CK} =t _{CK} (MIN); CKE = high; Address and other control inputs changing once per clock cycle. V _{in} = V _{ref} for DQ, DQS and DM.	240	240	mA
Active Power-Down Standby Current	I _{CC3P**}	One device bank active; Power-down mode; t _{CK} (MIN); CKE=(low)	400	280	mA
Active Standby Current	I _{CC3N**}	CS# = High; CKE = High; One device bank; Active-Precharge; t _{RC} =t _{RAS} (MAX); t _{CK} =t _{CK} (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	520	440	mA
Operating Current	I _{CC4R*}	Burst = 2; Reads; Continous burst; One device bank active;Address and control inputs changing once per clock cycle; t _{CK} =t _{CK} (MIN); I _{out} = 0mA.	736	652	mA
Operating Current	I _{CC4W**}	Burst = 2; Writes; Continous burst; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} =t _{CK} (MIN); DQ,DM and DQS inputs changing twice per clock cycle.	736	652	mA
Auto Refresh Current	I _{CC5**}	t _{RC} =t _{RC} (MIN)	1,600	1,440	mA
Self Refresh Current	I _{CC6**}	CKE ≤ 0.2V	24	24	mA
Operating Current	I _{CC7*}	Four bank interleaving Reads (BL=4) with auto precharge with t _{RC} =t _{RC} (MIN); t _{CK} =t _{CK} (MIN); Address and control inputs change only during Active Read or Write commands.	1,416	1,332	mA

Note: I_{CC} specification is based on SAMSUNG components. Other DRAM Manufacturers specification may be different.

* Value calculated as one module rank in this operation condition, and all other module ranks in I_{CC2P} (CKE LOW) mode.

** Value calculated reflects all module ranks in the operating condition.



DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

AC CHARACTERISTICS		403		335		UNITS
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	
Access window of DQs from CK/CK#	t _{AC}	-0.65	+0.65	-0.7	+0.7	ns
CK high-level width	t _{CH}	0.45	0.55	0.45	0.55	t _{CK}
CK low-level width	t _{CL}	0.45	0.55	0.45	0.55	t _{CK}
Clock cycle time	CL = 3	t _{CK} (3)	5	10		ns
	CL = 2.5	t _{CK} (2.5)		6	12	ns
DQ and DM input hold time relative to DQS	t _{DH}	0.40		0.40		ns
DQ and DM input setup time relative to DQS	t _{DS}	0.40		0.40		ns
DQ and DM input pulse width (for each input)	t _{DIPW}	1.75		1.75		ns
Access window of DQS from CK/CK#	t _{DQSCK}	-0.55	+0.65	-0.60	+0.60	ns
DQS input high pulse width	t _{DQSH}	0.35		0.35		t _{CK}
DQS input low pulse width	t _{DQSL}	0.35		0.35		t _{CK}
DQS-DQ skew, DQS to last DQ valid, per group, per access	t _{DQSQ}		0.40		0.45	ns
Write command to first DQS latching transition	t _{DQSS}	0.72	1.28	0.75	1.25	t _{CK}
DQS falling edge to CK rising - setup time	t _{DSS}	0.20		0.20		t _{CK}
DQS falling edge from CK rising - hold time	t _{DSH}	0.20		0.20		t _{CK}
Half clock period	t _{HP}	t _{CH} (MIN) or t _{CL} (MIN)		t _{CH} (MIN) or t _{CL} (MIN)		ns
Data-out high-impedance window from CK/CK#	t _{HZ}		+0.65		+0.70	ns
Data-out low-impedance window from CK/CK#	t _{LZ}	-0.65		-0.70		ns
Address and control input hold time (1 V/ns)	t _{HIF}	0.60		0.75		ns
Address and control input setup time (1 V/ns)	t _{ISF}	0.60		0.75		ns
Address and control input hold time (0.5 V/ns)	t _{HS}	0.70		0.80		ns
Address and control input setup time (0.5 V/ns)	t _{ISS}	0.70		0.75		ns
Address and Control input pulse width (for each input)	t _{IPW}	2.20		2.20		ns
LOAD MODE REGISTER command cycle time	t _{MRD}	10		10		ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t _{QH}	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ns
Data hold skew factor	t _{QHS}		0.50		0.55	ns
ACTIVE to PRECHARGE command	t _{RAS}	40	70K	42	70K	ns
ACTIVE to READ with Auto precharge command	t _{RAP}	15		18		ns
ACTIVE to ACTIVE/AUTO REFRESH command period	t _{RC}	55		60		ns
AUTO REFRESH command period	t _{RFC}	70		72		ns
ACTIVE to READ or WRITE delay	t _{RCd}	15		18		ns
PRECHARGE command period	t _{RP}	15		18		ns
DQS read preamble	t _{RPRE}	0.90	1.10	0.9	1.10	t _{CK}
DQS read postamble	t _{RPST}	0.40	0.60	0.4	0.60	t _{CK}
ACTIVE bank a to ACTIVE bank b command	t _{RRD}	10		12		ns
DQS write preamble	t _{WPRE}	0.25		0.25		t _{CK}
DQS write preamble setup time	t _{WPRES}	0		0		ns

Note: AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.

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**DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND
RECOMMENDED AC OPERATING CONDITIONS (Continued)**

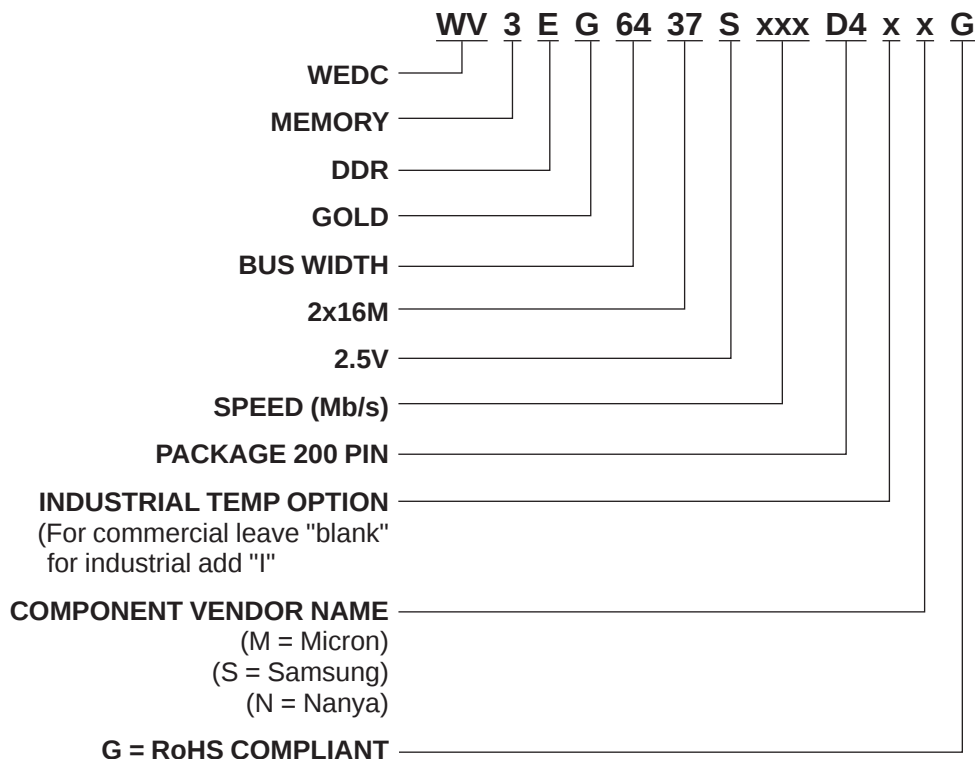
AC CHARACTERISTICS		403		355		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS
DQS write postamble	tWPST	0.40	0.60	0.40	0.60	tck
Write recovery time	tWR	15		15		ns
Internal WRITE to READ command delay	tWTR	2		1		tck
Average periodic refresh interval	tREFI		7.80		7.80	μs
Exit SELF REFRESH to non-READ command	tXSNR	75		75		ns
Exit SELF REFRESH to READ command	tXSRD	200		200		tck
Auto precharge write recovery + precharge time	tRAL	tWR/tck +tRP/tck		tWR/tck +tRP/tck		tck

Note: AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.





PART NUMBERING GUIDE





Document Title

256MB – 32Mx64, DDR SDRAM UNBUFFERED

DRAM DIE OPTIONS:

- SAMSUNG: H-Die (K4H561638H-UCB3) RoHS
- MICRON: T26A: F-Die

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	June 2006	Advanced