Integrated Circuit Systems, Inc.

ICS91730

Low EMI, Spread Modulating, Clock Generator

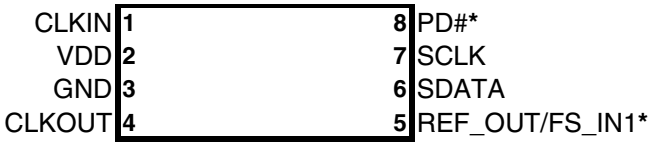
Features:

- ICS91730 is a Spread Spectrum Clock targeted for Mobile PC and LCD panel applications that generates an EMI-optimized clock signal (EMI peak reduction of 7-14 dB on 3rd-19th harmonics) through use of Spread Spectrum techniques.
- ICS91730 focuses on the lower input frequency range of 14.318 to 80.00 MHz with a spread modulation of 20kHz to 40kHz.

Specifications:

- Supply Voltages: V_{DD} = 3.3V ±0.3V
- Frequency range: 14.318 MHz ≤ Fin ≥ 80 MHz
- Cyc to Cyc jitter: <150ps
- Output duty cycle 45-55%
- Guarantees +85°C operational condition.
- 8-pin SOIC
- Reference input

Pin Configuration



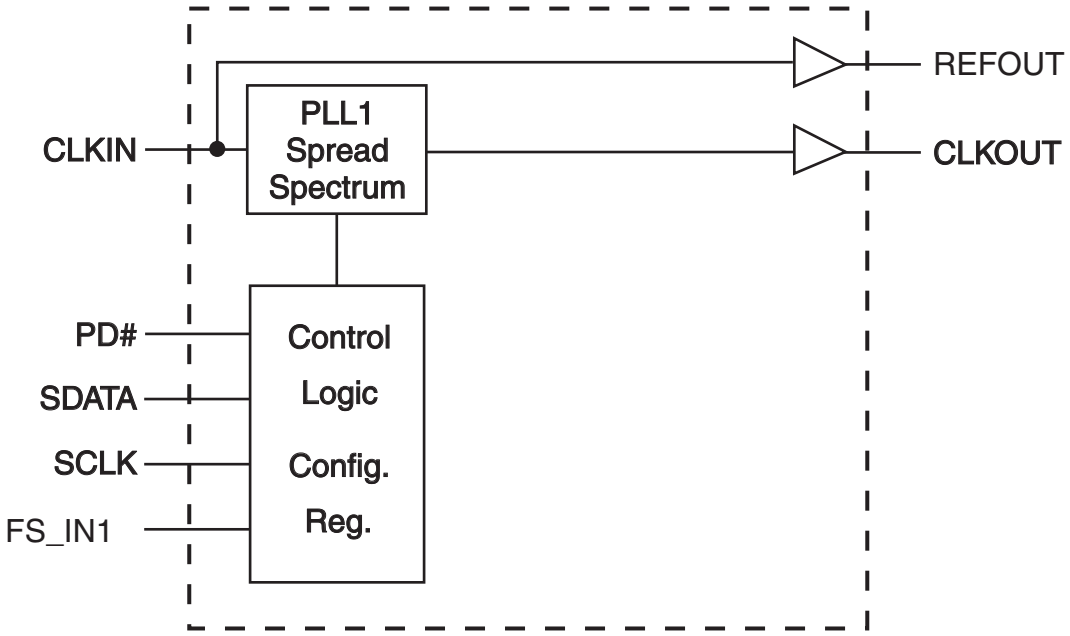
8 Pin SOIC

* Internal Pull-Up Resistor

Functionality

FSIN_1	MHz	Spread % default
0	14.318 MHz in --> 27MHz out	-0.8 down spread
1	27.00MHz in --> 27.00MHz out	-1.25 down spread

Block Diagram



Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	CLKIN	PWR	Input for reference clock.
2	VDD	IN	Power supply, nominal 3.3V
3	GND	OUT	Ground pin.
4	CLKOUT	I/O	Modulated clock output.
5	REF_OUT/FS_IN1*	I/O	Un-modulated 3.3V reference clock output. Frequency select latch input. Refer to the functionality table.
6	SDATA	PWR	Data pin for SMBus circuitry, 5V tolerant.
7	SCLK	PWR	Clock pin of SMBus circuitry, 5V tolerant.
8	PD#*	PWR	Asynchronous active low input pin, with 120Kohm internal pull-up resistor, used to power down the device. The internal clocks are disabled and the VCO and the crystal are stopped.

* Internal Pull-Up Resistor ** Internal Pull-Down Resistor

Table 1: Frequency Configuration Table (See I2C Byte 0)

	FS4	FS3	FS2	FS1	FS0	Sprd Type	Sprd %
14in/27out	0	0	0	0	0	DOWN SPREAD (-)	0.60
	0	0	0	0	1		0.80
	0	0	0	1	0		1.00
	0	0	0	1	1		1.25
	0	0	1	0	0		1.50
	0	0	1	0	1		2.00
	0	0	1	1	0	CENTER SPD (+/-)	0.50
	0	0	1	1	1		1.00
14in/14out 27in/27out	0	1	0	0	0	DOWN SPREAD (-)	0.60
	0	1	0	0	1		1.00
	0	1	0	1	0		0.80
	0	1	0	1	1	CTR SPD	0.3
	0	1	1	0	0	DOWN SPREAD (-)	1.50
	0	1	1	0	1		1.75
	0	1	1	1	0		2.00
	0	1	1	1	1		2.50
	1	0	0	0	0		3.00
	1	0	0	0	1		1.25
	1	0	0	1	0	CENTER SPD (+/-)	0.40
	1	0	0	1	1		0.50
	1	0	1	0	0		0.70
	1	0	1	0	1		1.00
	1	0	1	1	0		1.20
	1	0	1	1	1		1.50
48in/48out 66in/66out	1	1	0	0	0	DOWN SPREAD (-)	0.60
	1	1	0	0	1		0.80
	1	1	0	1	0		1.00
	1	1	0	1	1		1.25
	1	1	1	0	0		1.50
	1	1	1	0	1		2.00
	1	1	1	1	0	CENTER SPD (+/-)	0.50
	1	1	1	1	1		1.00

Above is the hard coded 5 bit (32 entry) ROM table.
FS3:0 are ONLY accessible through I2C software programming bits (byte0 bits5:7). FS4 can also be decoded from FS_IN1 latched input hardware pins.
FS_IN1 → FS4. Upon power-up the default is to use hardware selection of FS_IN1 latched value.
FS3 = 0, FS2 = 0, FS1 = 0, FS0 = 1 upon power-up (refer to the functionality table on page 1).
To access non-default spread entries in the ROM, byte0 programming should be used. In order to change the power up default of FS_IN1 = 1 (-1.25% down spread) to any other spread % entry, first change byte0bit 0 to software selection by switching this bit to a '1' and then program the desired percentage by changing byte0 bits 7:3.

General I²C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D4 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D4 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D5 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D4(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	○		
	○		○
	○		○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D4(H)			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D5(H)			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			○
	○		○
	○		○
	○		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Byte 0	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	-	FS0	Spread/FS0	RW	Srpead Pecentage See Table1 These are I2C bits only		1
Bit 6	-	FS1	Spread/FS1	RW			0
Bit 5		FS2	Spread/FS2	RW			0
Bit 4		FS3	Spread/FS3	RW			0
Bit 3		FS4	FS4	RW			0
Bit 2		PD# Tri_Sate	PD# Tri_Sate	RW	Hi-Z	LOW	1
Bit 1		Spread Enable	Spread Enable	RW	OFF	ON	1
Bit 0		HW/SW Control	Spread Spectrum Control FS 3:4 Hard/Software Select	RW	HW	SW	0

Byte 1	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7		REF_OUT	REF_OUT_Enable	RW	Disable	Enable	1
Bit 6	-	REF_OUT	Slew Rate REF-OUT	RW	Nominal	Fast	1
Bit 5		FS-IN_1	FS-IN_1 Readback	R	-	-	X
Bit 4		(Reserved)	(Reserved)	R	-	-	0
Bit 3		CLK_OUT	Slew Rate CLK-OUT	RW	Nominal	Fast	1
Bit 2		CLK_OUT	CLK_OUT_Enable	RW	Disable	Enable	1
Bit 1		(Reserved)	(Reserved)	R	-	-	1
Bit 0		(Reserved)	(Reserved)	R	-	-	1

Byte 2	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	x	-	(Reserved)	-	-	-	1
Bit 6	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 5	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 4	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 3	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 2	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 1	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 0	x	(Reserved)	(Reserved)	RW	Disable	Enable	1

Byte 3	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 6	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 5	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 4	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 3	x	(Reserved)	(Reserved)	RW	-	-	1
Bit 2	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 1	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 0	X	(Reserved)	(Reserved)	RW	-	-	1

Byte 4	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 6	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 5	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 4	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 3	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 2	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 1	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 0	X	(Reserved)	(Reserved)	RW	-	-	1

Byte 5	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	X	(Reserved)	(Reserved)	-	-	-	1
Bit 6	X	(Reserved)	(Reserved)	-	-	-	1
Bit 5	X	(Reserved)	(Reserved)	-	-	-	1
Bit 4	X	(Reserved)	(Reserved)	-	-	-	1
Bit 3	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 2	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 1	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 0	X	(Reserved)	(Reserved)	RW	-	-	1

Byte 6	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	X	Revision ID Bit 3	(Reserved)	R	-	-	1
Bit 6	X	Revision ID Bit 2	(Reserved)	R	-	-	1
Bit 5	X	Revision ID Bit 1	(Reserved)	R	-	-	1
Bit 4	X	Revision ID Bit 0	(Reserved)	R	-	-	1
Bit 3	X	Vendor ID Bit 3	(Reserved)	R	-	-	1
Bit 2	X	Vendor ID Bit 2	(Reserved)	R	-	-	1
Bit 1	X	Vendor ID Bit 1	(Reserved)	R	-	-	1
Bit 0	X	Vendor ID Bit 0	(Reserved)	R	-	-	1

Absolute Maximum Ratings

Supply Voltage . . . . . 3.7 V
Voltage on any pin with respect to GND . . . -0.5 to +3.7 V
Storage Temperature . . . . . –55°C to +150°C
Power Dissipation . . . . . 0.5 W

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Powerdown Current	$I_{DD3.3PD}$			1	5	mA
Input Frequency	Fi	V_{DD} = 3.3 V		14.318		MHz
Pin Inductance	Lpin				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition time[1]	T_{trans}	To 1st crossing of target frequency			3	ms
Settling time[1]	Ts	From 1st crossing to 1% target frequency			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target frequency			3	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CLKOUT

T_A = 0 - 85°C; V_{DD} = 3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	
Rise Time	tr3	V_{OL} = 0.41V, V_{OH} = 0.86V	0.5	0.6	1	ns
Fall Time	tf3	V_{OH} = 0.86V V_{OL} = 0.41V	0.5	0.6	1	ns
Duty Cycle	d_{t3}	measurement from differential wavefrom -0.35V to +035V	45	50	55	%
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50%		50	150	ps

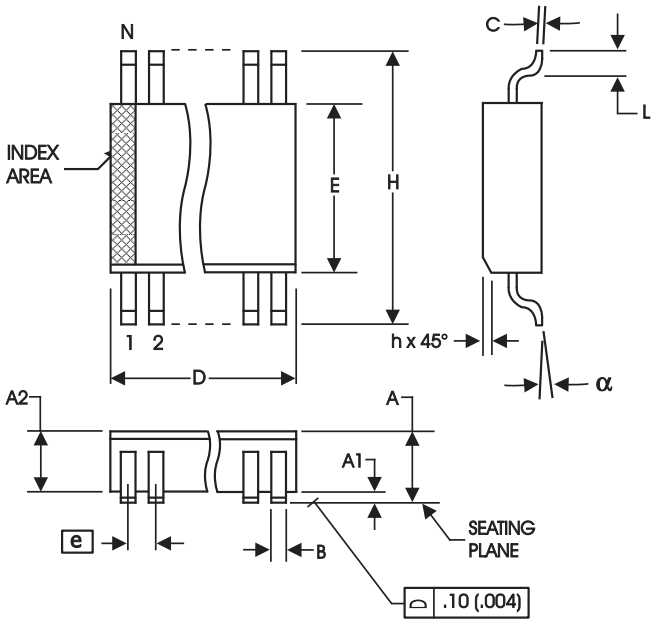
[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 85°C; V_{DD} = 3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	V_O = V_{DD}*(0.5)	20	48	60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.2	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.2	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		105	300	ps

[1]Guaranteed by design, not 100% tested in production.



8-pin SOIC

150 mil (Narrow Body) SOIC

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	SEE VARIATIONS		SEE VARIATIONS	
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
8	4.80	5.00	.1890	.1968

Reference Doc.: JEDEC Publication 95, MS-012

10-0030

Ordering Information

ICS91730yMLF-T

Example:

ICS XXXX y M LF- T

- **Designation for tape and reel packaging**
- **RoHS Compliant (Optional)**
- **Package Type**
  M = SOIC
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0794D—05/23/05

Revision History

Rev.	Issue Date	Description	Page #
B	06/25/04	Add Lead Free package description to Ordering Information	10
C	06/29/04	Add Revision History table to datasheet.	11
D	05/23/05	1. Revise ABS Max Ratings. 2. Updated REF Electrical Characteristics Table. 3. Updated LF Ordering Information from "Lead Free" to "RoHS Compliant".	8-10