
EM78P510N

**8-Bit Microprocessor
with OTP ROM**

Product Specification

Doc. Version 0.9


ELAN MICROELECTRONICS CORP.

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Specification Revision History

| Doc. Version | Revision Description | Date |
|--------------|--|------------|
| 0.9 | 1. Preliminary version 2. Modified sections 6-3 and 6-23 3. Modified the Operating Voltage | 2006/09/12 |

1 General Description

The EM78P510N is an 8-bit RISC type microprocessor with low power, high speed CMOS technology. Integrated onto a single chip are on-chip Watchdog Timer (WDT), LCD Data RAM, ROM, programmable real time clock counter, internal/external interrupt, power down mode, 12 bits A/D Converter, UART, SPI, 8-channel LED driver, LCD driver and tri-state I/O.

2 Features

- Operating voltage: 2.3V~5.5V
- Operating temperature: -40°C~85°C
- Dual clock operation or PLL operation mode
- Crystal/RC oscillation circuit selected by code option for system clock
- 32.768kHz crystal/RC oscillation circuit selected by code option for sub-oscillation
- Operation mode
 - Normal mode
 - Green mode
 - Idle mode
 - Sleep mode
- 272 bytes general purpose register
- 8K×13 on-chip Electrical One Time Programmable Read Only Memory (OTP-ROM)
- 43 bidirectional tri-state I/O ports
- 8-level stacks for subroutine nesting
- 8-bit real time clock/counter (TCC)
- 8-bit Timer 1, auto reload counter/timer which can be interrupt sources
 - Timer
 - Toggle output
 - UART baud rate generator
 - Capture
 - PWM
- 8-bit Timer 2, auto reload counter/timer which can be interrupt sources
 - Timer
 - PWM
 - SPI baud rate generator
- Two sets of 8 bits auto reload counter/timer which can be cascaded to one 16-bit counter/timer

- Programmable free running on chip watchdog timer
- Watch timer (1.0 sec / 0.5 sec / 0.25 sec / 3.91 ms) with Interrupt
- Buzzer Output (0.5K / 1K / 2K / 4K)
- Low Voltage Reset (2.6V / 3.3V / 3.9V)
- Low Voltage Detector (2.4V / 2.7V / 3.3V / 3.9V)
- 8-pin Direct Drive LED
- External Interrupt wake-up function
- 18 interrupt sources, 10 external, 8 internal
- 99.9% Single Instruction Cycle Commands
- LCD
 - Common driver pins: 1, 3, 4, 8
 - Segment driver pins: 4, 8, 12, 16, 20, 23
 - 1/2, 1/3, 1/4 bias
 - Static 1/3, 1/4, 1/8 duty
- A/D Converter
 - 12-bit Converter resolution
 - 56 μ s conversion speed at 1MHz f_{ADC} clock
 - 12-channel A/D Converter
- SPI (Serial Peripheral Interface)
 - 8-bit transmit/receive mode
 - 8-bit receive mode
 - LSB-first or MSB-first transmission selectable
 - Internal or external clock source
- UART: Universal Asynchronous Receiver/Transmitter
 - Three modes of transmit/receive
 - Allow the addition of a parity bit
- Package type:
 - 48-pin LQFP (7×7mm) : EM78P510NQ
 - 44-pin LQFP (10×10mm) : EM78P510NAQ
 - 44-pin QFP (10×10mm) : EM78P510NBQ
 - 42-pin DIP (600mil) : EM78P510NP
 - 32-pin SDIP(400mil) : EM78P510NK
 - 32-pin SDIP(400mil) : EM78P510NAK
 - 32-pin SOP (450mil) : EM78P510NM
 - 32-pin SOP (450mil) : EM78P510NAM

3 Applications

- Remote control for air conditioner
- Health care
- Home appliance

4 Pin Assignment

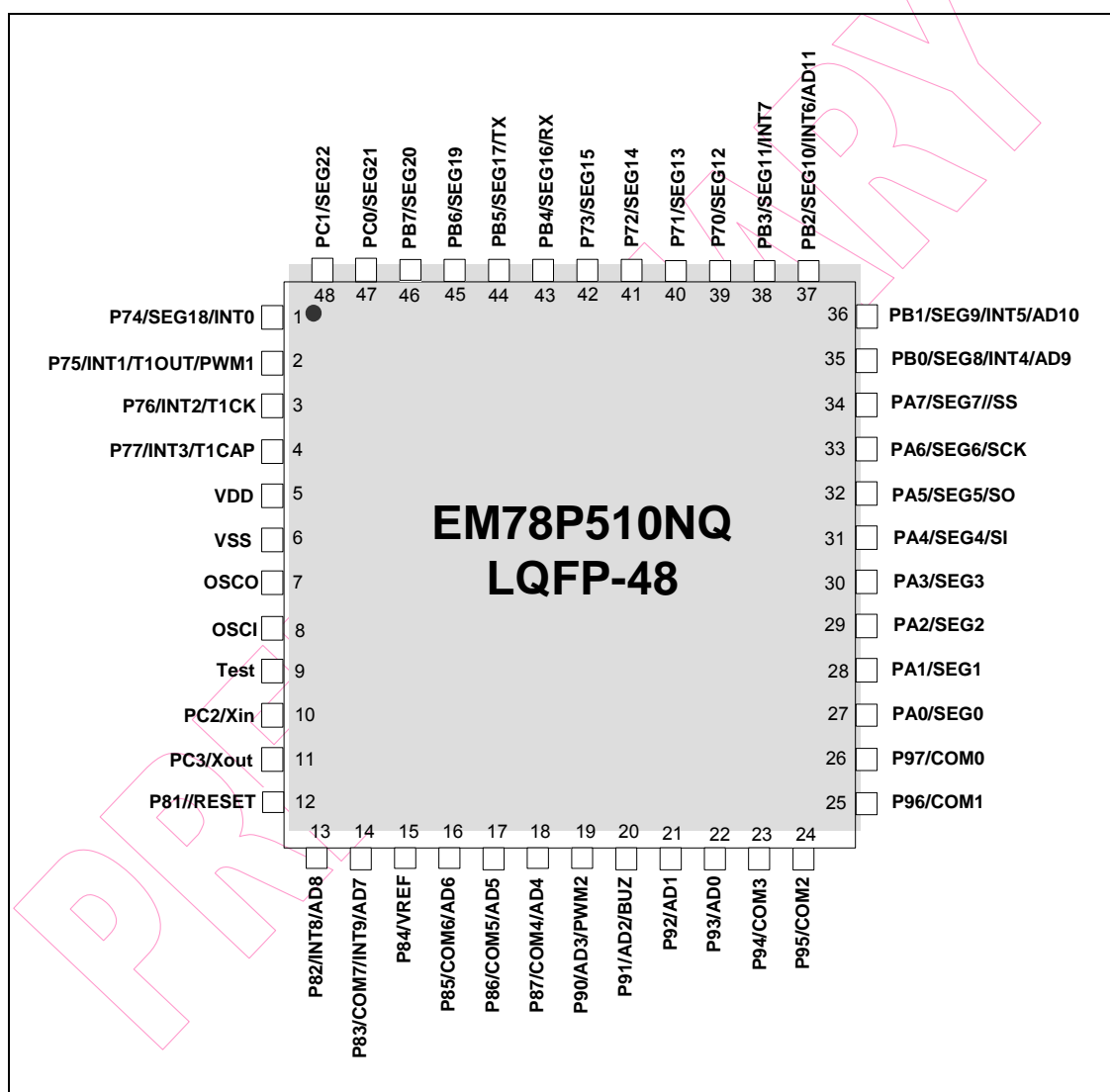


Figure 4-1a Pin Configuration for 48-pin LQFP Package

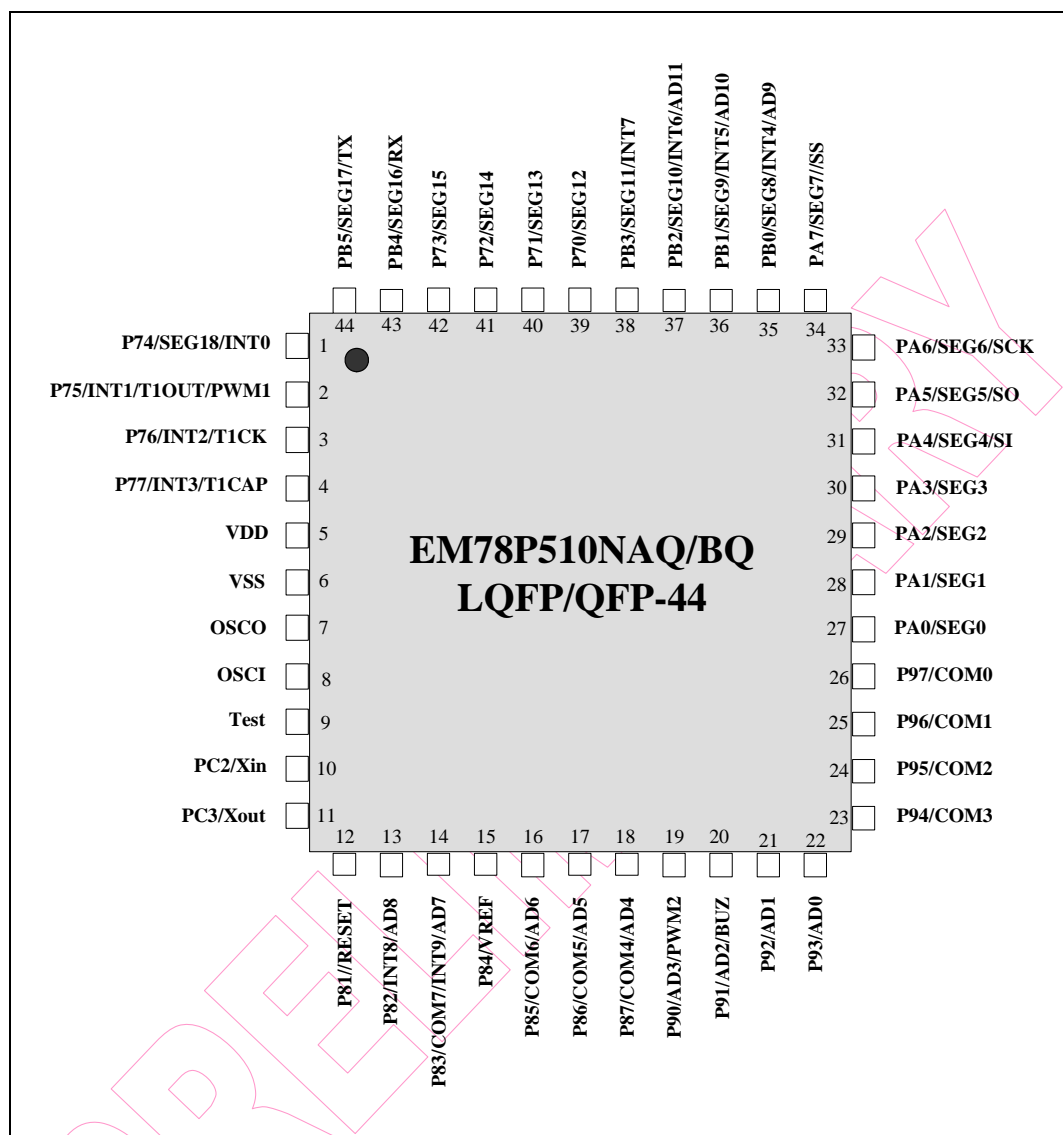


Figure 4-1b Pin Configuration for 44-pin LQFP/QFP Package

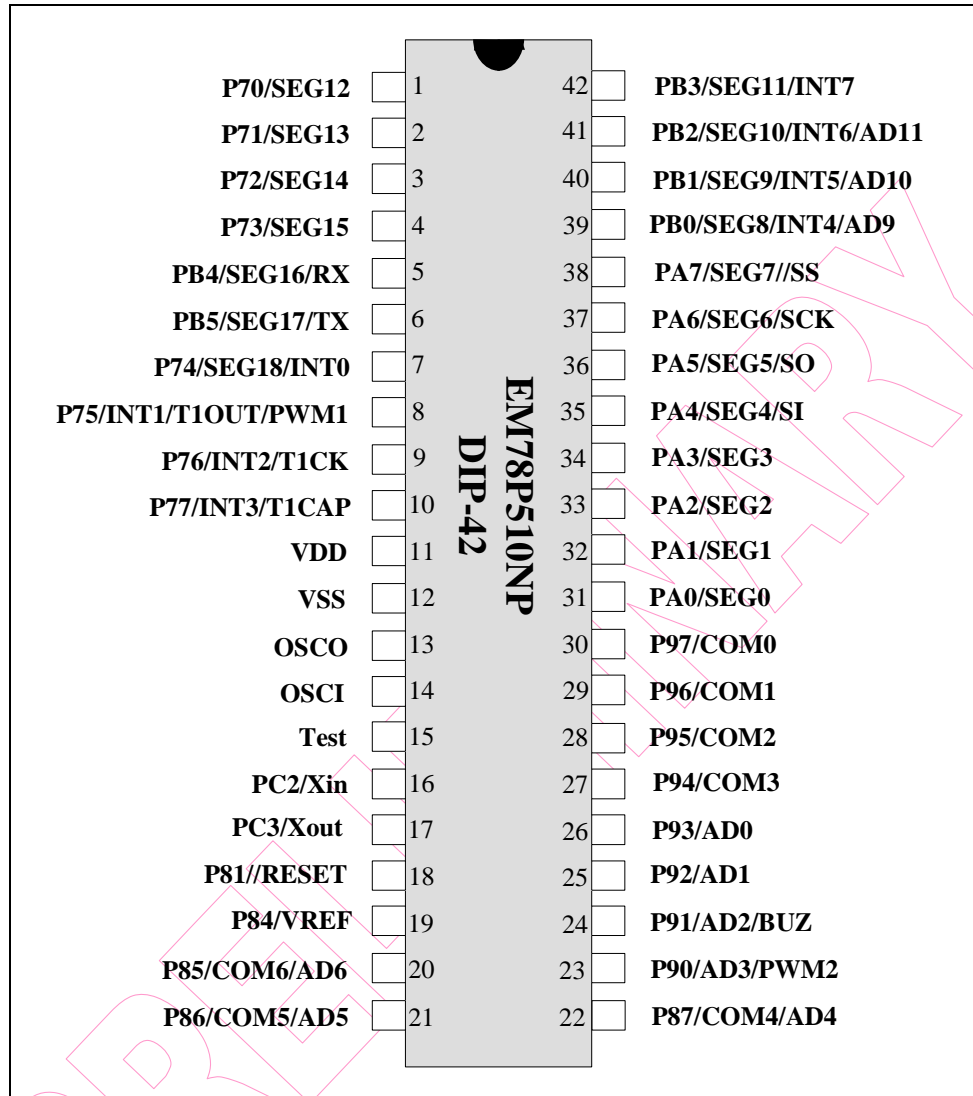


Figure 4-1c Pin Configuration for 42-pin DIP Package

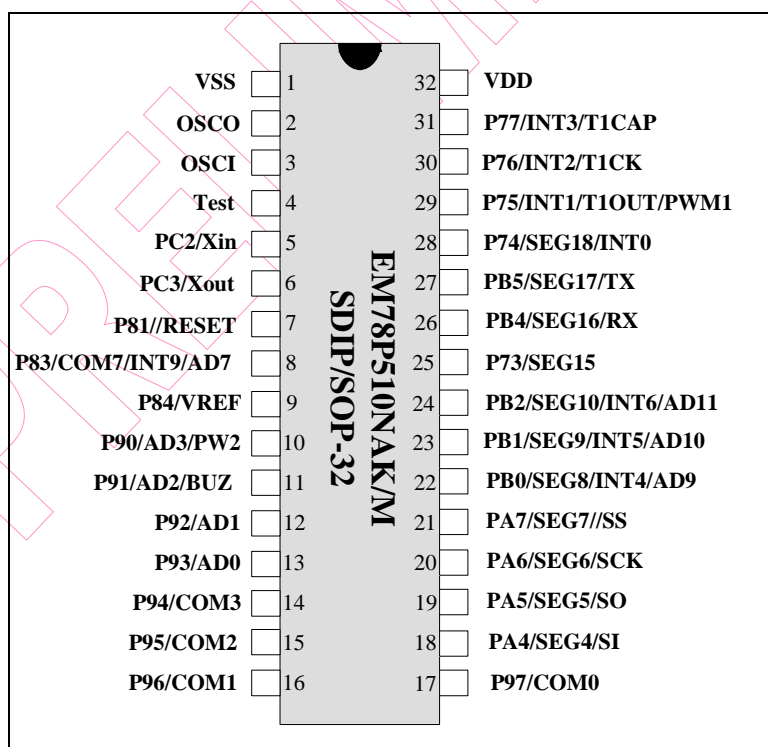
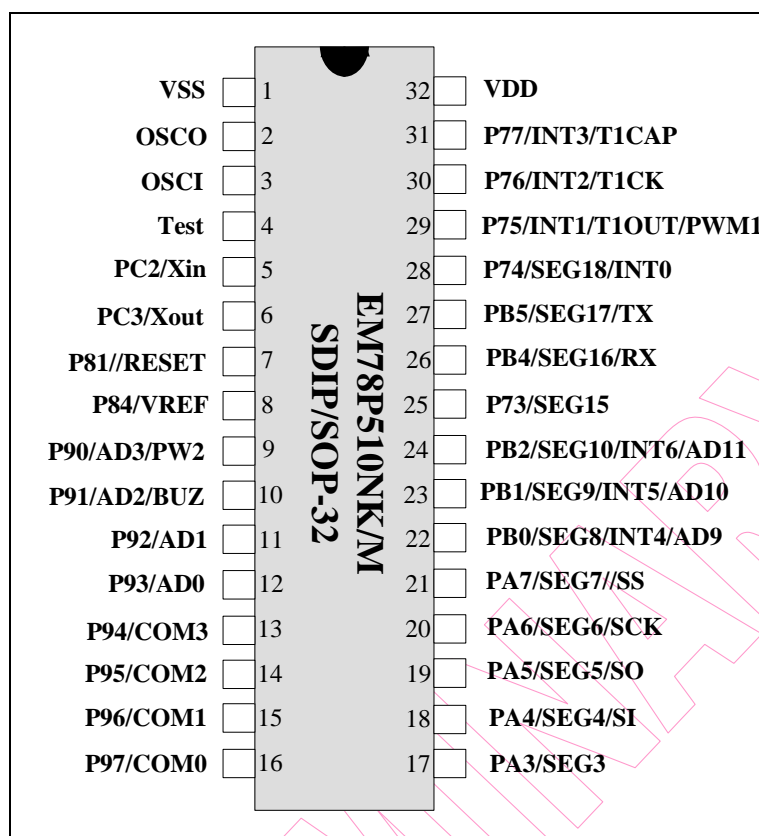


Figure 4-1d Pin Configuration for 32-pin skinny SDIP / SOP Package

5 Pin Description

Table 1 (a) LQFP-48

| Pin | Pin No. | I/O Type | Description |
|---------|-----------------|----------|--|
| P70~P77 | 1~4, 39~42 | I/O | 8-bit bidirectional I/O pins. P70 ~ P73 are pin-shared with SEG12 ~ SEG15, respectively. P74 is pin-shared with external Interrupt 0 or SEG18. P75 is pin-shared with external Interrupt 1 or T1OUT or PWM1. P76 is pin-shared with external Interrupt 2 or T1CK. P77 is pin-shared with external Interrupt 3 or T1CAP. |
| P81~P87 | 12~18 | I/O | 7-bit bidirectional I/O pins. P81 is pin-shared with RESET pin. P82 is pin-shared with Interrupt 8 or AD8 input. P83 is pin-shared with COM7 or Interrupt 9 or AD7 input. P84 is pin-shared with A/D reference input pin. P85 is pin-shared with COM6 or AD6 input. P86 is pin-shared with COM5 or AD5 input. P87 is pin-shared with COM4 or AD4 input. |
| P90~P97 | 19~26 | I/O | 8-bit bidirectional I/O pins. P90 is pin-shared with AD3 input or PWM2. P91 is pin-shared with AD2 input or BUZ. P92 ~P93 are pin-shared with AD1 ~ AD0 input, respectively. P94 ~P97 are pin-shared with COM3 ~ COM0, respectively. |
| PA0~PA7 | 27~34 | I/O | 8-bit bidirectional I/O pins. PA0 ~ PA3 are pin-shared with SEG0 ~ SEG3, respectively. PA4 is pin-shared with SEG4 or SPI SI pin. PA5 is pin-shared with SEG5 or SPI SO pin. PA6 is pin-shared with SEG6 or SPI SCK pin. PA7 is pin-shared with SEG7 or SPI /SS pin. |
| PB0~PB7 | 35~38, 43~46 | I/O | 8-bit bidirectional I/O pins. PB0 is pin-shared with SEG8 or external Interrupt 4 or AD9 input. PB1 is pin-shared with SEG9 or external Interrupt 5 or AD10 input. PB2 is pin-shared with SEG10 or external Interrupt 6 or AD11 input. PB3 is pin-shared with SEG11 or external Interrupt 7. PB4 is pin-shared with SEG16 or UART RX pin. PB5 is pin-shared with SEG17 or UART TX pin. PB6 ~ PB7 are pin-shared with SEG19 ~ SEG20, respectively. |
| PC0~PC3 | 47~48 10~11 | I/O | 4-bit bidirectional I/O pins. PC0 ~ PC1 are pin-shared with SEG21 ~ SEG22, respectively. PC2 ~PC3 are pin-shared with Xin ~ Xout, respectively. |
| OSCI | 8 | I | Crystal mode: crystal input RC mode: pull-high resistor PLL mode: connect 0.01μF capacitance to GND. Connect 0.01μF capacitor to GND and code option select PLL mode when high oscillator is not used. |
| OSCO | 7 | O | Crystal mode: crystal output RC mode: instruction clock output PLL mode: instruction clock output |
| Test | 9 | I | Test signal import pin (must be connected to VDD) |
| Xin | 10 | I | Crystal mode: input pin for sub-oscillator. Connect to a 32.768kHz crystal. RC mode: pull-high resistor |
| Xout | 11 | O | In crystal mode: connect to a 32.768kHz crystal. |
| /RESET | 12 | I | Input pin with Schmitt Trigger. If this pin remains at logic low, the controller will also remain in rest condition. |
| VDD | 5 | I | Power supply pin |
| VSS | 6 | I | System ground pin |

Table 1 (b) LQFP-44/QFP-44

| Pin | Pin No. | I/O Type | Description |
|---------|-----------------|----------|--|
| P70~P77 | 1~4, 39~42 | I/O | 8-bit bidirectional I/O pins. P70 ~ P73 are pin-shared with SEG12 ~ SEG15, respectively. P74 is pin-shared with external Interrupt 0 or SEG18. P75 is pin-shared with external Interrupt 1 or T1OUT or PWM1. P76 is pin-shared with external Interrupt 2 or T1CK. P77 is pin-shared with external Interrupt 3 or T1CAP. |
| P81~P87 | 12~18 | I/O | 7-bit bidirectional I/O pins. P81 is pin-shared with RESET pin. P82 is pin-shared with Interrupt 8 or AD8 input. P83 is pin-shared with COM7 or Interrupt 9 or AD7 input. P84 is pin-shared with A/D reference input pin. P85 is pin-shared with COM6 or AD6 input. P86 is pin-shared with COM5 or AD5 input. P87 is pin-shared with COM4 or AD4 input. |
| P90~P97 | 19~26 | I/O | 8-bit bidirectional I/O pins. P90 is pin-shared with AD3 input or PWM2. P91 is pin-shared with AD2 input or BUZ. P92 ~P93 are pin-shared with AD1 ~ AD0 input, respectively. P94 ~P97 are pin-shared with COM3 ~ COM0, respectively. |
| PA0~PA7 | 27~34 | I/O | 8-bit bidirectional I/O pins. PA0 ~ PA3 are pin-shared with SEG0 ~ SEG3, respectively. PA4 is pin-shared with SEG4 or SPI SI pin. PA5 is pin-shared with SEG5 or SPI SO pin. PA6 is pin-shared with SEG6 or SPI SCK pin. PA7 is pin-shared with SEG7 or SPI /SS pin. |
| PB0~PB5 | 35~38, 43~44 | I/O | 6-bit bidirectional I/O pins. PB0 is pin-shared with SEG8 or external Interrupt 4 or AD9 input. PB1 is pin-shared with SEG9 or external Interrupt 5 or AD10 input. PB2 is pin-shared with SEG10 or external Interrupt 6 or AD11 input. PB3 is pin-shared with SEG11 or external Interrupt 7. PB4 is pin-shared with SEG16 or UART RX pin. PB5 is pin-shared with SEG17 or UART TX pin. |
| PC2~PC3 | 10~11 | I/O | 2-bit bidirectional I/O pins. PC2 ~PC3 are pin-shared with Xin ~ Xout, respectively. |
| OSCI | 8 | I | Crystal mode: crystal input RC mode: pull-high resistor PLL mode: connect 0.01μF capacitance to GND. Connect 0.01μF capacitor to GND and code option select PLL mode when high oscillator is not used. |
| OSCO | 7 | O | Crystal mode: crystal output RC mode: instruction clock output PLL mode: instruction clock output |
| Test | 9 | I | Test signal import pin (must be connected to VDD) |
| Xin | 10 | I | Crystal mode: input pin for sub-oscillator. Connect to a 32.768kHz crystal. RC mode: pull-high resistor |
| Xout | 11 | O | Crystal mode: connect to a 32.768kHz crystal. |
| /RESET | 12 | I | Input pin with Schmitt Trigger. If this pin remains at logic low, the controller will also remain in reset condition. |
| VDD | 5 | I | Power supply pin |
| VSS | 6 | I | System ground pin |

Table 1 (c) DIP-42

| Pin | Pin No. | I/O Type | Description |
|----------------|---------------|----------|--|
| P70~P77 | 1~4, 7~10 | I/O | 8-bit bidirectional I/O pins. P70 ~ P73 are pin-shared with SEG12 ~ SEG15, respectively. P74 is pin-shared with external Interrupt 0 or SEG18. P75 is pin-shared with external Interrupt 1 or T1OUT or PWM1. P76 is pin-shared with external Interrupt 2 or T1CK. P77 is pin-shared with external Interrupt 3 or T1CAP. |
| P81 P84~P87 | 18~22 | I/O | 5-bit bidirectional I/O pins. P81 is pin-shared with RESET pin. P84 is pin-shared with A/D reference input pin. P85 is pin-shared with COM6 or AD6 input. P86 is pin-shared with COM5 or AD5 input. P87 is pin-shared with COM4 or AD4 input. |
| P90~P97 | 23~30 | I/O | 8-bit bidirectional I/O pins. P90 is pin-shared with AD3 input or PWM2. P91 is pin-shared with AD2 input or BUZ. P92 ~P93 are pin-shared with AD1 ~ AD0 input, respectively. P94 ~P97 are pin-shared with COM3 ~ COM0, respectively. |
| PA0~PA7 | 31~38 | I/O | 8-bit bidirectional I/O pins. PA0 ~ PA3 are pin-shared with SEG0 ~ SEG3, respectively. PA4 is pin-shared with SEG4 or SPI SI pin. PA5 is pin-shared with SEG5 or SPI SO pin. PA6 is pin-shared with SEG6 or SPI SCK pin. PA7 is pin-shared with SEG7 or SPI /SS pin. |
| PB0~PB5 | 39~42, 5~6 | I/O | 6-bit bidirectional I/O pins. PB0 is pin-shared with SEG8 or external Interrupt 4 or AD9 input. PB1 is pin-shared with SEG9 or external Interrupt 5 or AD10 input. PB2 is pin-shared with SEG10 or external Interrupt 6 or AD11 input. PB3 is pin-shared with SEG11 or external Interrupt 7. PB4 is pin-shared with SEG16 or UART RX pin. PB5 is pin-shared with SEG17 or UART TX pin. |
| PC2~PC3 | 16~17 | I/O | 2-bit bidirectional I/O pins. PC2 ~PC3 are pin-shared with Xin ~ Xout, respectively. |
| OSCI | 14 | I | Crystal mode: crystal input RC mode: pull-high resistor PLL mode: connect 0.01 μ F capacitance to GND. Connect 0.01 μ F capacitor to GND and code option select PLL mode when high oscillator is not used. |
| OSCO | 13 | O | Crystal mode: crystal output RC mode: instruction clock output PLL mode: instruction clock output |
| Test | 15 | I | Test signal import pin (must be connected to VDD) |
| Xin | 16 | I | Crystal mode: input pin for sub-oscillator. Connect to a 32.768kHz crystal. RC mode: pull-high resistor |
| Xout | 17 | O | Crystal mode: connect to a 32.768kHz crystal. |
| /RESET | 18 | I | Input pin with Schmitt Trigger. If this pin remains at logic low, the controller will also remain in reset condition. |
| VDD | 11 | I | Power supply pin |
| VSS | 12 | I | System ground pin |

Table 1 (d) SDIP-32/SOP-32

| Pin | Pin No. | I/O Type | Description |
|------------------------|-----------------|----------|--|
| P73, P74~P77 | 25, 28~31 | I/O | 5-bit bidirectional I/O pins. P73 is pin-shared with SEG15. P74 is pin-shared with external Interrupt 0 or SEG18. P75 is pin-shared with external Interrupt 1 or T1OUT or PWM1. P76 is pin-shared with external Interrupt 2 or T1CK. P77 is pin-shared with external Interrupt 3 or T1CAP. |
| P81//RESET P84/VREF | 7 8 | I/O | 2-bit bidirectional I/O pins. P81 is pin-shared with RESET pin. P83 can be used as COM7 or Interrupt 9 or AD7 input.(for EM78P510NAK/M use only) P84 is pin-shared with A/D reference input pin. |
| P90~P97 | 23~30 | I/O | 8-bit bidirectional I/O pins. P90 is pin-shared with AD3 input or PWM2. P91 is pin-shared with AD2 input or BUZ. P92 ~P93 are pin-shared with AD1 ~ AD0 input, respectively. P94 ~P97 are pin-shared with COM3 ~ COM0, respectively. |
| PA3~PA7 | 17~21 | I/O | 5-bit bidirectional I/O pins. PA3 is pin-shared with SEG3 (for EM78P510NK/M only) PA4 is pin-shared with SEG4 or SPI SI pin. PA5 is pin-shared with SEG5 or SPI SO pin. PA6 is pin-shared with SEG6 or SPI SCK pin. PA7 is pin-shared with SEG7 or SPI /SS pin. |
| PB0~PB2 PB4~PB5 | 22~24, 26~27 | I/O | 5-bit bidirectional I/O pins. PB0 is pin-shared with SEG8 or external Interrupt 4 or AD9 input. PB1 is pin-shared with SEG9 or external Interrupt 5 or AD10 input. PB2 is pin-shared with SEG10 or external Interrupt 6 or AD11 input. PB3 is pin-shared with SEG11 or external Interrupt 7. PB4 is pin-shared with SEG16 or UART RX pin. PB5 is pin-shared with SEG17 or UART TX pin. |
| PC2~PC3 | 5~6 | I/O | 2-bit bidirectional I/O pins. PC2 ~PC3 are pin-shared with Xin ~ Xout, respectively. |
| OSCI | 3 | I | Crystal mode: crystal input RC mode: pull-high resistor PLL mode: connect 0.01μF capacitance to GND. Connect 0.01μF capacitor to GND and code option select PLL mode when high oscillator is not used. |
| OSCO | 2 | O | Crystal mode: crystal output RC mode: instruction clock output PLL mode: instruction clock output |
| Test | 45 | I | Test signal import pin (must be connected to VDD) |
| Xin | 5 | I | Crystal mode: input pin for sub-oscillator. Connect to a 32.768kHz crystal. RC mode: pull-high resistor |
| Xout | 6 | O | Crystal mode: connect to a 32.768kHz crystal. |
| /RESET | 7 | I | Input pin with Schmitt Trigger. If this pin remains at logic low, the controller will also remain in reset condition. |
| VDD | 32 | I | Power supply pin |
| VSS | 1 | I | System ground pin |

5 Functional Block Diagram

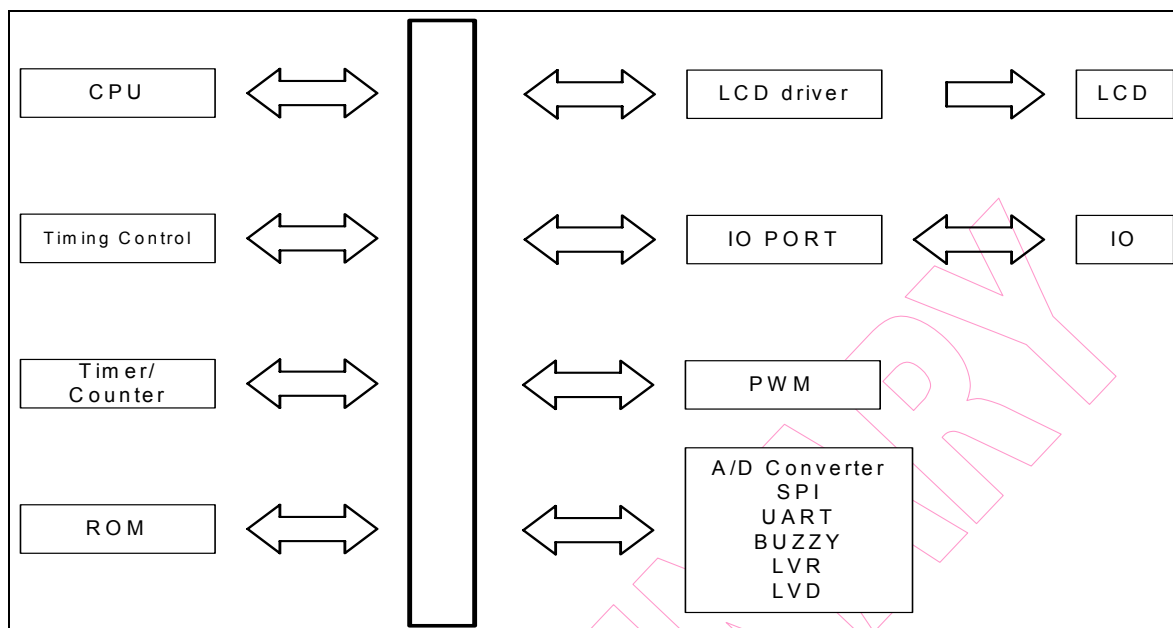


Figure 5-1a EM78P510N Block Diagram (Overview)

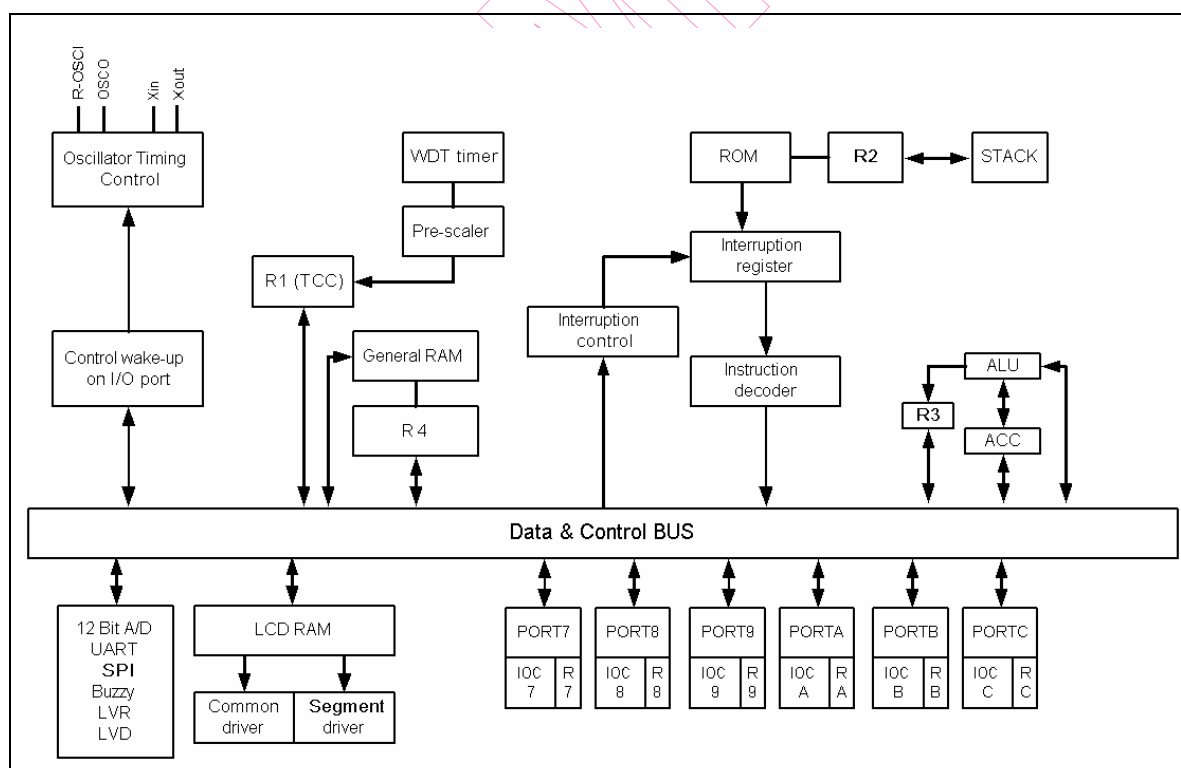


Figure 5-1b EM78P510N Block Diagram (Detailed)

6 Function Description

6.1 Register Configuration

6.1.1 R PAGE Register Configuration

| Bank0 | Bank1 | Bank2 | Bank3 | Bank4 | Bank5 | Bank6 |
|------------|---------------------|-------|-------|--------|--------|--------|
| R0 (IAR) | | | | | | |
| R1 (TCC) | | | | | | |
| R2 (PC) | | | | | | |
| R3 (SR) | | | | | | |
| R4 (RSR) | | | | | | |
| RBSR | LCDCCR | T1CR | URC | LEDDCR | | |
| RPSR | LCDAR | TSR | URS | WBCR | URC2 | LVRCR |
| PORT7 | LCDDBR | T1PD | URRD | IOC7 | P7PHCR | P7ODCR |
| PORT8 | LCDVCR | T1TD | URTD | IOC8 | P8PHCR | P8ODCR |
| PORT9 | LCDCCR | T2CR | ADCR | IOC9 | P9PHCR | P9ODCR |
| PORTA | LCDSCR0 | T2PD | ADICH | IOCA | PAPHCR | PAODCR |
| PORTB | LCDSCR1 | T2TD | ADICL | IOCB | PBPHCR | PBODCR |
| SCCR | LCDSCR2 | SPIS | ADDH | IOCC | PCPHCR | PORTC |
| TWTCR | | SPIC | ADDL | | | |
| IMR | EIMR | SPIR | EIESH | | | |
| ISR | EISR | SPIW | EIESL | WKCR | | |
| R10 | | | | | | |
| . | | | | | | |
| . | | | | | | |
| . | | | | | | |
| R20 | General Purpose Ram | | Bank7 | | | |
| . | | | R20 | | | |
| . | | | . | | | |
| . | | | . | | | |
| R3F | | | R3F | | | |

Figure 6-1 Data memory Configuration

6.2 Register Operations

6.2.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

6.2.2 R1 (TCC)

Incremented by the main oscillator clock (Fm) or sub oscillator clock (Fs) (controlled by TWTCR register). Written and read by the program as any other register.

6.2.3 R2 (Program Counter)

The structure is depicted in Fig. 6-2. Generates $8K \times 13$ on-chip ROM addresses to the relative programming instruction codes.

"JMP" instruction allows the direct loading of the low 10 program counter bits.

"CALL" instruction loads the low 10 bits of the PC and PC+1, and then push into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2, A" allows the loading of an address from the A register to the PC, and contents of the ninth and tenth bits don't change.

"ADD R2, A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits don't change.

The most significant bit (A10~A11) will be loaded with the contents of Bit PS0~PS2 in the status register (R6) upon the execution of a "JMP", "CALL" instruction.

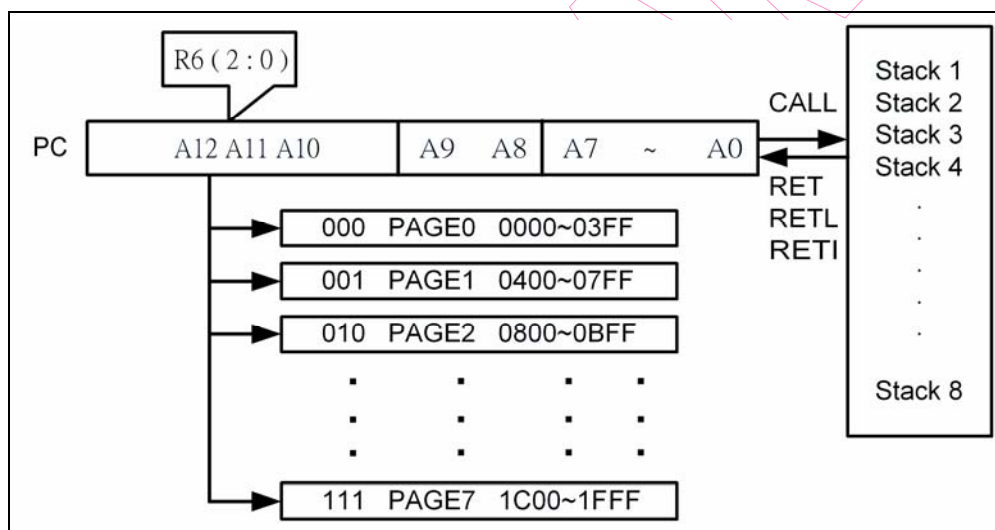


Figure 6-2 Program Counter Organization

User can use Long jump (LJMP) or long call (LCALL) instructions to program user's code. And the program page is maintained by ELAN's compiler. It will change user's program by inserting instructions within the program.

6.2.4 R3 (Status, Page Selection)

■ Status Flag, Page Selection Bits

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|--------|--------|-------|-------|-------|-------|-------|
| LV DEN | LV DS1 | LV DS0 | T | P | Z | DC | C |

Bit 7 (LV DEN): Voltage Detect Enable Bit

0 : No action

1 : Voltage detect enabled

Bits 6~5 (LVDS1~LVDS0): Detect Voltage Select Bits

| LVDS1 | LVDS0 | Detect Voltage |
|-------|-------|----------------|
| 0 | 0 | 2.4V |
| 0 | 1 | 2.7V |
| 1 | 0 | 3.3V |
| 1 | 1 | 3.9V |

Bit 4 (T): Time-out bit

Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

Bit 3 (P): Power down bit

Set to "1" during power on or by a "WDTC" command and reset to "0" by a "SLEP" command.

| Event | T | P | Remarks |
|-----------------------------------|---|---|----------------|
| WDT wakes up from sleep mode | 0 | 0 | |
| WDT times out (not in sleep mode) | 0 | 1 | |
| /RESET wakes up from sleep | 1 | 0 | |
| Power up | 1 | 1 | |
| Low pulse on /RESET | × | × | × = don't care |

Bit 2 (Z): Zero flag

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.2.5 R4 (RAM Select Register)

Bit 7 (VDB): Voltage Detector. This is a read only bit. When VDD pin voltage is lower than Vdet (select by LVDS0~LVDS1) this bit will be cleared.

0 : low voltage is detected

1 : low voltage is not detected or LVD function is disabled

Bit 6 (BNC): Bank Control Register.

0 : allow to access only Bank 0 registers

1 : Allow to access all registers of any Bank

Bits 5~0: are used to select up to 64 registers in the indirect addressing mode.

See the configuration of the data memory. User can use BANK instruction to change bank.

6.2.6 Bank 0 R5 (RAM Bank Select Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | 0 | 0 | BS2 | BS1 | BS0 |

Bits 7~3: Reserved

Bits 2~0 (BS2~BS0): RAM Bank Select Register

| BS2 | BS1 | BS0 | RAM Bank |
|-----|-----|-----|----------|
| 0 | 0 | 0 | Bank 0 |
| 0 | 0 | 1 | Bank 1 |
| : | : | : | : |
| : | : | : | : |
| 1 | 1 | 1 | Bank 7 |

6.2.7 Bank 0 R6 (Program Page Select Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | 0 | 0 | PS2 | PS1 | PS0 |

Bits 7~3: Reserved

Bits 2~0 (PS2~PS0): ROM Page Select Register

| PS2 | PS1 | PS0 | ROM PAGE |
|-----|-----|-----|----------|
| 0 | 0 | 0 | Page 0 |
| 0 | 0 | 1 | Page 1 |
| : | : | : | : |
| : | : | : | : |
| 1 | 1 | 1 | Page 7 |

6.2.8 Bank 0 R7 (Port 7)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R77 | R76 | R75 | R74 | R73 | R72 | R71 | R70 |

Bits 7~0 (R77~R70): Port 7 8-bit I/O Registers.

6.2.9 Bank 0 R8 (Port 8)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R87 | R86 | R85 | R84 | R83 | R82 | R81 | 0 |

Bits 7~1 (R87~R81): Port 8 7-bit I/O Registers.

Bit 0: Reserved

6.2.10 Bank 0 R9 (Port 9)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R97 | R96 | R95 | R94 | R93 | R92 | R91 | R90 |

Bits 7~0 (R97~R90): Port 9 8-bit I/O Registers.

6.2.11 Bank 0 RA (Port A)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 |

Bits 7~0 (RA7~RA0): Port A 8-bit I/O Registers

6.2.12 Bank 0 RB (Port B)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |

Bits 7~0 (RB7~RB0): Port B 8-bit I/O Registers

6.2.13 Bank 0 RC SCCR (System Clock Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | CLK2 | CLK1 | CLK0 | IDLE | 0 | 0 | CPUS |

Bit 7: Reserved, fixed to "0"

Bits 6~4 (CLK2~CLK0): Main Clock Select Bit for PLL Mode (code option select)

| CLK2 | CLK1 | CLK0 | Main Clock | Ex: $F_s=32.768K$ |
|------|------|------|-------------------|-------------------|
| 0 | 0 | 0 | $F_s \times 122$ | 3.997 MHz |
| 0 | 0 | 1 | $F_s \times 61$ | 1.998 MHz |
| 0 | 1 | 0 | $F_s \times 61/2$ | 0.999 MHz |
| 0 | 1 | 1 | $F_s \times 61/4$ | 499.7 kHz |
| 1 | 0 | 0 | $F_s \times 244$ | 7.995 MHz |
| 1 | 0 | 1 | $F_s \times 366$ | 11.99 MHz |
| 1 | 1 | × | $F_s \times 488$ | 15.99 MHz |

Bit 3 (IDLE): Idle Mode Enable Bit. This bit will decide SLEEP instruction which mode to go.

IDLE="0"+SLEEP instruction → sleep mode

IDLE="1"+SLEEP instruction → idle mode

Bits 2~1: Reserved, fixed to "0"

Bit 0 (CPUS): CPU Oscillator Source Select, 0/1 → sub-oscillator (fs)/ main oscillator (fosc) When CPUS=0, the CPU oscillator select sub-oscillator and the main oscillator is stopped.

CPU Operation Mode

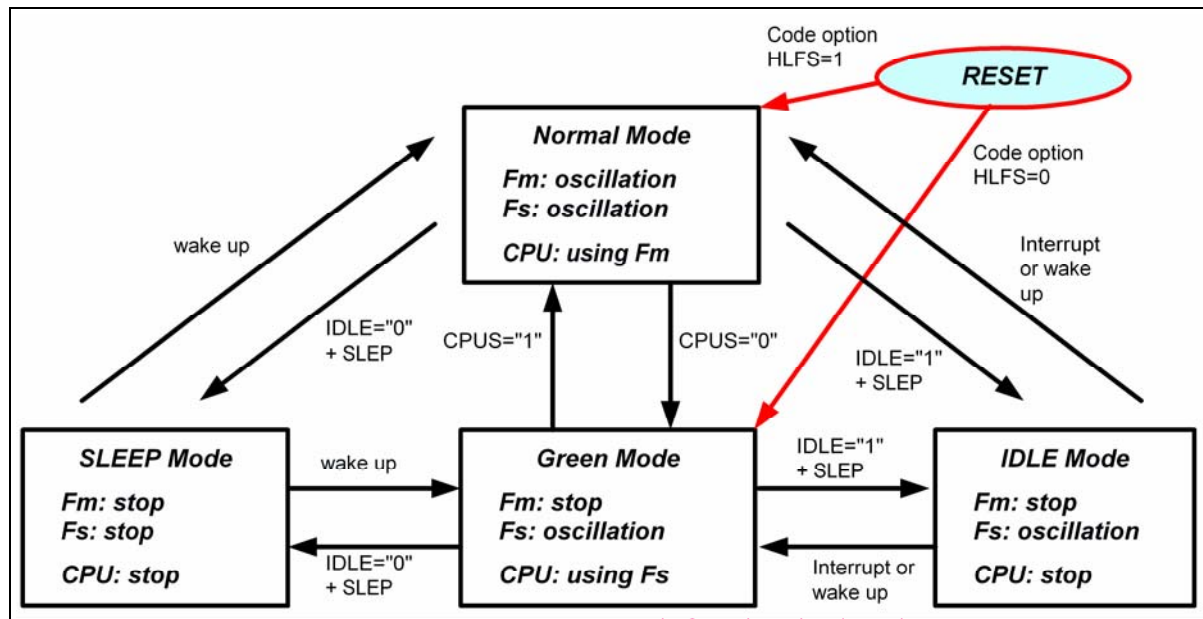


Figure 6-3 CPU operation mode

6.2.14 Bank 0 RD TWTCR (TCC and WDT Timer Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WDTE | WPSR2 | WPSR1 | WPSR0 | TCCS | TPSR2 | TPSR1 | TPSR0 |

Bit 7 (WDTE): Watchdog Timer Enable. This control bit is used to enable the watchdog timer.

0 : Disable WDT function

1 : Enable WDT function

Bits 6~4 (WPSR2~WPSR0): WDT Prescaler Bits

| WPSR2 | WPSR1 | WPSR0 | Prescaler |
|-------|-------|-------|---------------|
| 0 | 0 | 0 | 1:1 (Default) |
| 0 | 0 | 1 | 1 : 2 |
| 0 | 1 | 0 | 1 : 4 |
| 0 | 1 | 1 | 1 : 8 |
| 1 | 0 | 0 | 1 : 16 |
| 1 | 0 | 1 | 1 : 32 |
| 1 | 1 | 0 | 1 : 64 |
| 1 | 1 | 1 | 1 : 128 |

Bit 3 (TCCS): TCC Clock Source Select Bit

0 : Fm (main clock).

1 : Fs (sub clock: 32.768kHz)

Bits 2~0 (TPSR2~TPSR0): TCC Prescaler Bits

| TPSR2 | TPSR1 | TPSR0 | Prescaler |
|-------|-------|-------|---------------|
| 0 | 0 | 0 | 1:2 (Default) |
| 0 | 0 | 1 | 1 : 4 |
| 0 | 1 | 0 | 1 : 8 |
| 0 | 1 | 1 | 1 : 16 |
| 1 | 0 | 0 | 1 : 32 |
| 1 | 0 | 1 | 1 : 64 |
| 1 | 1 | 0 | 1 : 128 |
| 1 | 1 | 1 | 1 : 256 |

6.2.15 Bank 0 RE IMR (Interrupt Mask Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| T1IE | LVDIE | ADIE | SPIE | URTIE | EXIE9 | EXIE8 | TCIE |

Bits 7~0 (T1IE~TCIE): Interrupt Enable Bit. Enable interrupt source respectively.

0 : Disable interrupt

1 : Enable interrupt

External Interrupt

| INT pin | Secondary function Pin | Enable Condition | Edge | Digital Noise Reject |
|---------|------------------------|------------------|-------------------|----------------------|
| INT8 | P82, AD8 | ENI+EXIE8(IMR1) | Rising or Falling | 2/Fc |
| INT9 | P83, COM7, AD7 | ENI+EXIE9(IMR2) | Rising or Falling | 2/Fc |

INT8~INT9: Pulse less than 2/Fc is eliminated as noise. Pulse less than 5/Fc is eliminated as noise.

6.2.16 Bank 0 RF ISR (Interrupt Status Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| T1IF | LVDIF | ADIF | SPIF | URTIF | EXIF9 | EXIF8 | TCIF |

These bits are set to "1" when interrupt occurs respectively.

Bit 7 (T1IF): Interrupt Flag of Timer 1 Interrupt

Bit 6 (LVDIF): Interrupt Flag of Low Voltage Detector Interrupt

Bit 5 (ADIF): Interrupt Flag of A/D Convert Complete

Bit 4 (SPIIF): Interrupt Flag of SPI Transfer Complete

Bit 3 (URTIF): Interrupt Flag of UART Transfer Complete

Bit 2 (EXIF9): Interrupt Flag of External Interrupt 9 occurs

Bit 1 (EXIF8): Interrupt Flag of External Interrupt 8 occurs.

Bit 0 (TCIF): Interrupt Flag of TCC overflow

6.2.17 Bank 1 R5 LCDCR (LCD Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|---------|-------|-------|-------|-------|-------|-------|
| LCDEN | LCDTYPE | BS1 | BS0 | DS1 | DS0 | LCDF1 | LCDF0 |

Bit 7 (LCDEN): LCD Enable Select Bit

- 0 : LCD disabled. All common/segment outputs are set to VDD level.
- 1 : LCD enabled

Bit 6 (LCDTYPE): LCD Drive Waveform Type Select Bit

- 0 : A type wave
- 1 : B type wave

Bits 5~4 (BS1~BS0): LCD Bias Select Bits

| BS1 | BS0 | LCD Bias Select |
|-----|-----|-----------------|
| 0 | 0 | 1/2 Bias |
| 0 | 1 | 1/3 Bias |
| 1 | X | 1/4 Bias |

Bits 3~2 (DS1~DS0): LCD Duty Select Bits

| DS1 | DS0 | LCD Duty |
|-----|-----|----------|
| 0 | 0 | Static |
| 0 | 1 | 1/3 Duty |
| 1 | 0 | 1/4 Duty |
| 1 | 1 | 1/8 Duty |

Bits 1~0 (LCDF1~LCDF0): LCD Frame Frequency Control Bits

| LCD Frame Frequency (e.g. $F_s=32.768K$) | | | | | |
|---|-------|-----------------------------|-----------------------------|-----------------------------|----------------------------|
| LCDF1 | LCDF0 | Static | 1/3 Duty | 1/4 Duty | 1/8 Duty |
| 0 | 0 | $F_s/(512 \times 1) = 64.0$ | $F_s/(172 \times 3) = 63.5$ | $F_s/(128 \times 4) = 64$ | $F_s/(64 \times 8) = 64.0$ |
| 0 | 1 | $F_s/(560 \times 1) = 58.5$ | $F_s/(188 \times 3) = 58$ | $F_s/(140 \times 4) = 58.5$ | $F_s/(70 \times 8) = 58.5$ |
| 1 | 0 | $F_s/(608 \times 1) = 53.9$ | $F_s/(204 \times 3) = 53.5$ | $F_s/(152 \times 4) = 53.9$ | $F_s/(76 \times 8) = 53.9$ |
| 1 | 1 | $F_s/(464 \times 1) = 70.6$ | $F_s/(156 \times 3) = 70$ | $F_s/(116 \times 4) = 70.6$ | $F_s/(58 \times 8) = 70.6$ |

6.2.18 Bank 1 R6 LCDAR (LCD Address Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|--------|--------|--------|--------|--------|
| 0 | 0 | 0 | LCD_A4 | LCD_A3 | LCD_A2 | LCD_A1 | LCD_A0 |

Bits 7~5: Reserved

Bits 4~0 (LCD_A4~LCD_A0): LCD RAM Address

| R6 (LCD Address) | R7 (LCD Data Buffer) | | | | | | | | Segment |
|------------------------|----------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|---------|
| | Bit 7 (LCD_D7) | Bit 6 (LCD_D6) | Bit 5 (LCD_D5) | Bit 4 (LCD_D4) | Bit 3 (LCD_D3) | Bit 2 (LCD_D2) | Bit 1 (LCD_D1) | Bit 0 (LCD_D0) | |
| 00H | | | | | | | | | SEG0 |
| 01H | | | | | | | | | SEG1 |
| 02H | | | | | | | | | SEG2 |
| | | | | | | | | | |
| 14H | | | | | | | | | SEG20 |
| 15H | | | | | | | | | SEG21 |
| 16H | | | | | | | | | SEG22 |
| Common | COM7 | COM6 | COM5 | COM4 | COM3 | COM2 | COM1 | COM0 | |

6.2.19 Bank 1 R7 LCDBR (LCD Data Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| LCD_D 7 | LCD_D 6 | LCD_D 5 | LCD_D 4 | LCD_D 3 | LCD_D 2 | LCD_D 1 | LCD_D 0 |

Bit 7~0 (LCD_D7~LCD_D0): LCD RAM Data Transfer Register

6.2.20 Bank 1 R8 LCDVCR (LCD Voltage Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|--------|--------|--------|
| 0 | 0 | 0 | LCDC1 | LCDC0 | LCDVC2 | LCDVC1 | LCDVC0 |

Bits 7~5: Reserved

Bits 4~3 (LCDC1~LCDC0): LCD Clock

| LCDC1 | LCDC0 | F _m | F _{LCD} |
|-------|-------|----------------|--------------------------------|
| 0 | 0 | 16M | F _c /2 ⁹ |
| 0 | 1 | 8M | F _c /2 ⁸ |
| 1 | 0 | 4M | F _c /2 ⁷ |
| 1 | 1 | 2M | F _c /2 ⁶ |

When the main oscillator operates in crystal mode and the sub-oscillator does not, it's a must to set these two bits for the LCD clock.

Bits 2~0 (LCDVC2~LCDVC0): LCD Voltage Control Bits

| LCDVC2 | LCDVC1 | LCDVC0 | Output |
|--------|--------|--------|---------------|
| 0 | 0 | 0 | 0.4VDD ~ VDD |
| 0 | 0 | 1 | 0.34VDD ~ VDD |
| 0 | 1 | 0 | 0.26VDD ~ VDD |
| 0 | 1 | 1 | 0.18VDD ~ VDD |
| 1 | 0 | 0 | 0.13VDD ~ VDD |
| 1 | 0 | 1 | 0.07VDD ~ VDD |
| 1 | 1 | 0 | 0.04VDD ~ VDD |
| 1 | 1 | 1 | 0V ~ VDD |

6.2.21 Bank 1 R9 LCDCCR (LCD Com Control Register 3)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| COM7 | COM6 | COM5 | COM4 | COM3 | COM2 | COM1 | COM0 |

Bits 7~0 (COM7~COM0): LCD Com 7~0 Control Bits

0 : Disable, functions as normal I/O or other functions

1 : Enable, functions as LCD common driver pins

6.2.22 Bank 1 RA LCDSCR0 (LCD Segment Control Register 0)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SEG7 | SEG6 | SEG5 | SEG4 | SEG3 | SEG2 | SEG1 | SEG0 |

Bits 7~0 (SEG7~SEG0): LCD Segments 7~0 Control Bits

0 : Disable, functions as normal I/O or other functions

1 : Enable, functions as LCD common driver pins

6.2.23 Bank 1 RB LCDSCR1 (LCD Segment Control Register 1)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SEG15 | SEG14 | SEG13 | SEG12 | SEG11 | SEG10 | SEG9 | SEG8 |

Bits 7~0 (SEG15~SEG8): LCD Segments 15~8 Control Bits

0 : Disable, functions as normal I/O or other functions

1 : Enable, functions as LCD common driver pins

6.2.24 Bank 1 RC LCDSCR2 (LCD Segment Control Register 2)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| - | SEG22 | SEG21 | SEG20 | SEG19 | SEG18 | SEG17 | SEG16 |

Bit 7: Reserved

Bits 6~0 (SEG22~SEG16): LCD Segment 22~16 Control Bits

0 : Disable, functions as normal I/O or other functions

1 : Enable, functions as LCD common driver pins

6.2.25 Bank 1 RE EIMR (External Interrupt Mask Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EXIE7 | EXIE6 | EXIE5 | EXIE4 | EXIE3 | EXIE2 | EXIE1 | EXIE0 |

Bits 7~0 (EXIE7~EXIE0): Interrupt Enable Bit. Enable interrupt source respectively.

External interrupt

| INT Pin | Secondary Function Pin | Enable Condition | Edge | Digital Noise Reject |
|---------|------------------------|------------------|-------------------|----------------------|
| INT7 | PB3, SEG11 | ENI+EXIE7(EIMR7) | Rising or Falling | 2/Fc |
| INT6 | PB2, SEG10, AD11 | ENI+EXIE6(EIMR6) | Rising or Falling | 2/Fc |
| INT5 | PB1, SEG9, AD10 | ENI+EXIE5(EIMR5) | Rising or Falling | 2/Fc |
| INT4 | PB0, SEG8, AD9 | ENI+EXIE4(EIMR4) | Rising or Falling | 2/Fc |
| INT3 | P77, T1CAP | ENI+EXIE3(EIMR3) | Rising or Falling | 2/Fc |
| INT2 | P76, T1CK | ENI+EXIE2(EIMR2) | Rising or Falling | 2/Fc |
| INT1 | P75, T1OUT, PWM1 | ENI+EXIE1(EIMR1) | Rising or Falling | 2/Fc |
| INT0 | P74, SEG18 | ENI+EXIE0(EIMR0) | Rising or Falling | 2/Fc |

INT7~INT0: Pulse less than 2/Fc is eliminated as noise. Pulse less than 5/Fc is eliminated as noise.

6.2.26 Bank 1 RF EISR (External Interrupt Status Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EXIF7 | EXIF6 | EXIF5 | EXIF4 | EXIF3 | EXIF2 | EXIF1 | EXIF0 |

These bits are set to "1" when interrupt occurs respectively.

Bits 7~0 (EXIF7~EXIF0): Interrupt Flag when External Interrupt 7~0 occur

6.2.27 Bank 2 R5 T1CR (Timer1 Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TIS1 | TIS0 | T1MS2 | T1MS1 | T1MS0 | T1P2 | T1P1 | T1P0 |

Bits 7~6 (TIS1~ TIS0): Timer 1 and Timer 2 Interrupt Type Select Bits. These two bits are used when the Timer operates in PWM mode.

| TIS1 | TIS0 | Timer 1 and Timer 2 Interrupt Type Select |
|------|------|---|
| 0 | 0 | T1PD underflow |
| 0 | 1 | T1TD underflow |
| 1 | X | T1PD and T1TD underflow |

Bits 5~3 (T1MS2~T1MS0): Timer 1 Operation Mode Select Bits

| T1MS2 | T1MS1 | T1MS0 | Timer 1 Mode Select |
|-------|-------|-------|---------------------------|
| 0 | 0 | 0 | Timer 1 |
| 0 | 0 | 1 | T1OUT Mode |
| 0 | 1 | 0 | Capture Mode Rising Edge |
| 0 | 1 | 1 | Capture Mode Falling Edge |
| 1 | 0 | 0 | UART Baud Rate Generator |
| 1 | 0 | 1 | PWM 1 |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

Bits 2~0 (T1P2~T1P0): Timer 1 Prescaler Bits

| T1P2 | T1P1 | T1P0 | Prescaler |
|------|------|------|---------------|
| 0 | 0 | 0 | 1:2 (Default) |
| 0 | 0 | 1 | 1 : 4 |
| 0 | 1 | 0 | 1 : 8 |
| 0 | 1 | 1 | 1 : 16 |
| 1 | 0 | 0 | 1 : 32 |
| 1 | 0 | 1 | 1 : 64 |
| 1 | 1 | 0 | 1 : 128 |
| 1 | 1 | 1 | 1 : 256 |

6.2.28 Bank 2 R6 TSR (Timer Status Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|--------|--------|-------|-------|-------|-------|
| T1MOD | TRCB | T1CSS1 | T1CSS0 | T2CSS | T1EN | T1OMS | T1OC |

Bit 7 (T1MOD): Timer Operates Mode Select Bit

- 0 : Two 8-bit Timer
- 1 : Timer 1 and Timer 2 cascade to one 16-bit Timer

NOTE

By setting T1MOD to "1", Timer can cascade to one 16-bit Timer. This 16 bits Timer is controlled by Time r1, including enable, clock source and prescaler. Timer 1 is MSB and Timer 2 is LSB in value of period and duty.

Bit 6 (TRCB): Timers 1, 2 Read Control Bit

- 0: When this bit set to 0, read data from T1PD or T2PD.
- 1: When this bit set to 1, read data from T1PD or T2PD, but this is value of timer counter.

Bits 5~4 (T1CSS1~T1CSS0): Timer 1 Clock Source Select Bits

| T1CSS1 | T1CSS0 | Timer 1 Clock Source Select |
|--------|--------|-----------------------------|
| 0 | 0 | Fm |
| 0 | 1 | Fs |
| 1 | X | T1CK |

Bit 3 (T2CSS): Timer 2 Clock Source Select Bit

- 0 : Main clock with prescaler
- 1 : Sub clock with prescaler

Bit 2 (T1EN): Timer 1 Start Bit

- 0 : Timer 1 stop
- 1 : Timer 1 start

Bit 1 (T1OMS): Timer 1 Output Mode Select Bit

- 0 : Repeating mode
- 1 : One-shot mode

NOTE

One-shot mode is only used in Timer 1, Capture and PWM1 modes.

| Mode Selected | Description |
|---------------|--|
| Timer 1 | Down-counter wills underflow once and can't auto reload from T1PD. |
| Capture | In this mode, period and duty of the T1CAP input pin are measured once. This moment free running counter stop and can't detect a change of T1CAP edge. |
| PWM1 | In this mode will generate one set of PWM1's duty and period, and then free running counter will stop. |

Bit 0 (T1OC): Timer1 Output Flip-Flop Control Bit

0 : T-FF is low

1 : T-FF is high

6.2.29 Bank 2 R7 T1PD (Timer1 Period Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| PRD1[7] | PRD1[6] | PRD1[5] | PRD1[4] | PRD1[3] | PRD1[2] | PRD1[1] | PRD1[0] |

Bits 7~0 (PRD1[7]~PRD1[0]): The content of this register is a period of Timer 1.

6.2.30 Bank 2 R8 T1TD (Timer 1 Duty Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| TD1[7] | TD1[6] | TD1[5] | TD1[4] | TD1[3] | TD1[2] | TD1[1] | TD1[0] |

Bits 7~0 (TD1[7]~TD1[0]): The content of this register is a duty of Timer 1.

6.2.31 Bank 2 R9 T2CR (Timer 2 Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| T2IF | T2IE | T2EN | T2MS1 | T2MS0 | T2P2 | T2P1 | T2P0 |

Bit 7 (T2IF): Interrupt Flag of Timer 2 Interrupt

Bit 6 (T2IE): Timer 2 Interrupt Mask Bit

0 : Disable Timer 2 interrupt

1 : Enable Timer 2 interrupt

Bit 5 (T2EN): Timer 2 Start Bit

0 : Timer 2 stop

1 : Timer 2 start

Bits 4~3 (T2MS1~T2MS0): Timer 2 Operation Mode Selects Bits

| T2MS1 | T2MS0 | Timer 2 Mode Select |
|-------|-------|-------------------------|
| 0 | 0 | Timer 2 |
| 0 | 1 | SPI Baud Rate Generator |
| 1 | 0 | PWM 2 |
| 1 | 1 | |

Bits 2~0 (T2P2~T2P0): Timer 2 Prescaler Bits

| T2P2 | T2P1 | T2P0 | Prescaler |
|------|------|------|---------------|
| 0 | 0 | 0 | 1:2 (Default) |
| 0 | 0 | 1 | 1 : 4 |
| 0 | 1 | 0 | 1 : 8 |
| 0 | 1 | 1 | 1 : 16 |
| 1 | 0 | 0 | 1 : 32 |
| 1 | 0 | 1 | 1 : 64 |
| 1 | 1 | 0 | 1 : 128 |
| 1 | 1 | 1 | 1 : 256 |

6.2.32 Bank 2 RA T2PD (Timer 2 Period Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| PRD2[7] | PRD2[6] | PRD2[5] | PRD2[4] | PRD2[3] | PRD2[2] | PRD2[1] | PRD2[0] |

Bits 7~0 (PRD2[7]~PRD2[0]): The content of this register is a period of Timer2.

6.2.33 Bank 2 RB T2TD (Timer 2 Duty Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| TD2[7] | TD2[6] | TD2[5] | TD2[4] | TD2[3] | TD2[2] | TD2[1] | TD2[0] |

Bits 7~0 (TD2[7]~TD2[0]): The contents of this register is a duty of Timer 2.

6.2.34 Bank 2 RC SPIS (SPI Status Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DORD | TD1 | TD0 | 0 | OD3 | OD4 | 0 | RBF |

Bit 7 (DORD): Data Shift Control Bit

0 : Shift left (MSB first)

1 : Shift right (LSB first)

Bits 6~5 (TD1~TD0): SDO Status Output Delay Times Options

| TD1 | TD0 | Delay Time |
|-----|-----|------------|
| 0 | 0 | 8 CLK |
| 0 | 1 | 16 CLK |
| 1 | 0 | 24 CLK |
| 1 | 1 | 32 CLK |

Bit 4: Reserved

Bit 3 (OD3): Open-Drain Control Bit

1 : Open-drain enable for SDO

0 : Open-drain disable for SDO

Bit 2 (OD4): Open-Drain Control bit

1 : Open-drain enable for SCK

0 : Open-drain disable for SCK

Bit 1: Reserved

Bit 0 (RBF): Read Buffer Full Flag

1 : Receiving completed, and SPIRB is fully exchanged.

0 : Receiving not completed, and SPIRB has not fully exchanged.

6.2.35 Bank 2 RD SPIC (SPI Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CES | SPIE | SRO | SSE | SDOC | SBR2 | SBR1 | SBR0 |

Bit 7 (CES): Clock Edge Select Bit

0 : Data shift out on rising edge, and shifts in on falling edge. Data is on hold during low-level.

1 : Data shift out falling edge, and shift in on rising edge. Data is on hold during high-level.

Bit 6 (SPIE): SPI Enable Bit

0 : Disable SPI mode

1 : Enable SPI mode

Bit 5 (SRO): SPI Read Overflow Bit

0 : No overflow

1 : A new data is received while the previous data is still being held in the SPIRB register. In this situation, the data in SPIS register will be destroyed. To avoid setting this bit, user is required to read the SPIRB register although only the transmission is implemented. This can only occur in slave mode.

Bit 4 (SSE): SPI Shift Enable Bit

0 : Reset as soon as the shift is complete, and the next byte is read to shift.

1 : Start to shift, and remain on “1” while the current byte is still being transmitted.

Bit 3 (SDOC): SDO Output Status Control Bit

0 : After the serial data output, the SDO remain high.

1 : After the serial data output, the SDO remain low.

Bits 2~0 (SBR2~SBR0): SPI Baud Rate Select Bits

| SBR2 | SBR1 | SBR0 | Mode | SPI Baud Rate |
|------|------|------|--------|---------------|
| 0 | 0 | 0 | Master | Fosc/2 |
| 0 | 0 | 1 | Master | Fosc/4 |
| 0 | 1 | 0 | Master | Fosc/8 |
| 0 | 1 | 1 | Master | Fosc/16 |
| 1 | 0 | 0 | Master | Fosc/32 |
| 1 | 0 | 1 | Master | Timer2 |
| 1 | 1 | 0 | Slave | /SS enable |
| 1 | 1 | 1 | Slave | /SS disable |

6.2.36 Bank 2 RE SPIR (SPI Read Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SRB7 | SRB6 | SRB5 | SRB4 | SRB3 | SRB2 | SRB1 | SRB0 |

Bits 7~0 (SRB7~SRB0): SPI Read Data Buffer

6.2.37 Bank 2 RF SPIW (SPI Write Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SWB7 | SWB6 | SWB5 | SWB4 | SWB3 | SWB2 | SWB1 | SWB0 |

Bits 7~0 (SWB7~SWB0): SPI Write Data Buffer

6.2.38 Bank 3 R5 URC (UART Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|--------|--------|--------|--------|--------|-------|-------|
| URTD8 | UMODE1 | UMODE0 | BRATE2 | BRATE1 | BRATE0 | UTBE | TXE |

Bit 7 (URTD8): Transmission Data Bit 8

Bits 6~5 (UMODE1~UMODE0): UART Transmission Mode Select Bit

| UMODE1 | UMODE0 | UART Mode |
|--------|--------|----------------|
| 0 | 0 | Mode 1 : 7-Bit |
| 0 | 1 | Mode 2 : 8-Bit |
| 1 | 0 | Mode 3 : 9-Bit |
| 1 | 1 | Reserved |

Bits 4~2 (BRATE2~BRATE0): Transmit Baud Rate Select ($T_{uart}=F_c/16$)

| BRATE2 | BRATE1 | BRATE0 | Baud Rate | e.g. $F_c = 8\text{MHz}$ |
|--------|--------|--------|----------------|--------------------------|
| 0 | 0 | 0 | $T_{uart}/13$ | 38400 |
| 0 | 0 | 1 | $T_{uart}/26$ | 19200 |
| 0 | 1 | 0 | $T_{uart}/52$ | 9600 |
| 0 | 1 | 1 | $T_{uart}/104$ | 4800 |
| 1 | 0 | 0 | $T_{uart}/208$ | 2400 |
| 1 | 0 | 1 | $T_{uart}/416$ | 1200 |
| 1 | 1 | 0 | Timer 1 | |
| 1 | 1 | 1 | Reserved | |

Bit 1 (UTBE): UART transfer buffer empty flag. Set to 1 when transfer buffer is empty. Reset to 0 automatically when write in to URTD register. UTBE bit will be cleared by hardware when enabling transmission. The UTBE bit is read-only. Therefore, writing to the URTD register is necessary to start transmit shifting.

Bit 0 (TXE): Enable transmission

0 : Disable

1 : Enable

6.2.39 Bank 3 R6 URS (UART Status)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| URRD8 | EVEN | PRE | PRERR | OVERR | FMERR | URBF | RXE |

Bit 7 (URRD8): Receiving Data Bit 8

Bit 6 (EVEN): Select Parity Check

0 : Odd parity

1 : Even parity

Bit 5 (PRE): Enable Parity Addition

0 : Disable

1 : Enable

Bit 4 (PRERR): Parity Error Flag

Set to 1 when parity error occurs and cleared to 0 by software.

Bit 3 (OVERR): Over Running Error Flag

Set to 1 when overrun error occurs and cleared to 0 by software.

Bit 2 (FMERR): Framing Error Flag

Set to 1 when framing error occurs and cleared to 0 by software.

Bit 1 (URBF): UART Read Buffer Full Flag

Set to 1 when one character is received. Reset to 0 automatically when read from URS register. URBF will be cleared by hardware when enabling receiving. And URBF bit is read-only. Therefore, reading the URS register is necessary to avoid overrun error.

Bit 0 (RXE): Enable Receiving

0 : Disable

1 : Enable

6.2.40 Bank 3 R7 URRD (UART_RD Data Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| URRD7 | URRD6 | URRD5 | URRD4 | URRD3 | URRD2 | URRD1 | URRD0 |

Bits 7~0 (URRD7~URRD0): UART Receive Data Buffer. Read only.

6.2.41 Bank 3 R8 URTD (UART_TD Data Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|--------|--------|--------|--------|--------|--------|-------|
| URTD 7 | URTD 6 | URTD 5 | URTD 4 | URTD 3 | URTD 2 | URTD 1 | URTD0 |

Bits 7~0 (URTD7~URTD0): UART Transmit Data Buffer. Write only.

6.2.42 Bank 3 R9 ADCR (A/D Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ADRUN | ADP | ADCK1 | ADCK0 | ADIS3 | ADIS2 | ADIS1 | ADIS0 |

Bit 7 (ADRUN): AD Conversion Start

0 : Reset on completion of the conversion by hardware, this bit cannot be reset by software.

1 : Conversion starts

Bit 6 (ADP): A/D Power Control

Bits 5~4 (ADCK1~ADCK0): AD Converted Time Select Bits

| ADCK1 | ADCK0 | Clock Source | Max. Operating Frequency (Fc) |
|-------|-------|--------------|-------------------------------|
| 0 | 0 | Fc/4 | 1MHz |
| 0 | 1 | Fc/16 | 4MHz |
| 1 | 0 | Fc/32 | 8MHz |
| 1 | 1 | Fc/64 | 16MHz |

Bits 3~0 (ADIS3~ADIS0): A/D Input Select Bits

| ADIS3 | ADIS2 | ADIS1 | ADIS0 | Analog Input Pin |
|-------|-------|-------|-------|------------------|
| 0 | 0 | 0 | 0 | AD0 |
| 0 | 0 | 0 | 1 | AD1 |
| 0 | 0 | 1 | 0 | AD2 |
| 0 | 0 | 1 | 1 | AD3 |
| 0 | 1 | 0 | 0 | AD4 |
| 0 | 1 | 0 | 1 | AD5 |
| 0 | 1 | 1 | 0 | AD6 |
| 0 | 1 | 1 | 1 | AD7 |
| 1 | 0 | 0 | 0 | AD8 |
| 1 | 0 | 0 | 1 | AD9 |
| 1 | 0 | 1 | 0 | AD10 |
| 1 | 0 | 1 | 1 | AD11 |

6.2.43 Bank 3 RA ADICH (A/D Input Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CALI | ADREF | 0 | 0 | ADE11 | ADE10 | ADE9 | ADE8 |

Bit 7 (CALI): Calibration Enable Bit for A/D Offset

0 : disable Calibration

1 : enable Calibration

Bit 6 (ADREF): AD Reference Voltage Input Select

0 : Internal VDD, P84 is used as I/O.

1 : External reference pin, P84 is used as reference input pin.

Bits 5~4: Reserved

Bits 3~0 (ADE11~ADE8): AD Input Pin Enable Control

0 : Functions as I/O pin

1 : Functions as analog input pin

6.2.44 Bank 3 RB ADICL (A/D Input Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE0 |

Bits 7~0 (ADE7~ADE0): AD input pin enable control.

0 : Functions as I/O pin

1 : Functions as analog input pin

6.2.45 Bank 3 RC ADDH (AD High 8-bit Data Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ADD11 | ADD10 | ADD9 | ADD8 | ADD7 | ADD6 | ADD5 | ADD4 |

Bits 7~0 (ADD11~ADD4): AD High 8-Bit Data Buffer

6.2.46 Bank 3 RD ADDL (AD Low 4-bit Data Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|--------|--------|--------|-------|-------|-------|-------|
| SIGN | VOF[2] | VOF[1] | VOF[0] | ADD3 | ADD2 | ADD1 | ADD0 |

Bit 7 (SIGN): Polarity Bit of Offset Voltage

0 : Negative voltage

1 : Positive voltage

Bits 6~4 (VOF[2]~VOF[0]): Offset Voltage Bits

| VOF[2] | VOF[1] | VOF[0] | EM78P510N |
|--------|--------|--------|-----------|
| 0 | 0 | 0 | 0LSB |
| 0 | 0 | 1 | 2LSB |
| 0 | 1 | 0 | 4LSB |
| 0 | 1 | 1 | 6LSB |
| 1 | 0 | 0 | 8LSB |
| 1 | 0 | 1 | 10LSB |
| 1 | 1 | 0 | 12LSB |
| 1 | 1 | 1 | 14LSB |

Bits 3~0 (ADD3~ADD0): AD Low 4-Bit Data Buffer

6.2.47 Bank 3 RE EIESH (External Interrupt Edge Select High Byte Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EIES7 | EIES6 | EIES5 | EIES4 | EIES3 | EIES2 | EIES1 | EIES0 |

Bits 7~0 (EIES7~EIES0): External Interrupt 7~0 Edge Select Bit

0 : Falling edge interrupt

1 : Rising edge interrupt

6.2.48 Bank 3 RF EIESL (External Interrupt Edge Select Low Byte Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|--------|--------|-------|-------|
| 0 | 0 | 0 | ADWK | INTWK9 | INTWK8 | EIES9 | EIES8 |

Bits 7~5: Reserved

Bit 4 (ADWK): A/D Converter Wake-up Function Enable Bit

0 : Disable

1 : Enable

Bits 3~2 (INTWK9~INTWK8): External Interrupt 9~8 Wake-up Function Enable Bit

0 : Disable

1 : Enable

Bits 1~0 (EIES9~EIES8): External Interrupt 9~8 Edge Select Bit

0 : Falling edges interrupt

1 : Rising edges interrupt

6.2.49 Bank 4 R5 LEDDCR (LED Drive Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| LEDD7 | LEDD6 | LEDD5 | LEDD4 | LEDD3 | LEDD2 | LEDD1 | LEDD0 |

Bits 7~0 (LEDD7~LEDD0): 8-bit LED Drive Control Registers

- 0 : Port 9 functions as normal I/O
- 1 : Port 9 functions as LED direct drive I/O

6.2.50 Bank 4 R6 WBCR (Watchdog Timer and Buzzer Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|--------|--------|-------|-------|-------|
| WTCS | WTIE | WTIF | WTSSB1 | WTSSB0 | BUZE | BSSB1 | BSSB0 |

Bit 7 (WTCS): Watchdog Timer and Buzzer Clock Source Select Bit

- 0 : Main Clock divided by 256
- 1 : Sub clock

Bit 6 (WTIE): Watch Timer Enable Bit and Interrupt Mask

- 0 : Disable
- 1 : Enable

Bit 5 (WTIF): Watch Timer Interrupt Flag

Bits 4~3 (WTSSB1~ WTSSB0): Watch Timer Interval Select Bits

| WTSSB1 | WTSSB0 | Watch Timer Interval Select (WTCS=1) |
|--------|--------|--------------------------------------|
| 0 | 0 | 1.0S |
| 0 | 1 | 0.5S |
| 1 | 0 | 0.25S |
| 1 | 1 | 3.91ms |

Bit 2 (BUZE): Buzzer Enable and PORT 91 as Buzzer Output Pin

- 0 : No action
- 1 : Enable buzzer output

Bits 1~0 (BSSB1~BSSB0): Buzzer Output Frequency Select Bits

| BSSB1 | BSSB0 | Buzzer Signal Select (WTCS=1) |
|-------|-------|-------------------------------|
| 0 | 0 | 0.5kHz |
| 0 | 1 | 1kHz |
| 1 | 0 | 2kHz |
| 1 | 1 | 4kHz |

6.2.51 Bank 4 R7 PIOC (Port 7 I/O Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IOC77 | IOC76 | IOC75 | IOC74 | IOC73 | IOC72 | IOC71 | IOC70 |

Bits 7~0 (IOC77~IOC70): Port 7 8-Bit I/O Direction Control Registers

0 : Define Port 7 as output port

1 : Define Port 7 as input port

6.2.52 Bank 4 R8 PIOC (Port 8 I/O Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IOC87 | IOC86 | IOC85 | IOC84 | IOC83 | IOC82 | IOC81 | 0 |

Bits 7~1 (IOC87~IOC81): Port 8 7-Bit I/O Direction Control Registers

0 : Define Port 8 as output port

1 : Define Port 8 as input port

Bit 0: Reserved

6.2.53 Bank 4 R9 PIOC (Port 9 I/O Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IOC97 | IOC96 | IOC95 | IOC94 | IOC93 | IOC92 | IOC91 | IOC90 |

Bits 7~0 (IOC97~IOC90): Port 9 8-Bit I/O Direction Control Registers

0 : Define Port 9 as output port

1 : Define Port 9 as input port

6.2.54 Bank 4 RA PIOC (Port A I/O Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IOCA7 | IOCA6 | IOCA5 | IOCA4 | IOCA3 | IOCA2 | IOCA1 | IOCA0 |

Bits 7~0 (IOCA7~IOCA0): Port A 8-Bit I/O Direction Control Registers

0 : Define Port A as output port

1 : Define Port A as input port

6.2.55 Bank 4 RB PIOC(R) (Port B I/O Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IOCB7 | IOCB6 | IOCB5 | IOCB4 | IOCB3 | IOCB2 | IOCB1 | IOCB0 |

Bits 7~0 (IOCB7~IOCB0): Port B 8-Bit I/O Direction Control Registers

0 : Define Port B as output port

1 : Define Port B as input port

6.2.56 Bank 4 RC PIOC(R) (Port C I/O Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 1 | 1 | 1 | 1 | IOCC3 | IOCC2 | IOCC1 | IOCC0 |

Bits 7~4: Reserved

Bits 3~0 (IOCC3~IOCC0): Port C 4-Bit I/O Direction Control Registers

0 : Define Port C as output port

1 : Define Port C as input port

6.2.57 Bank 4 RF WKCR (Wake-up Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| INTWK7 | INTWK6 | INTWK5 | INTWK4 | INTWK3 | INTWK2 | INTWK1 | INTWK0 |

Bits 7~0 (INTWK7~INTWK0): External Interrupt 7~0 Wake Up Function Enable Bit

0 : Disable

1 : Enable

6.2.58 Bank 5 R6 UARC2 (UART Control Register 2)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|--------|-------|-------|-------|
| 0 | 0 | UARTE | 0 | UINVEN | 0 | 0 | 0 |

Bits 7~6: Reserved

Bit 5 (UARTE): UART Function Enable

0 : UART functions disable. PB4, PB5 as general I/O

1 : UART functions enable. PB4, PB5 as UART Rx, Tx pin

Bit 4: Reserved

Bit 3 (UINVEN): Enable UART TX and Rx Port Inverse Output

0 : Disable Tx and Rx port inverse output

1 : Enable Tx and Rx port inverse output

Bits 2~0: Reserved

6.2.59 Bank 5 R7 P7PHCR (Port 7 Pull High Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PH77 | PH76 | PH75 | PH74 | PH73 | PH72 | PH71 | PH70 |

Bits 7~0 (PH77~PH70): Port 7 8-Bit I/O Pull High Control Registers

0 : Pull high disable

1 : Pull high enable

6.2.60 Bank 5 R8 P8PHCR (Port 8 Pull High Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PH87 | PH86 | PH85 | PH84 | PH83 | PH82 | PH81 | 0 |

Bits 7~1 (PH87~PH81): PORT 8 7-Bit I/O Pull High Control Registers

0 : Pull high disable

1 : Pull high enable

Bit 0: Reserved

6.2.61 Bank 5 R9 P9PHCR (Port 9 Pull-high Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PH97 | PH96 | PH95 | PH94 | PH93 | PH92 | PH91 | PH90 |

Bits 7~0 (PH97~PH90): Port 9 8-bit I/O Pull-high Control Registers

0 : Pull-high disable

1 : Pull-high enable

6.2.62 Bank 5 RA PAPHCR (Port A Pull-high Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PHA7 | PHA6 | PHA5 | PHA4 | PHA3 | PHA2 | PHA1 | PHA0 |

Bits 7~0 (PHA7~PHA0): Port A 8-bit I/O Pull-high Control Registers

0 : Pull-high disable

1 : Pull-high enable

6.2.63 Bank 5 RB PBPBHC (Port B Pull-high Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PHB7 | PHB6 | PHB5 | PHB4 | PHB3 | PHB2 | PHB1 | PHB0 |

Bits 7~0 (PHB7~PHB0): Port B 8-Bit I/O Pull-high Control Registers

0 : Pull high disable

1 : Pull high enable

6.2.64 Bank 5 RC PCPHCR (Port C Pull High Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | 0 | PHC3 | PHC2 | PHC1 | PHC0 |

Bits 7~4: Reserved

Bits 3~0 (PHC3~PHC0): Port C 4-Bit I/O Pull-high Control Registers

0 : Pull high disable

1 : Pull high enable

6.2.65 Bank 6 R6 LVRCCR (Low Voltage Reset Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | 0 | 0 | LVREN | LVR51 | LVR50 |

R6 use only ICE510 simulator

Bits 7~3: Reserved

Bit 2 (LVREN): Low Voltage Reset Enable Bit

0 : Disable

1 : Enable

Bits 1~0 (LVR51~LVR50): Low Voltage Reset Voltage Select Bits

| LVR51 | LVR50 | Reset Voltage |
|-------|-------|---------------|
| 0 | 0 | 2.6V |
| 0 | 1 | 3.3V |
| 1 | 0 | 3.9V |

6.2.66 Bank 6 R7 P7ODCR (Port 7 Open Drain Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OD77 | OD76 | OD75 | OD74 | OD73 | OD72 | OD71 | OD70 |

Bits 7~0 (OD77~OD70): Port 7 8-Bit I/O Open Drain Control Registers

0 : Open drain disable

1 : Open drain enable

6.2.67 Bank 6 R8 P8ODCR (Port 8 Open Drain Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OD87 | OD86 | OD85 | OD84 | OD83 | OD82 | OD81 | 0 |

Bits 7~1 (OD87~OD80): Port 8 7-bit I/O Open Drain Control Registers

0 : Open drain disable

1 : Open drain enable

Bit 0: Reserved

6.2.68 Bank 6 R9 P9ODCR (Port 9 Open Drain Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OD97 | OD96 | OD95 | OD94 | OD93 | OD92 | OD91 | OD90 |

Bits 7~0 (OD97~OD90): Port 9 8-Bit I/O Open Drain Control Registers

0 : Open drain disable

1 : Open drain enable

6.2.69 Bank 6 RA PAODCR (Port A Open Drain Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ODA7 | ODA6 | ODA5 | ODA4 | ODA3 | ODA2 | ODA1 | ODA0 |

Bits 7~0 (ODA7~ODA0): Port A 8-Bit I/O Open Drain Control Registers

0 : Open drain disable

1 : Open drain enable

6.2.70 Bank 6 RB PBODCR (Port B Open Drain Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ODB7 | ODB6 | ODB5 | ODB4 | ODB3 | ODB2 | ODB1 | ODB0 |

Bits 7~0 (ODB7~ODB0): Port B 8-Bit I/O Open Drain Control Registers

0 : Open drain disable

1 : Open drain enable

6.2.71 Bank 6 RC (Port C)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 1 | 1 | 1 | 1 | RC3 | RC2 | RC1 | RC0 |

Bits 7~4: Reserved

Bits 3~0 (RC3~RC0): Port C 4-Bit I/O Registers

6.2.72 R10~R3F (General Purpose Register)

R10~R1F and R20~R3F (Banks 0~7) are general purpose registers.

6.3 TCC/WDT Pre-scaler

Registers for the TCC/WDT Circuit

| R_BANK | Address | NAME | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|---------|--------------|-------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Bank 0 | 0x0D | TWTCR | WDTE | WPSR2 | WPSR1 | WPSR0 | TCCS | TPSR2 | TPSR1 | TPSR0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x0E | IMR | T1IE | LVDIE | ADIE | SPIE | URTIE | EXIE9 | EXIE8 | TCIE |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x0F | ISR | T1IF | LVDIF | ADIF | SPIIF | URTIF | EXIF9 | EXIF8 | TCIF |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

There are two 8-bit counters available as prescalers for the TCC and WDT, respectively. The TPSR0~TPSR2 bits of the Bank 0 RD (TWTCR) register are used to determine the ratio of the TCC prescaler. Likewise, the WPSR0~WPSR2 bits of the Bank 0 RD (TWTCR) register are used to determine the WDT prescaler. The prescaler (TPSR0~TPSR2) will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the “WDTC” and “SLEP” instructions. Fig.6-4 depicts the circuit diagram of TCC/WDT.

R1 (TCC) is an 8-bit timer/counter. The TCC clock source can be internal clock main clock or sub clock (32.768kHz). If TCC signal source is from the internal clock, TCC will be incremented by 1 at every instruction cycle (without prescaler). As illustrated in Fig. 6-4. The watchdog timer is a free running on-chip RC oscillator. The WDT will continue running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming. Refer to WDTE bit of Bank 0 RD (TWTCR) register. With no prescaler, the WDT time-out period is approximately 18 ms¹.

¹ **Note:** VDD=5V, Setup time period = 16.5ms ± 30% VDD=3V, Setup time period = 18ms ± 30%

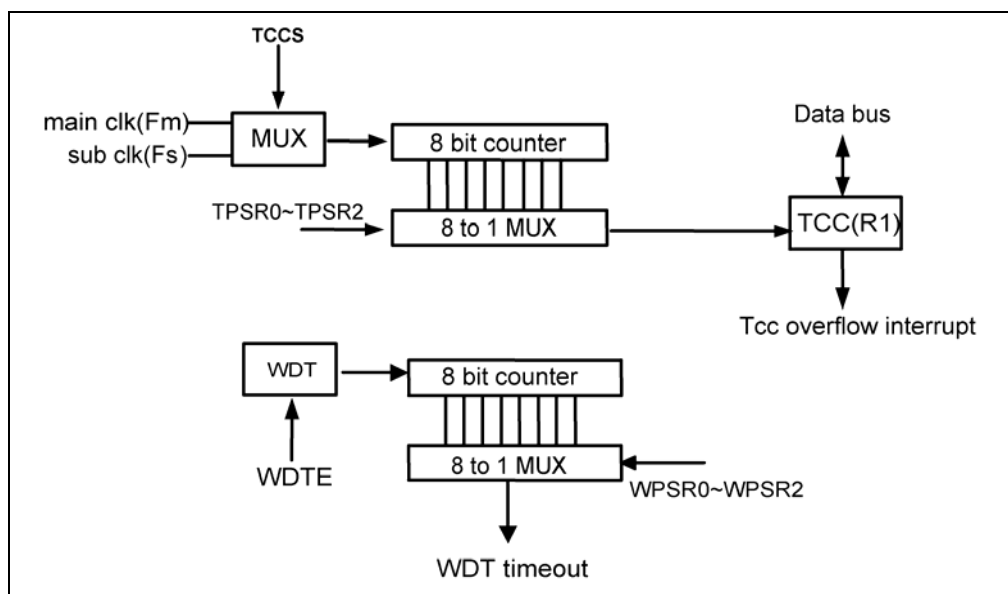


Figure 6-4 TCC/WDT Block Diagram

6.4 I/O Port

Registers for I/O Circuit

| R_BANK | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|-----------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bank 4 | 0X07~0X0C | PIOCR | IOC7 | IOC6 | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 5 | 0X07~0X0C | PHCR | PH7 | PH6 | PH5 | PH4 | PH3 | PH2 | PH1 | PH0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 6 | 0X07~0X0B | ODCR | OD7 | OD6 | OD5 | OD4 | OD3 | OD2 | OD1 | OD0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The I/O registers, (Port 7, Port 8, Port 9, Port A, Port B and Port C), are bidirectional tri-state I/O ports. All pins are pulled-high internally by software. Likewise, Port 7, Port 8, Port 9, Port A, Port B and Port C, can have open-drain output also through software. Port 7 [7:4], Port B [3:0] and Port 8 [3:2] provides an input status changed interrupt (or wake-up) function and is pulled-high by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register Bank 4 R7 ~ RC. The I/O registers and I/O control registers are both readable and writeable. The I/O interface circuits are shown in Fig. 6-5.

The I/O cannot be set to pull-high and output low at the same time. It can relatively increase the power consumption.

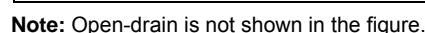


Figure 6-5 Circuits of I/O Port and I/O Control Register for Ports 7~ 9, and Ports A ~ C

A Reset can be caused by:

- Power-on reset
- WDT timeout (if enabled)
- LVR Reset
- RESET pin pulls low

The power-on reset circuit is always enabled, it will reset the CPU at 2.3V and power consumption is 0.5μA.

Once a Reset occurs, the following functions are performed:

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The TCC/Watchdog timer and prescaler are cleared.
- When power is on, all bits of R5 and R6 are cleared.
- The other registers are described in Table 2

Table 2 Summary of the Registers Initialized Values

| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------|-------------------------|--------------------------------------|--------|--------|-------|-------|-------|-------|-------|
| 0x00 | R0 (IAR) | Bit Name | - | - | - | - | - | - | - | - |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x01 | R1 (TCC) | Bit Name | - | - | - | - | - | - | - | - |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x02 | R2 (PC) | Bit Name | - | - | - | - | - | - | - | - |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | Continue to execute next instruction | | | | | | | |
| 0x03 | R3 (SR) | Bit Name | LV DEN | LV DS1 | LV DS0 | T | P | Z | DC | C |
| | | Power-on | 0 | 0 | 0 | 1 | 1 | U | U | U |
| | | /RESET and WDT | 0 | 0 | 0 | t | t | P | P | P |
| | | Wake-up from Pin Change | P | P | P | t | t | P | P | P |
| 0x04 | R4 (RSR) | Bit Name | VDB | BNC | X | X | X | X | X | X |
| | | Power-on | 1 | 1 | U | U | U | U | U | U |
| | | /RESET and WDT | 1 | 1 | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x05 | R5 (RBSR) | Bit Name | 0 | 0 | 0 | 0 | 0 | BS2 | BS1 | BS0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x06 | R6 (RPSR) | Bit Name | 0 | 0 | 0 | 0 | 0 | PS2 | PS1 | PS0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x07 | R7 (Port 7) | Bit Name | R77 | R76 | R75 | R74 | R73 | R62 | R71 | R70 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x08 | R8 (Port 8) | Bit Name | R87 | R86 | R85 | R84 | R83 | R82 | R81 | 0 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |

| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------|-------------------------|-------------------------|-------|---------|-------|--------|--------|--------|--------|--------|
| 0x09 | R9 (Port 9) | Bit Name | R97 | R96 | R95 | R94 | R93 | R92 | R91 | R90 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0A | RA (Port A) | Bit Name | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0B | RB (Port B) | Bit Name | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0C | RC (SCCR) | Bit Name | 0 | CLK2 | CLK1 | CLK0 | IDLE | 0 | 0 | CPUS |
| | | Power-on | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| | | Wake-Up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0D | RD (TWTCR) | Bit Name | WDTE | WPSR2 | WPSR1 | WPSR0 | TCCS | TPSR2 | TPSR1 | TPSR0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0E | RE (IMR) | Bit Name | T1IE | LVDIE | ADIE | SPIE | URTIE | EXIE9 | EXIE8 | TCIE |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0F | RF (ISR) | Bit Name | T1IF | LVDIF | ADIF | SPIIF | URTIF | EXIF9 | EXIF8 | TCIF |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| Bank1 0x05 | Bank 1 R5 (LCDCR) | Bit Name | LCDEN | LCDPYTE | BS1 | BS0 | DS1 | DS0 | LCDF1 | LCDF0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x06 | R6 (LCDAR) | Bit Name | 0 | 0 | 0 | LCD_A4 | LCD_A3 | LCD_A2 | LCD_A1 | LCD_A0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |

| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------|-----------------------|-------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0X07 | R7 (LCDBR) | Bit Name | LCD_D7 | LCD_D6 | LCD_D5 | LCD_D4 | LCD_D3 | LCD_D2 | LCD_D1 | LCD_D0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X08 | R8 (LCDVCR) | Bit Name | 0 | 0 | 0 | LCDC1 | LCDC0 | LCDVC2 | LCDVC1 | LCDVC0 |
| | | Power-on | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X09 | R9 (LCDCCR) | Bit Name | COM7 | COM6 | COM5 | COM4 | COM3 | COM2 | COM1 | COM0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X0A | RA (LCDSCR0) | Bit Name | SEG7 | SEG6 | SEG5 | SEG4 | SEG3 | SEG2 | SEG1 | SEG0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X0B | RB (LCDSCR1) | Bit Name | SEG15 | SEG14 | SEG13 | SEG12 | SEG11 | SEG10 | SEG9 | SEG8 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X0C | RC (LCDSCR2) | Bit Name | 0 | SEG22 | SEG21 | SEG20 | SEG19 | SEG18 | SEG17 | SEG16 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X0E | RE (EIMR) | Bit Name | EXIE7 | EXIE6 | EXIE5 | EXIE4 | EXIE3 | EXIE2 | EXIE1 | EXIE0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X0F | RF (EISR) | Bit Name | EXIF7 | EXIF6 | EXIF5 | EXIF4 | EXIF3 | EXIF2 | EXIF1 | EXIF0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| Bank 2 0X05 | Bank2 R5 (T1CR) | Bit Name | TIS1 | TIS0 | T1MS2 | T1MS1 | TIMS0 | T1P2 | T1P1 | T1P0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |

| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------------|-------------------------|---------|---------|---------|---------|---------|---------|---------|---------|
| 0X06 | R6 (TSR) | Bit Name | T1MOD | TCRB | T1CSS1 | T1CSS0 | T2CSS | T1EN | T1OMS | T1OC |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X07 | R7 (T1PD) | Bit Name | PRD1[7] | PRD1[6] | PRD1[5] | PRD1[4] | PRD1[3] | PRD1[2] | PRD1[1] | PRD1[0] |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X08 | R8 (T1TD) | Bit Name | TD1[7] | TD1[6] | TD1[5] | TD1[4] | TD1[3] | TD1[2] | TD1[1] | TD1[0] |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X09 | R9 (T2CR) | Bit Name | T2IF | T2IE | T2EN | T2MS1 | T2MS0 | T2P2 | T2P1 | T2P0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X0A | RA (T2PD) | Bit Name | PRD2[7] | PRD2[6] | PRD2[5] | PRD2[4] | PRD2[3] | PRD2[2] | PRD2[1] | PRD2[0] |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X0B | RB (T2TD) | Bit Name | TD2[7] | TD2[6] | TD2[5] | TD2[4] | TD2[3] | TD2[2] | TD2[1] | TD2[0] |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X0C | RC (SPIS) | Bit Name | DORD | TD1 | TD0 | 0 | OD3 | OD4 | 0 | RBF |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X0D | RD (SPIC) | Bit Name | CES | SPIE | SRO | SSE | SDOC | SBRS2 | SBRS1 | SBRS0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0X0E | RE (SPIR) | Bit Name | SRB7 | SRB6 | SRB5 | SRB4 | SRB3 | SRB2 | SRB1 | SRB0 |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | U | U | U | U | U | U | U | U |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |

| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------|----------------------|-------------------------|-------|--------|--------|--------|--------|--------|-------|-------|
| 0x0F | RF (SPIW) | Bit Name | SWB7 | SWB6 | SWB5 | SWB4 | SWB3 | SWB2 | SWB1 | SWB0 |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | U | U | U | U | U | U | U | U |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| Bank3 0x05 | Bank3 R5 (URC) | Bit Name | URTD8 | UMODE1 | UMODE0 | BRATE2 | BRATE1 | BRATE0 | UTBE | TXE |
| | | Power-on | U | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | P | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x06 | R6 (URS) | Bit Name | URRD8 | EVEN | PRE | PRERR | OVERR | FMERR | URBF | RXE |
| | | Power-on | U | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | P | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x07 | R7 (URRD) | Bit Name | URRD7 | URRD6 | URRD5 | URRD4 | URRD3 | URRD2 | URRD1 | URRD0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x08 | R8 (URTD) | Bit Name | URTD7 | URTD6 | URTD5 | URTD4 | URTD3 | URTD2 | URTD1 | URTD0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x09 | R9 (ADCR) | Bit Name | ADRUN | ADP | ADCK1 | ADCK0 | ADIS3 | ADIS2 | ADIS1 | ADIS0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0A | RA (ADICH) | Bit Name | CALI | ADREF | 0 | 0 | ADE11 | ADE10 | ADE9 | ADE8 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0B | RB (ADICL) | Bit Name | ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0C | RC (ADDH) | Bit Name | ADD11 | ADD10 | ADD9 | ADD8 | ADD7 | ADD6 | ADD5 | ADD4 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |

| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------|-------------------------|-------------------------|-------|--------|--------|--------|--------|--------|-------|-------|
| 0x0D | RD (ADDL) | Bit Name | SIGN | VOF[2] | VOF[1] | VOF[0] | ADD3 | ADD2 | ADD1 | ADD0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0E | RE (EIESH) | Bit Name | EIES7 | EIES6 | EIES5 | EIES4 | EIES3 | EIES2 | EIES1 | EIES0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0F | RF (EIESL) | Bit Name | 0 | 0 | 0 | ADWK | INTWK9 | INTWK8 | EIES9 | EIES8 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| Bank4 0x05 | Bank4 R5 (LEDDCR) | Bit Name | LEDD7 | LEDD6 | LEDD5 | LEDD4 | LEDD3 | LEDD2 | LEDD1 | LEDD0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x06 | R6 (WBCR) | Bit Name | WTCS | WTIE | WTIF | WTSSB1 | WTSSB0 | BUZE | BSSB1 | BSSB0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x07 | R7 (IOC7) | Bit Name | IOC77 | IOC76 | IOC75 | IOC74 | IOC73 | IOC72 | IOC71 | IOC70 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x08 | R8 (IOC8) | Bit Name | IOC87 | IOC86 | IOC85 | IOC84 | IOC83 | IOC82 | IOC81 | 0 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x09 | R9 (IOC9) | Bit Name | IOC97 | IOC96 | IOC95 | IOC94 | IOC93 | IOC92 | IOC91 | IOC90 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0A | RA (IOCA) | Bit Name | IOCA7 | IOCA6 | IOCA5 | IOCA4 | IOCA3 | IOCA2 | IOCA1 | IOCA0 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |

| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------|------------------------|-------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0x0B | RB (IOCB) | Bit Name | IOCB7 | IOCB6 | IOCB5 | IOCB4 | IOCB3 | IOCB2 | IOCB1 | IOCB0 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0C | RC (IOCC) | Bit Name | 1 | 1 | 1 | 1 | IOCC3 | IOCC2 | IOCC1 | IOCC0 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0F | RF (WKCR) | Bit Name | INTWK7 | INTWK6 | INTWK5 | INTWK4 | INTWK3 | INTWK2 | INTWK1 | INTWK0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| Bank5 0x06 | Bank5 R6 (UARC2) | Bit Name | 0 | 0 | UARTE | 0 | UINVEN | 0 | 0 | 0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x07 | R7 (P7PHCR) | Bit Name | PH77 | PH76 | PH75 | PH74 | PH73 | PH72 | PH71 | PH70 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x08 | R8 (P8PHCR) | Bit Name | PH87 | PH86 | PH85 | PH84 | PH83 | PH82 | PH81 | 0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x09 | R9 (P9PHCR) | Bit Name | PH97 | PH96 | PH95 | PH94 | PH93 | PH92 | PH91 | PH90 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0A | RA (PAPHCR) | Bit Name | PHA7 | PHA6 | PHA5 | PHA4 | PHA3 | PHA2 | PHA1 | PHA0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0B | RB (PBPHCR) | Bit Name | PHB7 | PHB6 | PHB5 | PHB4 | PHB3 | PHB2 | PHB1 | PHB0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |

| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------|-------------------------|-------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0x0C | RC (PCPHCR) | Bit Name | 0 | 0 | 0 | 0 | PHC3 | PHC2 | PHC1 | PHC0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| Bank6 0x07 | Bank6 R7 (P7ODCR) | Bit Name | OD77 | OD76 | OD75 | OD74 | OD73 | OD72 | OD71 | OD70 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x08 | R8 (P8ODCR) | Bit Name | OD87 | OD86 | OD85 | OD84 | OD83 | OD82 | OD81 | 0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x09 | R9 (P9ODCR) | Bit Name | OD97 | OD96 | OD95 | OD94 | OD93 | OD92 | OD91 | OD90 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0A | RA (PAODCR) | Bit Name | ODA7 | ODA6 | ODA5 | ODA4 | ODA3 | ODA2 | ODA1 | ODA0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0B | RB (PBODCR) | Bit Name | ODB7 | ODB6 | ODB5 | ODB4 | ODB3 | ODB2 | ODB1 | ODB0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET and WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0C | RC | Bit Name | 1 | 1 | 1 | 1 | RC3 | RC2 | RC1 | RC0 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET and WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x10~ 0x3F | R10~R3F | Bit Name | - | - | - | - | - | - | - | - |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET and WDT | U | U | U | U | U | U | U | U |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |

Legend: "x" = not used "P" = previous value before reset
"u" = unknown or don't care

The controller can be awakened from sleep mode and idle mode. The wake-up signals list as following.

| Wake-up Signal | Sleep Mode | Idle Mode | Green Mode | Normal Mode |
|----------------|---|--|------------|-------------|
| TCC time out | × | Wake-up + interrupt + next instruction | Interrupt | Interrupt |
| INT pin | Wake-up + interrupt (if enabled) + next instruction | Wake-up + interrupt(if enabled) + next instruction | Interrupt | Interrupt |
| Timer 1 | × | Wake-up + interrupt + next instruction | Interrupt | Interrupt |
| Timer 2 | × | Wake-up + interrupt + next instruction | Interrupt | Interrupt |
| UART | × | Wake-up + interrupt + next instruction | Interrupt | Interrupt |
| SPI | × | × | Interrupt | Interrupt |
| LVD | × | Wake-up + interrupt + next instruction | Interrupt | Interrupt |
| A/D | Wake-up + interrupt(if enabled) + next instruction | Wake-up + interrupt(if interrupt enable) + next instruction | Interrupt | Interrupt |
| Watch timer | × | Wake-up + interrupt + next instruction | Interrupt | Interrupt |
| WDT time out | RESET | RESET | RESET | RESET |

Note: User must set the wake-up register (Bank 3 RF(EIESL) Bits 2~4 and Bank 4 RF(WKCR) Bits 0~7).

Wake up from INT pin or A/D in sleep and idle mode

After wake up:

1. If interrupt is enabled → interrupt+ next instruction
2. If interrupt is disabled → next instruction

6.6 Oscillator

6.6.1 Oscillator Modes

The EM78P510N can be operated in the three different oscillator modes for the main oscillator (R-OSCI, OSCO), namely, RC oscillator with external resistor and Internal capacitor mode (IC), crystal oscillator mode, and PLL operation mode. User can select one of those three modes by programming FMMD1 and FMMD0 in the Code Option register, the sub-oscillator can be operated in crystal mode and ERIC mode. Table 3 shows these three modes are defined.

Table 3 Oscillator Modes Defined by FSMD, FMMD1, FMMD0.

| FSMD | FMMD1 | FMMD0 | Main Clock | Sub-clock |
|------|-------|-------|----------------|----------------|
| 0 | 0 | 0 | RC type (ERIC) | RC type (ERIC) |
| 0 | 0 | 1 | Crystal type | RC type (ERIC) |
| 0 | 1 | 0 | PLL type | RC type (ERIC) |
| 0 | 1 | 1 | PLL type | RC type (ERIC) |
| 1 | 0 | 0 | RC type (ERIC) | Crystal type |
| 1 | 0 | 1 | Crystal type | Crystal type |
| 1 | 1 | 0 | PLL type | Crystal type |
| 1 | 1 | 1 | Crystal | None |

Table 4 Summary of Maximum Operating Speeds

| Conditions | VDD | Fxt max.(MHz) |
|------------|-----|---------------|
| Two clocks | 2.0 | 4 |
| | 3.0 | 8 |
| | 5.0 | 16 |

6.6.2 Crystal Oscillator/Ceramic Resonators (Crystal)

EM78P510N can be driven by an external clock signal through the OSCO pin as shown in Fig.6-6 below.

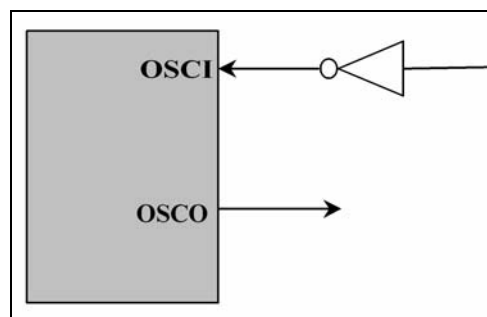


Figure 6-6 External Clock Input Circuit

In most applications, pin R-OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Fig. 6-7 depicts such circuitry. Table 5 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

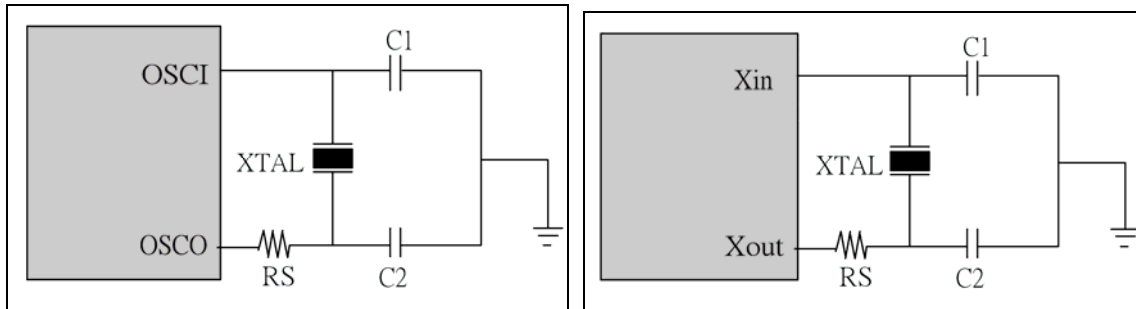


Fig. 6-7 Circuit for Crystal/Resonator

Table 5 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonators

| Oscillator Source | Oscillator Type | Frequency | C1 (pF) | C2 (pF) |
|-------------------|--------------------|-----------|---------|---------|
| Main oscillator | Ceramic Resonators | 455kHz | 100~150 | 100~150 |
| | | 2.0 MHz | 20~40 | 20~40 |
| | | 4.0 MHz | 10~30 | 10~30 |
| | Crystal Oscillator | 455kHz | 20~40 | 20~150 |
| | | 1.0MHz | 15~30 | 15~30 |
| | | 2.0MHz | 15 | 15 |
| | | 4.0MHz | 15 | 15 |
| Sub-oscillator | Crystal Oscillator | 32.768kHz | 25 | 25 |

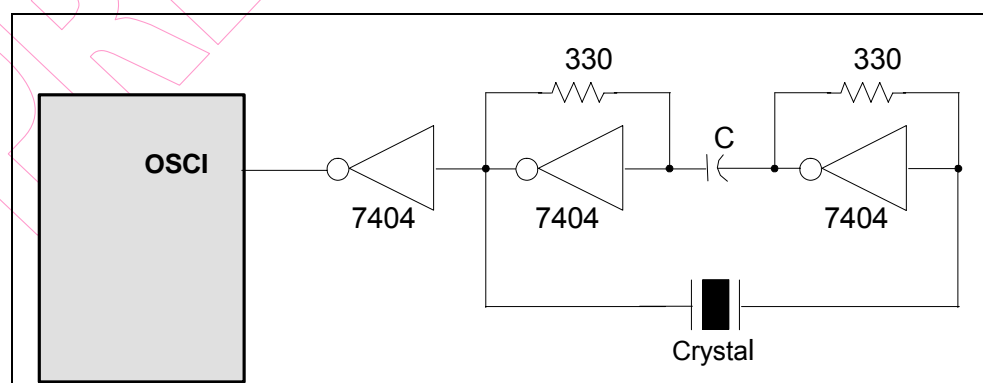


Fig. 6-8 Circuit for Crystal/Resonator-Series Mode

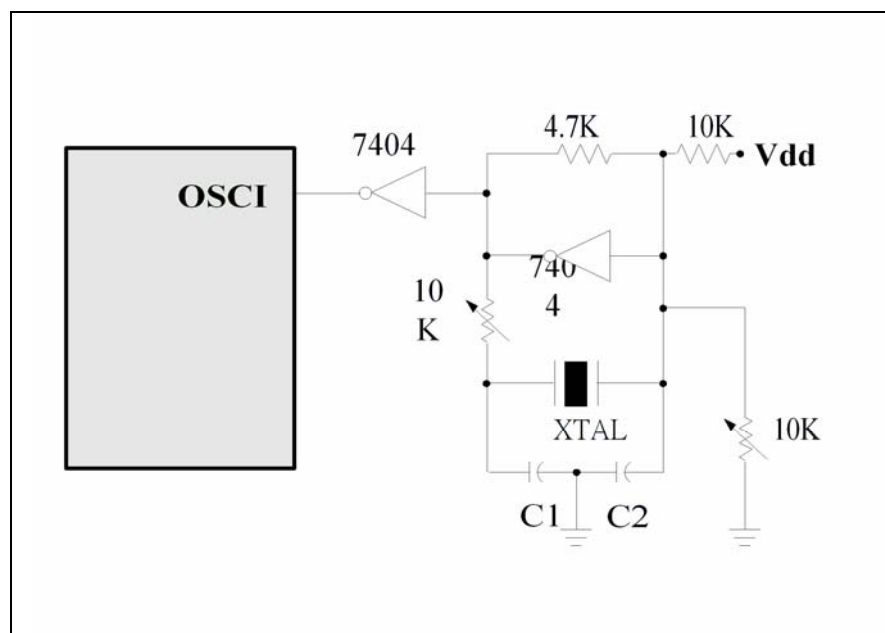


Fig. 6-9 Circuit for Crystal/Resonator-Parallel Mode

6.6.3 RC Oscillator Mode with Internal Capacitor

If both precision and cost are taken into consideration, the EM78P510N also offers a special oscillation mode, which has a built-in internal capacitor and an external resistor connected to Vcc. The internal capacitor functions as temperature compensator. In order to obtain more accurate frequency, a precise resistor is recommended.

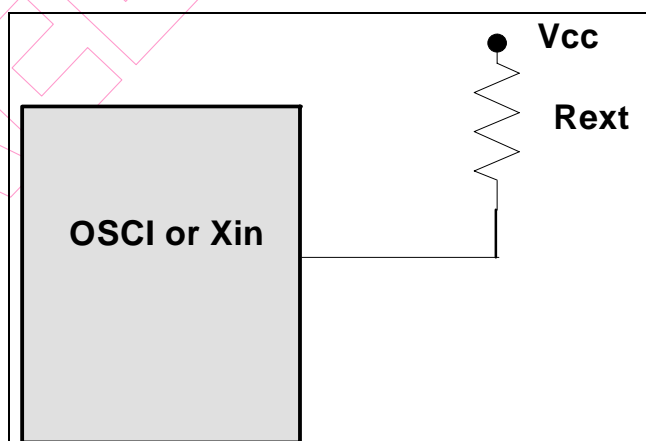


Fig. 6-10 Circuit for Internal C Oscillator Mode

Table 6 R Oscillator Frequencies

| Pin | Rext | Average Fosc 5V, 25°C | Average Fosc 3V, 25°C |
|--------|------|-----------------------|-----------------------|
| R-OSCI | 51k | 2.2221 MHz | 2.1972 MHz |
| | 100k | 1.1345 MHz | 1.1203 MHz |
| | 300k | 381.36kHz | 374.77kHz |
| Xin | 2.2M | 32.768kHz | 32.768kHz |

Note: ¹: Measured based on DIP packages.

²: The values are for design reference only.

6.6.4 Phase Lock Loop (PLL Mode)

When operating in PLL mode, the High frequency is determined by the sub-oscillator. RC (Bank 0) register can be chosen to change to high oscillator frequency. The relation between high frequency (Fm) and sub-oscillator is shown on the table below:

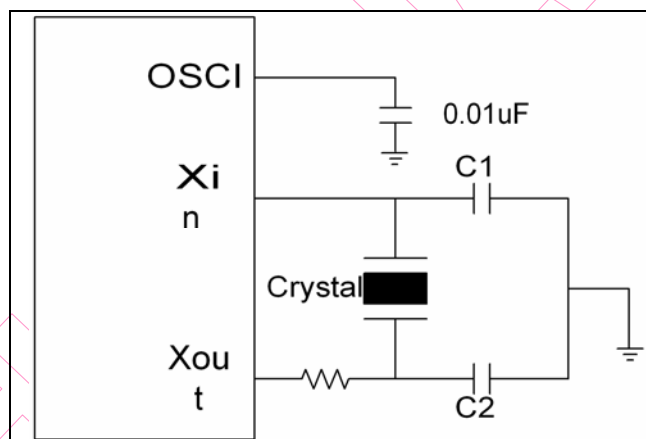


Fig. 6-11 Circuit for PLL mode

Bits 4~6 (CLK0~CLK2) of RC (Bank 0): Main Clock Selection Bits for PLL Mode
(Code Option Select)

| CLK2 | CLK1 | CLK0 | Main Clock | Example Fs = 32.768K |
|------|------|------|------------|----------------------|
| 0 | 0 | 0 | Fs × 122 | 3.997 MHz |
| 0 | 0 | 1 | Fs × 61 | 1.998 MHz |
| 0 | 1 | 0 | Fs × 61/2 | 0.999 MHz |
| 0 | 1 | 1 | Fs × 61/4 | 499.7 kHz |
| 1 | 0 | 0 | Fs × 244 | 7.995 MHz |
| 1 | 0 | 1 | Fs × 366 | 11.99 MHz |
| 1 | 1 | X | Fs × 488 | 15.99 MHz |

6.7 Power-on Considerations

Any microcontroller is not warranted to start operating properly before the power supply stabilizes in steady state. The EM78P510N has a built-in Power-on Reset (POR) with detection level range of 1.9V to 2.1V. The circuitry eliminates the extra external reset circuit. It will work well if V_{dd} rises quickly enough (50 ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

6.7.1 External Power-on Reset Circuit

The circuit shown in Fig.6-12 implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow V_{dd} to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time. Because the current leakage from the /RESET pin is about $\pm 5\mu\text{A}$, it is recommended that R should not be greater than 40K. In this way, the voltage at Pin /RESET is held below 0.2V. The diode (D) acts as a short circuit at power-down. The capacitor, C, is discharged rapidly and fully. R_{in}, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

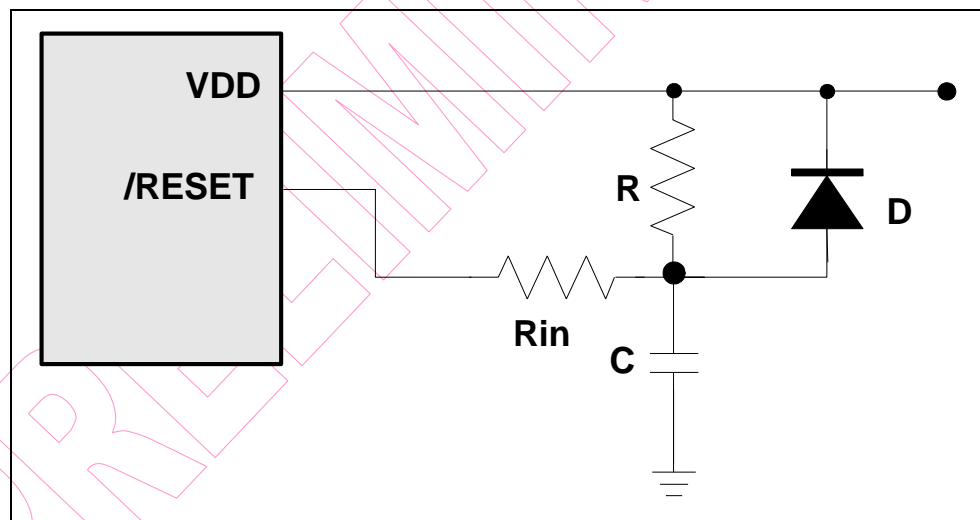


Fig. 6-12 External Power-on Reset Circuit

6.7.2 Residue-Voltage Protection

When battery is replaced, device power (V_{dd}) is taken off but residue-voltage remains. The residue-voltage may trips below V_{dd} minimum, but not to zero. This condition may cause a poor power-on reset. Fig.6-13 and Fig.6-14 show how to build a residue-voltage protection circuit.

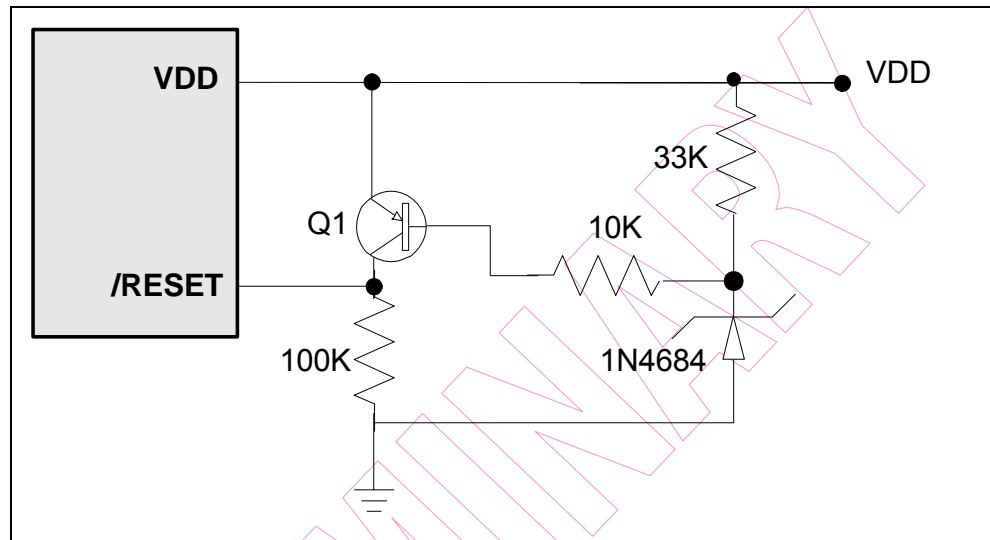


Fig. 6-13 Residue Voltage Protection Circuit 1

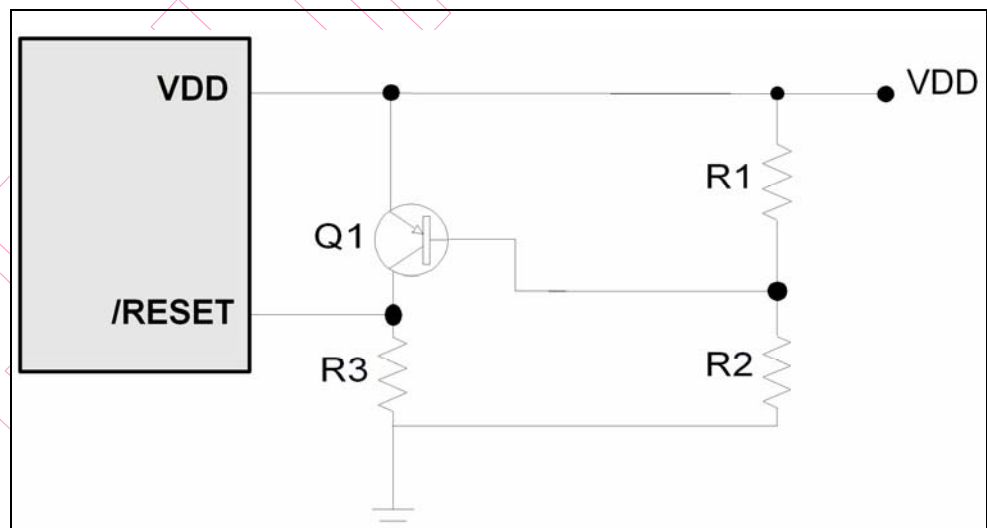


Fig. 6-14 Residue Voltage Protection Circuit 2

6.8 Interrupt

Registers for Interrupt

| R_BANK | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|---------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bank 0 | 0x0E | IMR | T1IE | LVDIE | ADIE | SPIE | URTIE | EXIE9 | EXIE8 | TCIE |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x0F | ISR | T1IF | LVDIF | ADIF | SPIF | URTIF | EXIF9 | EXIF8 | TCIF |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0X0E | EIMR | EXIE7 | EXIE6 | EXIE5 | EXIE4 | EXIE3 | EXIE2 | EXIE1 | EXIE0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0X0F | EISR | EXIF7 | EXIF6 | EXIF5 | EXIF4 | EXIF3 | EXIF2 | EXIF1 | EXIF0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 2 | 0X09 | T2CR | T2IF | T2IE | T2EN | T2MS1 | T2MS0 | T2P2 | T2P1 | T2P0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The EM78P510N has ten interrupt sources as listed below:

- TCC overflow interrupt
- External interrupt pin
- Watch timer interrupt
- Timer 1 overflow interrupt
- Timer 2 overflow interrupt
- A/D conversion complete interrupt
- UART transmit interrupt
- SPI transmit/receive interrupt
- Low voltage detector

This IC has internal interrupts which are falling edge triggered, as follows: TCC timer overflow interrupt, and two 8-bit upper counter/timer overflow interrupt. If these interrupt sources change signal from high to low, the RF register will generate a "1" flag to the corresponding register if RE register is enabled.

RF is the interrupt status register which records the interrupt request in flag bit. RE is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it will cause the next instruction to be fetched from address 0003H~001BH according to the interrupt source.

For EM78P510N, each individual interrupt source has its own interrupt vector as depicted in Table 7.

Before the interrupt subroutine is executed, the contents of ACC, R3[4:0], R5 and the R6 register will be saved by hardware. After the interrupt service routine is finished, ACC, R3[4:0], R5 and R6 will be pushed back. While in interrupt service routine, other interrupt service routine should not be allowed to be executed, so if other interrupts occur in an interrupt service routine, the hardware will save this interrupt, after which when interrupt service routine is completed, the next interrupt service routine will be executed.

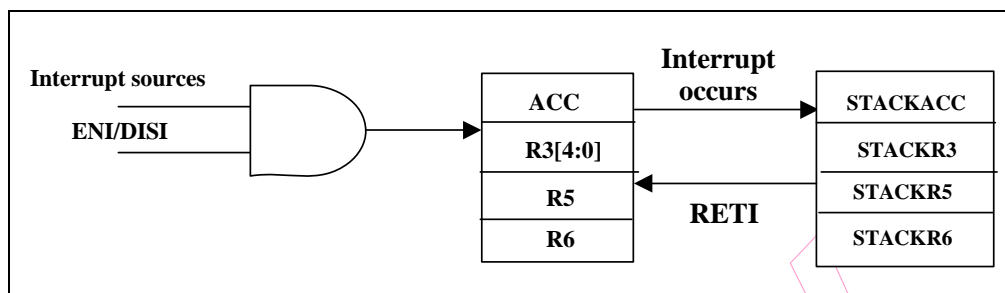


Fig. 6-15 Interrupt Backup Diagram

Table 7 Interrupt Vector

| Interrupt Vector | Interrupt Status |
|------------------|--|
| 0003H | TCC overflow interrupt |
| 0006H | External interrupt |
| 0009H | Watch timer interrupt |
| 000CH | Timer 1 overflow interrupt |
| 000FH | Timer 2 overflow interrupt |
| 0012H | A/D conversion complete interrupt |
| 0015H | UART transmit/receive complete interrupt |
| 0018H | SPI transmit/receive complete interrupt |
| 001BH | Low voltage detector interrupt |

6.9 LCD Driver

Registers for LCD Driver Circuit

| R_BANK | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|-----------|-----------|--------|---------|--------|--------|--------|--------|--------|--------|
| Bank 1 | 0X05 | LCD CR | LCDEN | LCDTYPE | BS1 | BS0 | DS1 | DS0 | LCDF1 | LCDF0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0X06 | LCDAR | 0 | 0 | 0 | LCD_A4 | LCD_A3 | LCD_A2 | LCD_A1 | LCD_A0 |
| | | | | | | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0X07 | LCD BR | LCD_D7 | LCD_D6 | LCD_D5 | LCD_D4 | LCD_D3 | LCD_D2 | LCD_D1 | LCD_D0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0X08 | LCDVCR | 0 | 0 | 0 | LCDC1 | LCDC0 | LCDVC2 | LCDVC1 | LCDVC0 |
| | | | | | | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0X09 | LCDCCR | CON7 | CON6 | CON5 | CON4 | CON3 | CON2 | CON1 | CON0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 1 | 0X0A~0X0C | LCDSCR0~2 | SEG | SEG | SEG | SEG | SEG | SEG | SEG | SEG |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The EM78P510N can drive LCD, up to 23 segments and 8 commons that can drive 8×23 dots totally. LCD block is made up of LCD driver, display RAM, segment output pins, common output pins and LCD operating power supply pins. This circuit can work on normal mode, green mode and idle mode.

The LCD duty, bias, the number of segment, the number of common and frame frequency are determined by the LCD controller register.

The basic structure contains a timing control which use the main system clock or subsystem clock to generate the proper timing for different duty and display access. The R5 register is command register for LCD driver that include LCD enable/disable, bias (1/2, 1/3 and 1/4), duty (Static, 1/3, 1/4, 1/8) and LCD frame frequency control. The register bank 1 R6 is LCD RAM address control register. The register bank 1 R7 is LCD RAM data buffer. The register bank1 R8 is LCD contrast control and LCD clock register. The control register is explained below.

6.9.1 R5 LCDCR (LCD Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|---------|-------|-------|-------|-------|-------|-------|
| LCDEN | LCDTYPE | BS1 | BS0 | DS1 | DS0 | LCDF1 | LCDF0 |

Bit 7 (LCDEN): LCD Enable Select Bit

- 0 : disable LCD Circuit. All common/segment outputs are set to VDD Level.
- 1 : enable LCD circuit

Bit 6 (LCDTYPE): LCD Drive Waveform Type Select Bit

- 0 : A type wave
- 1 : B type wave

Bits 5~4 (BS1~BS0): LCD Bias Select Bits

| BS1 | BS0 | LCD Bias Select |
|-----|-----|-----------------|
| 0 | 0 | 1/2 Bias |
| 0 | 1 | 1/3 Bias |
| 1 | X | 1/4 Bias |

Bits 3~2 (DS1~DS0): LCD Duty Select Bits

| DS1 | DS0 | LCD Duty |
|-----|-----|----------|
| 0 | 0 | Static |
| 0 | 1 | 1/3 Duty |
| 1 | 0 | 1/4 Duty |
| 1 | 1 | 1/8 Duty |

Bits 1~0 (LCDF1~LCDF0): LCD Frame Frequency Control Bits

| LCD Frame Frequency (e.g. $F_s = 32.768K$) | | | | | |
|---|-------|-----------------------------|-----------------------------|-----------------------------|----------------------------|
| LCDF1 | LCDF0 | Static | 1/3 Duty | 1/4 Duty | 1/8 Duty |
| 0 | 0 | $F_s/(512 \times 1) = 64.0$ | $F_s/(172 \times 3) = 63.5$ | $F_s/(128 \times 4) = 64$ | $F_s/(64 \times 8) = 64.0$ |
| 0 | 1 | $F_s/(560 \times 1) = 58.5$ | $F_s/(188 \times 3) = 58$ | $F_s/(140 \times 4) = 58.5$ | $F_s/(70 \times 8) = 58.5$ |
| 1 | 0 | $F_s/(608 \times 1) = 53.9$ | $F_s/(204 \times 3) = 53.5$ | $F_s/(152 \times 4) = 53.9$ | $F_s/(76 \times 8) = 53.9$ |
| 1 | 1 | $F_s/(464 \times 1) = 70.6$ | $F_s/(156 \times 3) = 70$ | $F_s/(116 \times 4) = 70.6$ | $F_s/(58 \times 8) = 70.6$ |

6.9.2 R6 LCDADDR (LCD Address Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|--------|--------|--------|--------|--------|
| 0 | 0 | 0 | LCD_A4 | LCD_A3 | LCD_A2 | LCD_A1 | LCD_A0 |

Bits 7~5: Reserved

Bits 4~0 (LCD_A4~LCD_A0): LCD RAM Address

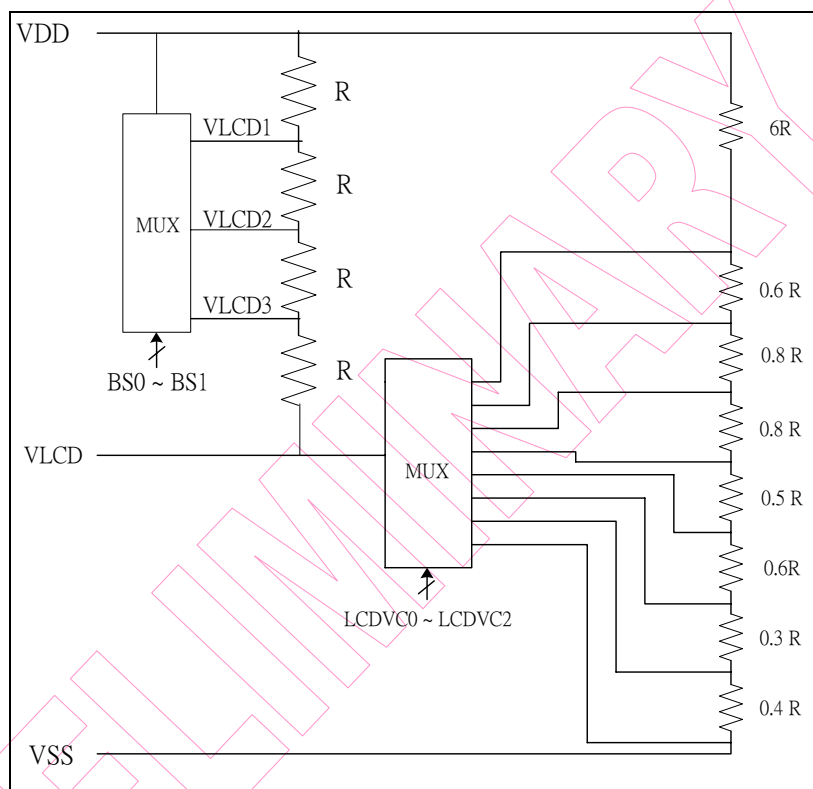
| R6 (LCD address) | R7 (LCD data buffer) | | | | | | | | Segment |
|------------------------|----------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|---------|
| | Bit 7 (LCD_D7) | Bit 6 (LCD_D6) | Bit 5 (LCD_D5) | Bit 4 (LCD_D4) | Bit 3 (LCD_D3) | Bit 2 (LCD_D2) | Bit 1 (LCD_D1) | Bit 0 (LCD_D0) | |
| 00H | | | | | | | | | SEG0 |
| 01H | | | | | | | | | SEG1 |
| 02H | | | | | | | | | SEG2 |
| | | | | | | | | | |
| 14H | | | | | | | | | SEG20 |
| 15H | | | | | | | | | SEG21 |
| 16H | | | | | | | | | SEG22 |
| Common | COM7 | COM6 | COM5 | COM4 | COM3 | COM2 | COM1 | COM0 | |

6.9.3 R7 LCDBR (LCD Data Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| LCD_D 7 | LCD_D 6 | LCD_D 5 | LCD_D 4 | LCD_D 3 | LCD_D 2 | LCD_D 1 | LCD_D 0 |

Bits 7~0 (LCD_D7~LCD_D0): LCD RAM Data Transfer Register

* When the value of the display segment is “1”, the LCD display is turned on; when the bit value is “0”, the display is turned off



6.9.4 R8 LCDVCR (LCD Voltage Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|--------|--------|--------|
| 0 | 0 | 0 | LCDC1 | LCDC0 | LCDVC2 | LCDVC1 | LCDVC0 |

Bits 7~5: Reserved

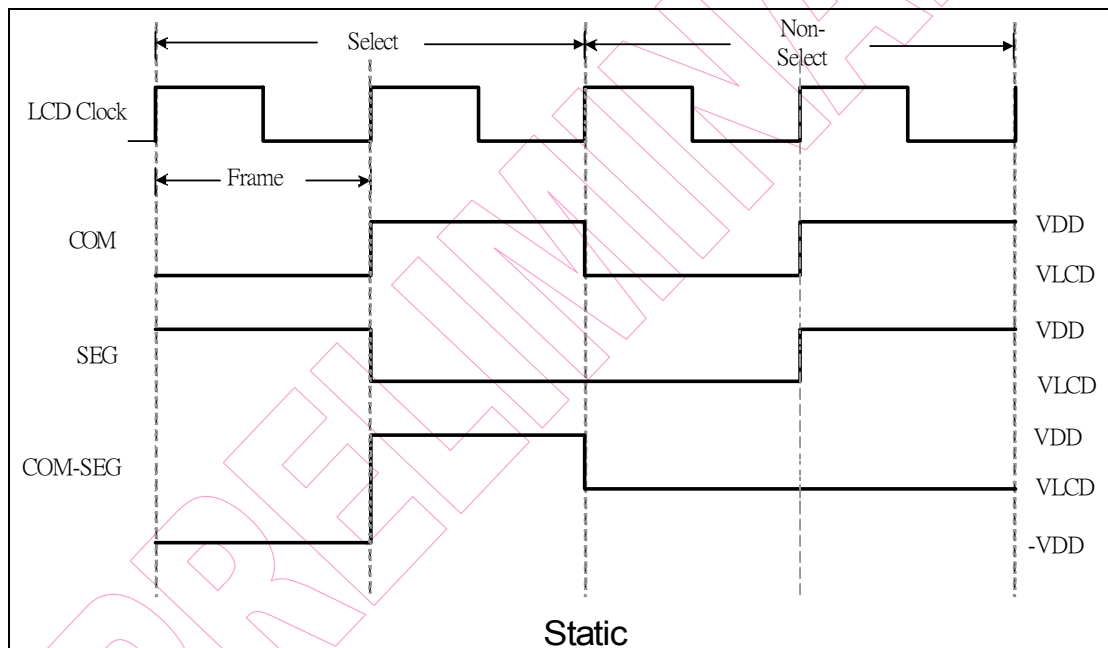
Bits 4~3 (LCDC1~LCDC0): LCD Clock

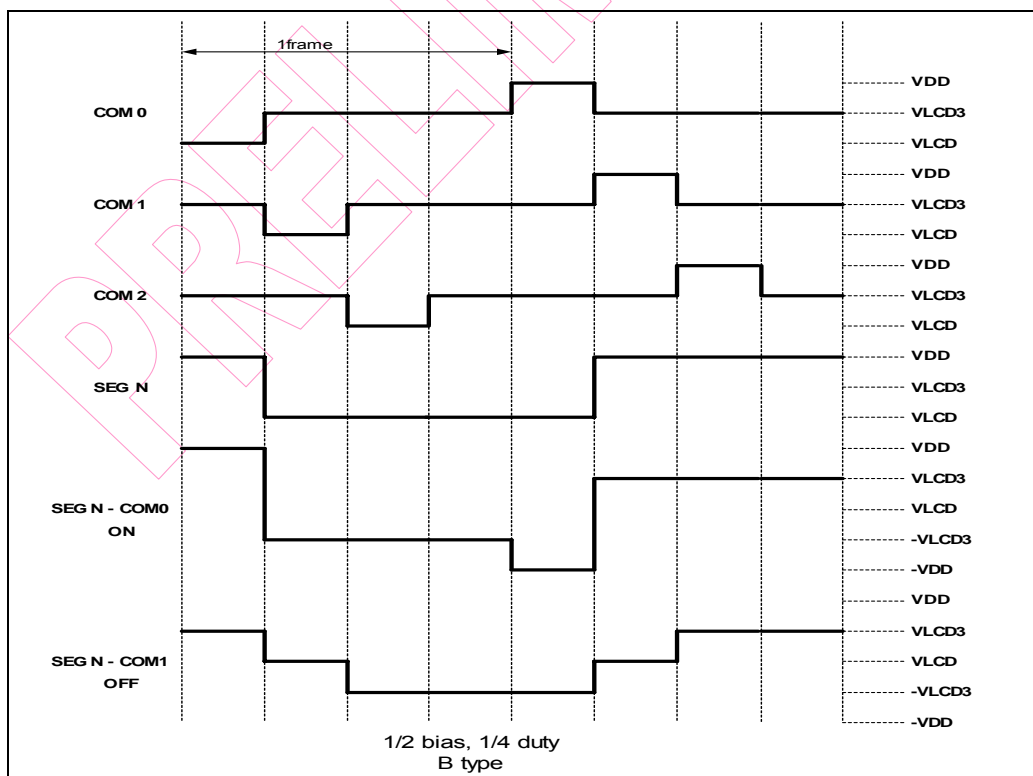
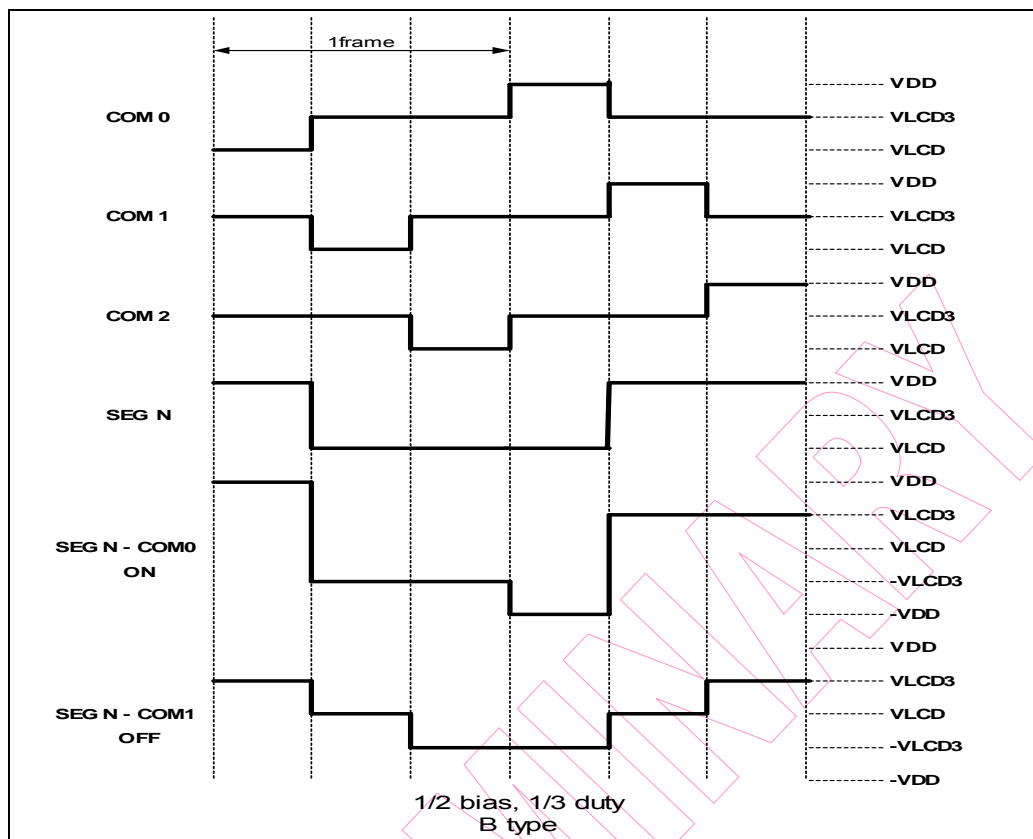
| LCDC1 | LCDC0 | F _m | F _{LCD} |
|-------|-------|----------------|--------------------------------|
| 0 | 0 | 16M | F _c /2 ⁹ |
| 0 | 1 | 8M | F _c /2 ⁸ |
| 1 | 0 | 4M | F _c /2 ⁷ |
| 1 | 1 | 2M | F _c /2 ⁶ |

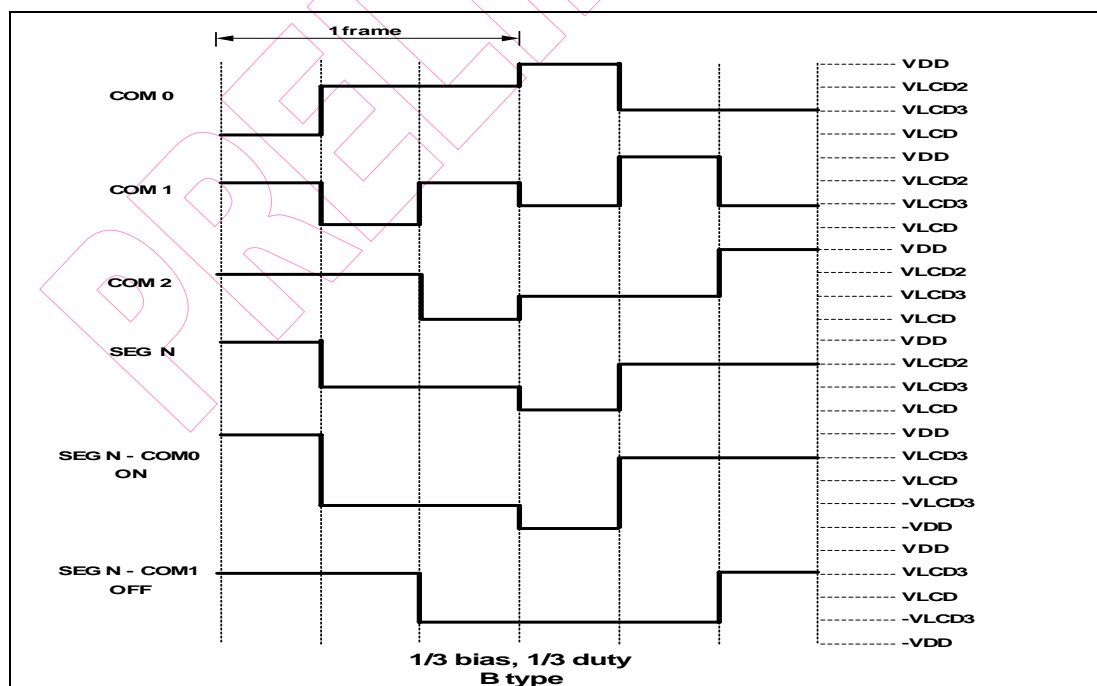
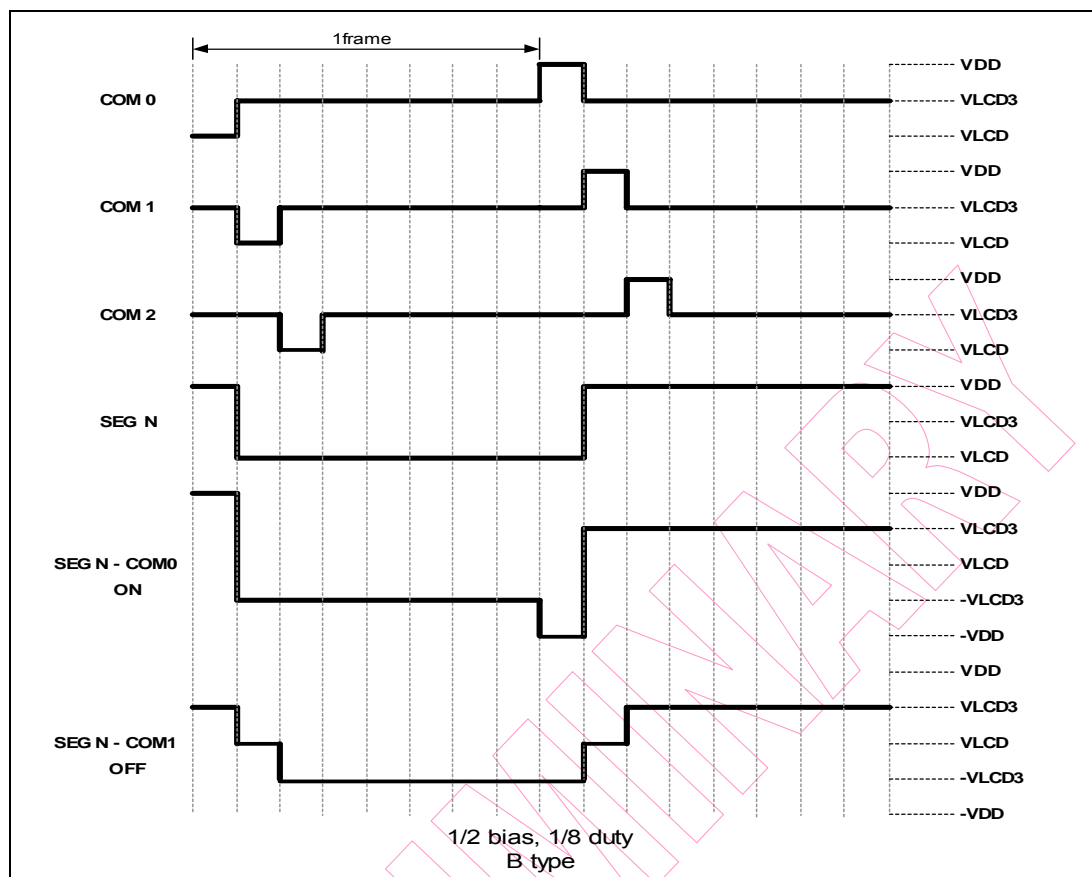
When the main oscillator operates in crystal mode and there is no sub-oscillator, it is a must to set these two bits used for LCD clock.

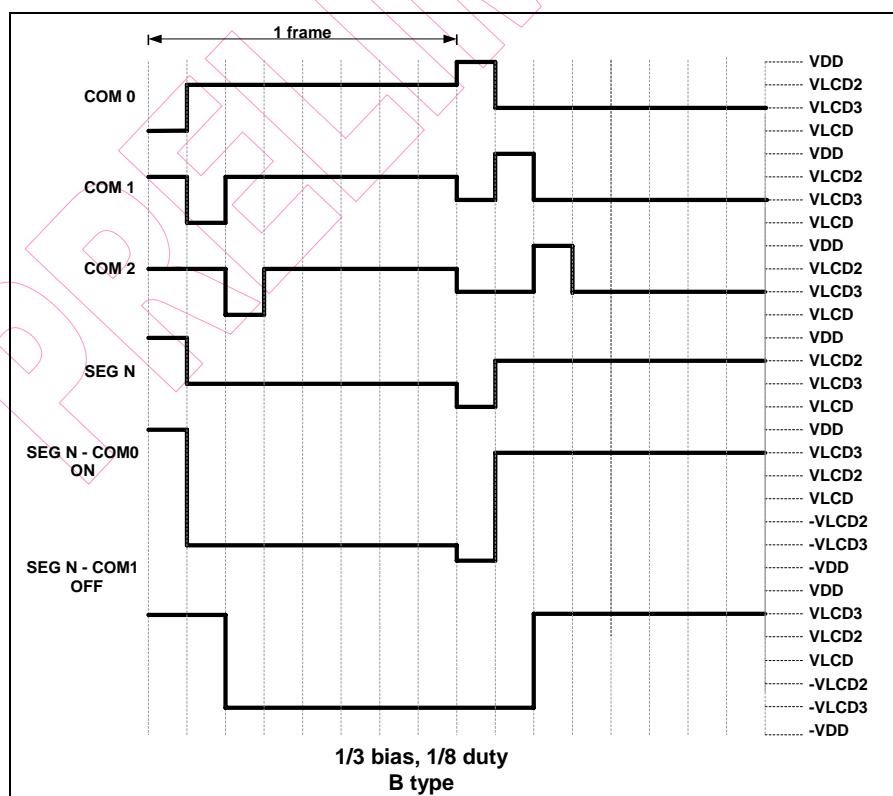
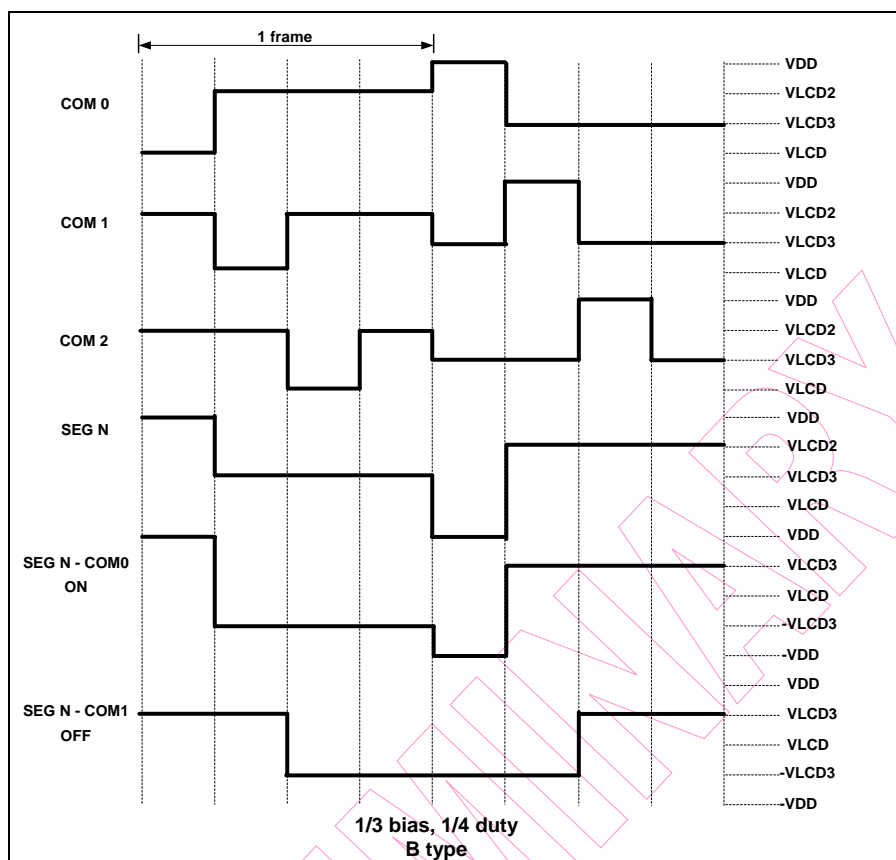
Bit 2~0 (LCDVC2~LCDVC0): LCD Voltage Control Bits

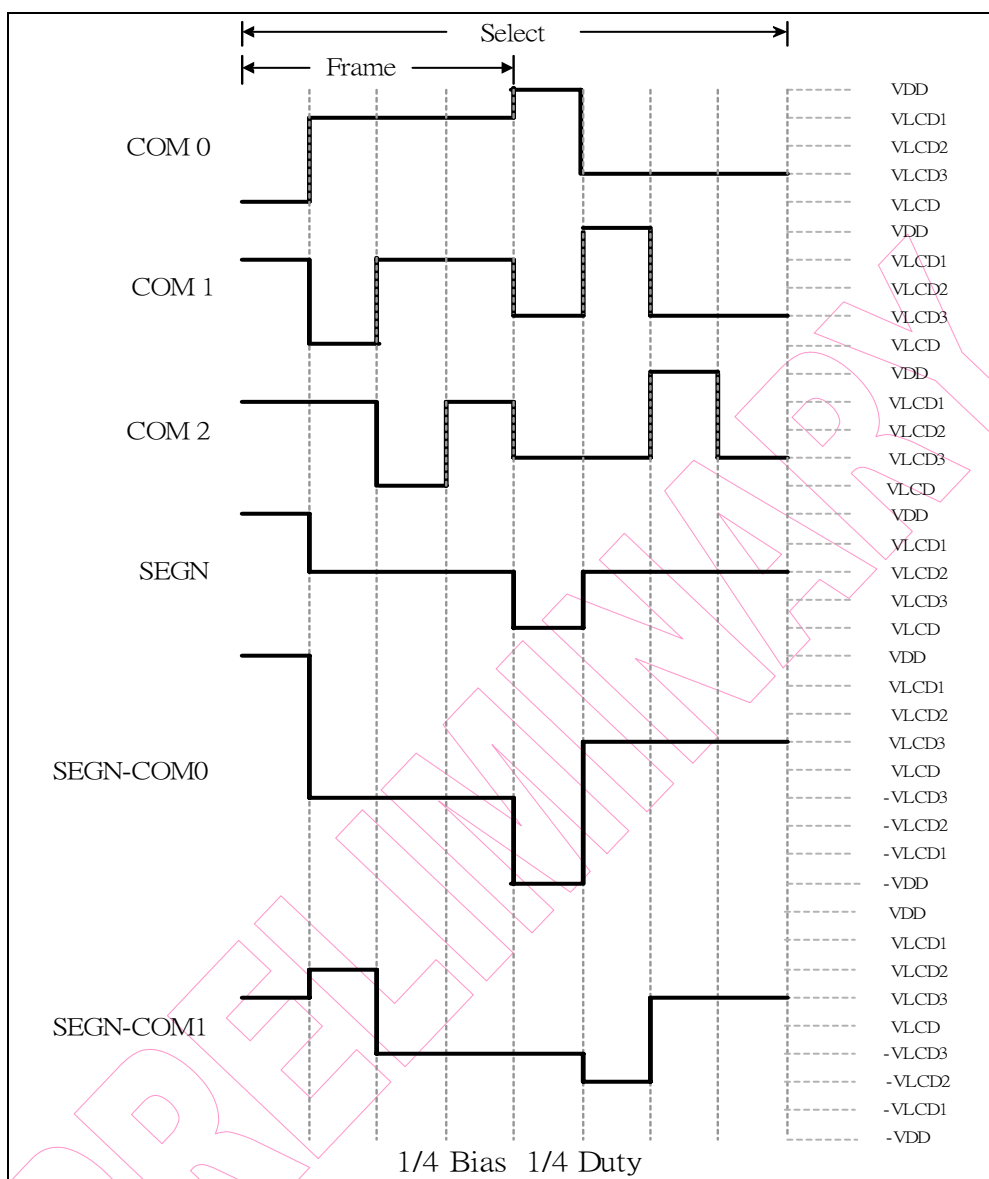
| LCDVC2 | LCDVC1 | LCDVC0 | Output |
|--------|--------|--------|---------------|
| 0 | 0 | 0 | 0.4VDD ~ VDD |
| 0 | 0 | 1 | 0.34VDD ~ VDD |
| 0 | 1 | 0 | 0.26VDD ~ VDD |
| 0 | 1 | 1 | 0.18VDD ~ VDD |
| 1 | 0 | 0 | 0.13VDD ~ VDD |
| 1 | 0 | 1 | 0.07VDD ~ VDD |
| 1 | 1 | 0 | 0.04VDD ~ VDD |
| 1 | 1 | 1 | 0V ~ VDD |

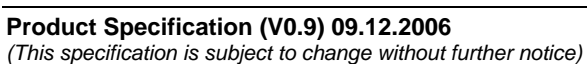












6.10 A/D Converter

Registers for AD Converter Circuit

| R_BANK | Address | NAME | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|---------|-------|-------|--------|--------|--------|-------|-------|-------|-------|
| Bank 3 | 0X09 | ADCR | ADRUN | ADP | ADCK1 | ADCK0 | ADIS3 | ADIS2 | ADIS1 | ADIS0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 3 | 0x0A | ADICH | CALI | ADREF | | | ADE11 | ADE10 | ADE9 | ADE8 |
| | | | R/W | R/W | | | R/W | R/W | R/W | R/W |
| Bank 3 | 0X0B | ADICL | ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 3 | 0X0C | ADDH | ADD11 | ADD10 | ADD9 | ADD8 | ADD7 | ADD6 | ADD5 | ADD4 |
| | | | R | R | R | R | R | R | R | R |
| Bank 3 | 0X0D | ADDL | SIGN | VOF[2] | VOF[1] | VOF[0] | ADD3 | ADD2 | ADD1 | ADD0 |
| | | | R/W | R/W | R/W | R/W | R | R | R | R |
| Bank 0 | 0x0E | IMR | T1IE | LVDIE | ADIE | SPIE | URTIE | EXIE9 | EXIE8 | TCIE |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x0F | ISR | T1IF | LVDIF | ADIF | SPIF | URTIF | EXIF9 | EXIF8 | TCIF |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

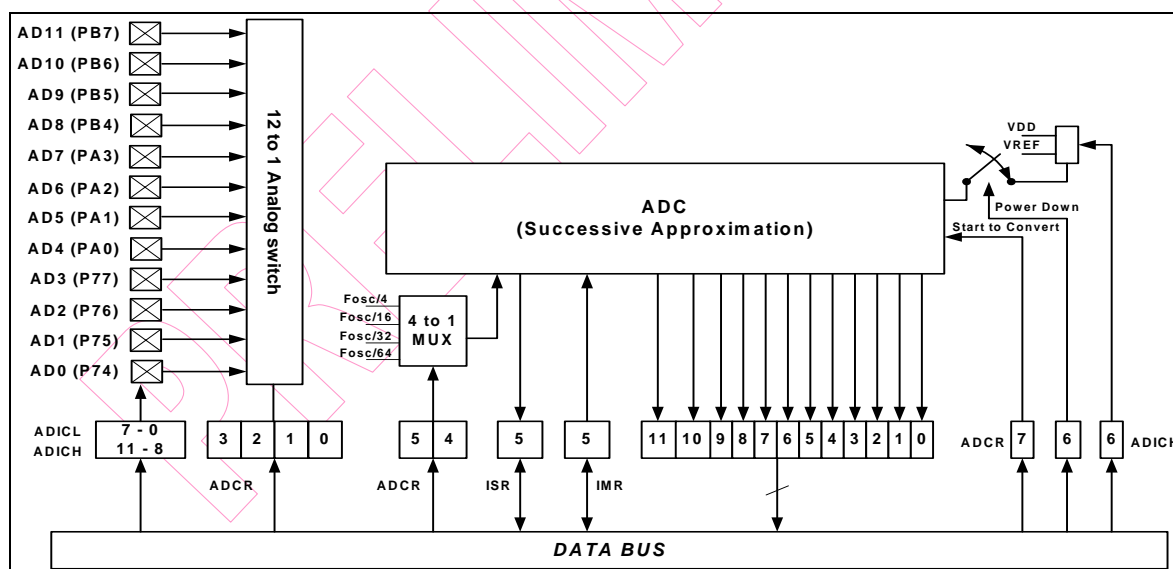


Fig. 6-16 AD Converter

This is a 12-bit successive approximation type AD converter. The upper side of analog reference voltage can select either internal VDD or external input pin P84 (VREF) by setting the ADREF bit in ADICH.

6.10.1 ADC Data Register

When the A/D conversion is completed, the result is loaded to the ADDH (8-bit) and ADDL (4-bit). The START/END bit is cleared, and the ADIF is set.

6.10.2 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation A/D converter are dependent on the properties of the ADC. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2 μ s for each K Ω of the analog source impedance and at least 2 μ s for the low-impedance source. The maximum recommended impedance for the analog source is 10K Ω at VDD = 5V. After the analog input channel is selected, this acquisition time must be done before A/D conversion can be started.

6.10.3 A/D Conversion Time

ADCK0 and ADCK1 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at maximum frequency without sacrificing accuracy of A/D conversion. For the EM78P510N, the conversion time per bit is about 4 μ s. Table 8 shows the relationship between Tct and the maximum operating frequencies.

Table 8

| ADCK1:0 | Operation Mode | Max. Frequency (Fc) | Max. Conversion Rate per Bit | Max. Conversion Rate |
|---------|----------------|---------------------|------------------------------|----------------------|
| 0 0 | Fc/4 | 1MHz | 250kHz (4 μ s) | 56us(17.86kHz) |
| 0 1 | Fc/16 | 4MHz | 250kHz (4 μ s) | 56us(17.86kHz) |
| 1 0 | Fc/32 | 8MHz | 250kHz (4 μ s) | 56us(17.86kHz) |
| 1 1 | Fc/64 | 16MHz | 250kHz (4 μ s) | 56us(17.86kHz) |

6.11 UART (Universal Asynchronous Receiver/Transmitter)

Registers for UART Circuit

| R_BANK | Address | NAME | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|---------|-------|--------|--------|--------|--------|--------|--------|--------|-------|
| Bank 3 | 0X05 | URC | URTD8 | UMODE1 | UMODE0 | BRATE2 | BRATE1 | BRATE0 | UTBE | TXE |
| | | | W | R/W | R/W | R/W | R/W | R/W | R | R/W |
| Bank 3 | 0X06 | URS | URRD8 | EVEN | PRE | PRERR | OVERR | FMERR | URBF | RXE |
| | | | R | R/W | R/W | R | R | R | R | R/W |
| Bank 3 | 0X07 | URRD | URRD7 | URRD6 | URRD5 | URRD4 | URRD3 | URRD2 | URRD1 | URRD0 |
| | | | R | R | R | R | R | R | R | R |
| Bank 3 | 0X08 | URTD | URTD 7 | URTD 6 | URTD 5 | URTD 4 | URTD 3 | URTD 2 | URTD 1 | URTD0 |
| | | | W | W | W | W | W | W | W | W |
| Bank 5 | 0x06 | UARC2 | | | UARTE | | UINVEN | | | |
| | | | | | R/W | | R/W | | | |
| Bank 0 | 0x0E | IMR | T1IE | LVDIE | ADIE | SPIE | URTIE | EXIE9 | EXIE8 | TCIE |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x0F | ISR | T1IF | LVDIF | ADIF | SPIF | URTIF | EXIF9 | EXIF8 | TCIF |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

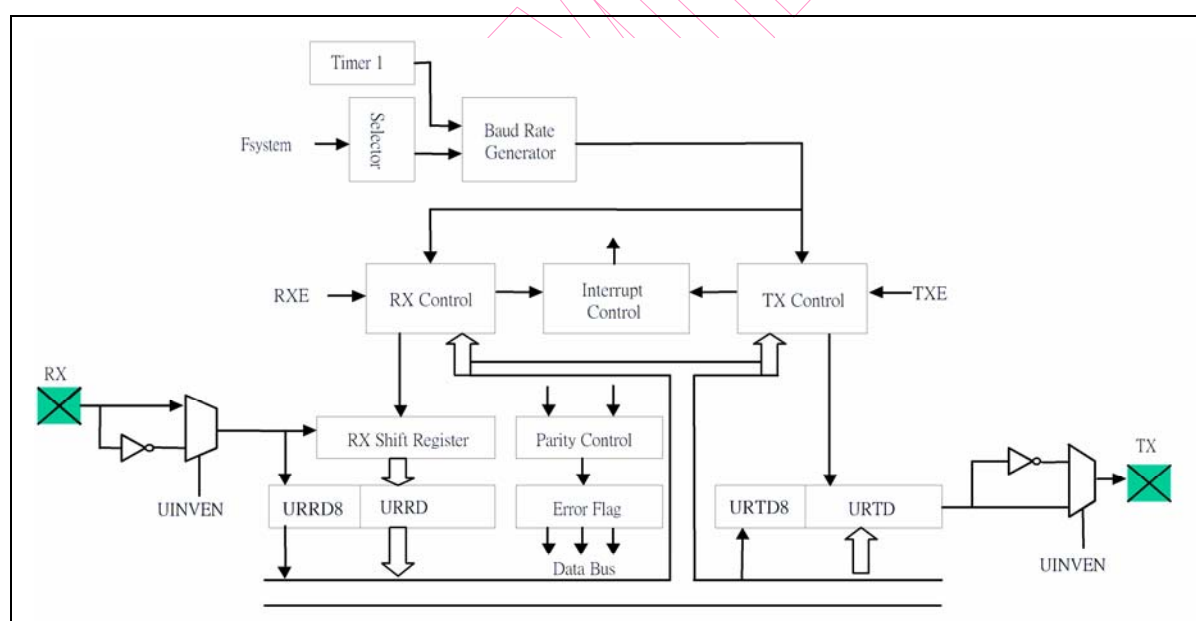


Fig 6-17 Function Block Diagram

In Universal Asynchronous Receiver Transmitter (UART), each transmitted or received character is individually synchronized by framing it with a start bit and stop bit.

Full duplex data transfer is possible since the UART has independent transmit and receive sections. Double buffering for both sections allows the UART to be programmed for continuous data transfer.

The figure below shows the general format of one character sent or received. The communication channel is normally held in the marked state (high). Character transmission or reception starts with a transition to the space state (low).

The first bit transmitted or received is the start bit (low). It is followed by the data bits, in which the least significant bit (LSB) comes first. The data bits are followed by the parity bit. If present, then the stop bit or bits (high) confirm the end of the frame.

In receiving, the UART synchronizes on the falling edge of the start bit. When two or three "0" are detected during three samples, it is recognized as normal start bit and the receiving operation is started.

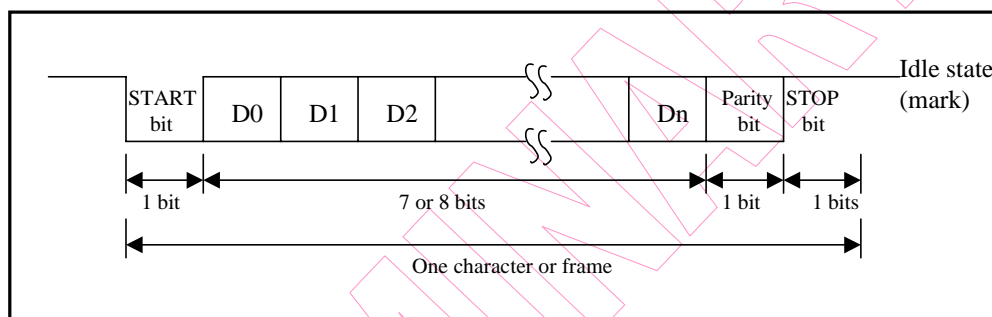


Fig 6-18 Data Format in UART

6.11.1 UART Mode

There are three UART modes. Mode 1 (7 bits data) and Mode 2 (8 bits data) allow the addition of a parity bit. The parity bit addition is not available in Mode 3. Figure 6-19 below shows the data format in each mode.

| | UMODE | PRE | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|--------|-------|-----|---|---|-------------------------------|---|---|---|---|---|---|---|----|----|
| Mode 1 | { | 0 | 0 | 0 | START 7 bits DATA STOP | | | | | | | | | |
| | | 0 | 0 | 1 | START 7 bits DATA Parity STOP | | | | | | | | | |
| Mode 2 | { | 0 | 1 | 0 | START 8 bits DATA STOP | | | | | | | | | |
| | | 0 | 1 | 1 | START 8 bits DATA Parity STOP | | | | | | | | | |
| Mode 3 | | 1 | 0 | X | START 9 bits DATA STOP | | | | | | | | | |

Fig 6-19 UART Model

6.11.2 Transmitting

In transmitting serial data, the UART operates as follows:

1. Set the TXE bit of the URC register to enable the UART transmission function.
2. Write data into the URTD register and the UTBE bit of the URC register will be set by hardware.
3. Then start transmitting.
4. Serially transmitted data are transmitted in the following order from the TX pin.
5. Start bit: one "0" bit is output.
6. Transmit data: 7, 8 or 9 bits data are output from the LSB to the MSB.
7. Parity bit: one parity bit (odd or even selectable) is output.
8. Stop bit: one "1" bit (stop bit) is output.

Mark state: output "1" continues until the start bit of the next transmitted data.

After transmitting the stop bit, the UART generates a TBEF interrupt (if enabled).

6.11.3 Receiving

In receiving, the UART operates as follows:

1. Set RXE bit of the URS register to enable the UART receiving function. The UART monitors the RX pin and synchronizes internally when it detects a start bit.
2. Receive data is shifted into the URRD register in the order from LSB to MSB.
3. The parity bit and the stop bit are received. After one character is received, the URBF bit of the URS register will be set to 1. This means UART interrupt will occur.
4. The UART makes the following checks:
 - (a) Parity check: The number of 1 of the received data must match the even or odd parity setting of the EVEN bit in the URS register.
 - (b) Frame check: The start bit must be 0 and the stop bit must be 1.
 - (c) Overrun check: The URBF bit of the URS register must be cleared (that means the URRD register should be read out) before the next received data is loaded into the URRD register.

If any checks failed, the URTIF interrupt will be generated (if enabled), and an error flag is indicated in PRERR, OVERR or FMERR bit. The error flag should be cleared by software otherwise, URTIF interrupt will occur when the next byte is received.

5. Read received data from URRD register. And URBF bit will be cleared by hardware.

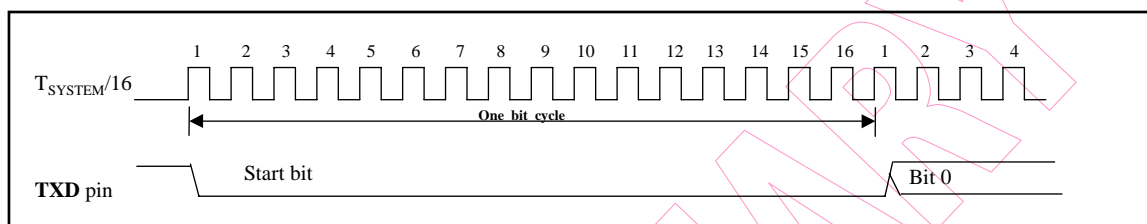
6.11.4 Baud Rate Generator

The baud rate generator is comprised of a circuit that generates a clock pulse to determine the transfer speed for transmission/reception in the UART.

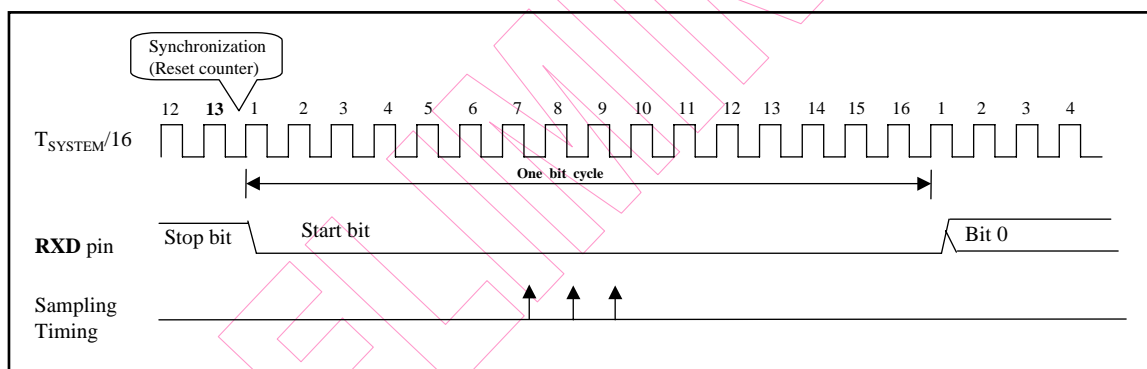
The BRATE2~BRATE0 bits of the URC register can determine the desired baud rate.

6.11.5 UART Timing

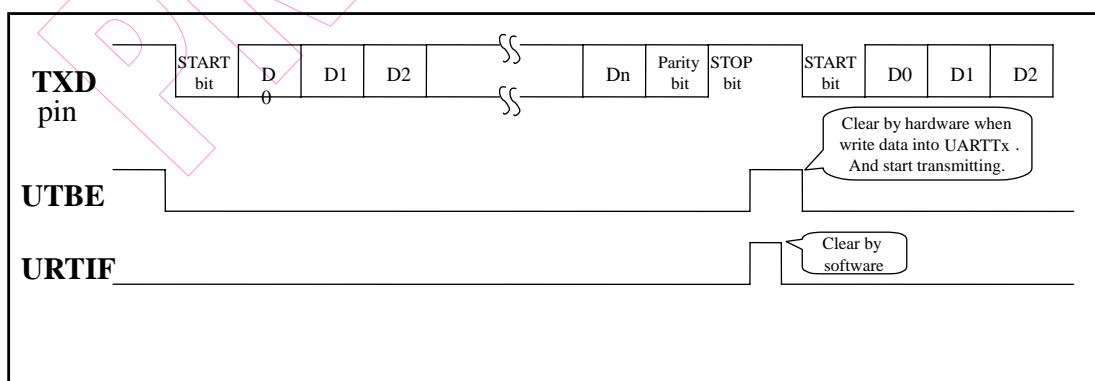
1. Transmission Counter Timing:



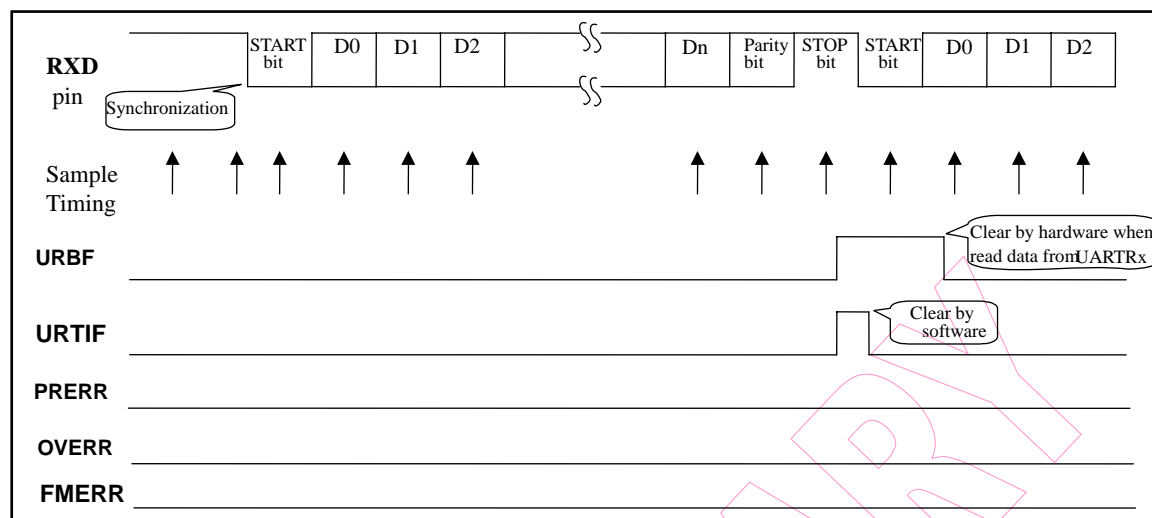
2. Receiving Counter Timing:



3. UART Transmit operation (8 bits data with parity bit):



4. UART Receive operation (8 bits data with parity and stop bit):



6.12 SPI (Serial Peripheral Interface)

6.12.1 Overview & Features

Overview:

Figures 6-20 and 6-21 show how the EM78P510N communicates with other devices through the SPI module. If the EM78P510N is a master controller, it sends the clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if the EM78P510N is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both the clock rate and the selected edge. You can also set SPIS Bit 7 (DORD) to determine the SPI transmission order, SPIC Bit 3 (SDOC) to control the SO pin after serial data output status and SPIS Bit 6 (TD1), Bit 5 (TD0) determines the SO status output delay times.

Features:

- Operation in either Master mode or Slave mode
- Full duplex, three-wire synchronous communication
- Programmable baud rates of communication
- Programming clock polarity, (RD Bit 7)
- Interrupt flag available for the read buffer full
- SPI transmission order
- After serial data output SDO status select
- SDO status output delay times
- Up to 8 MHz (maximum) bit frequency

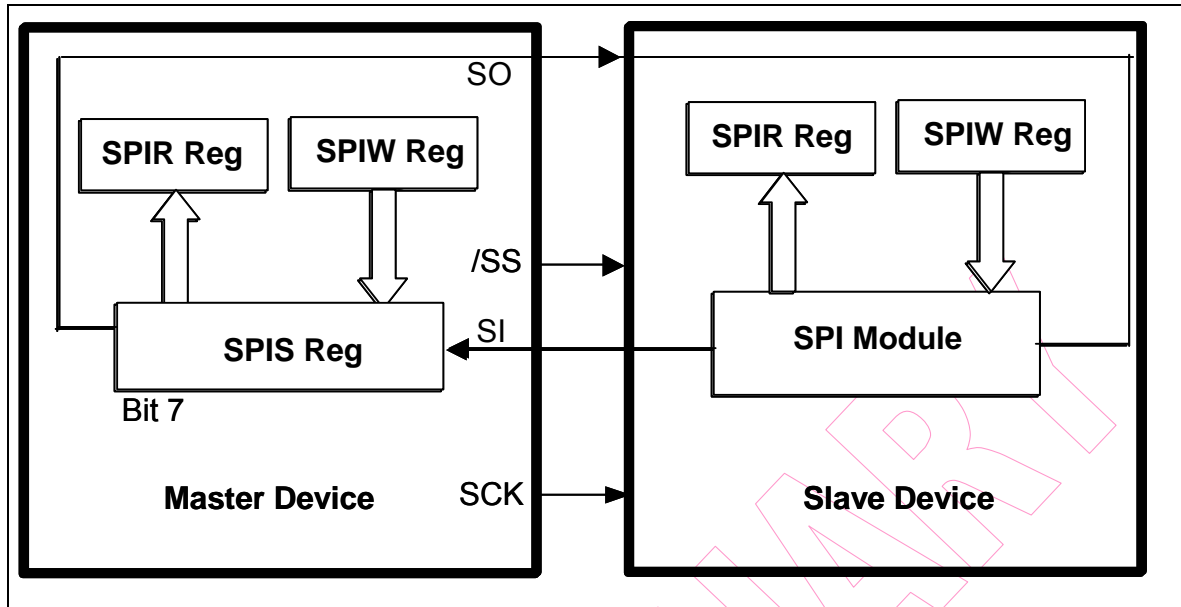


Fig. 6-20 SPI Master/Slave Communication

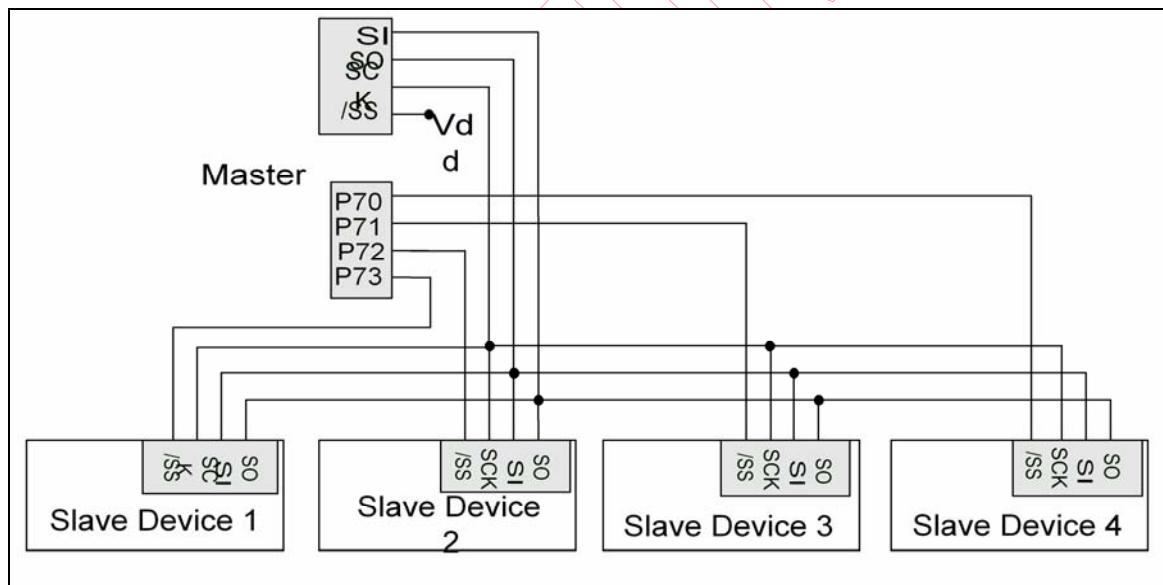


Fig. 6-21 SPI Configuration of Single-Master and Multi-Slave

6.12.2 SPI Function Description

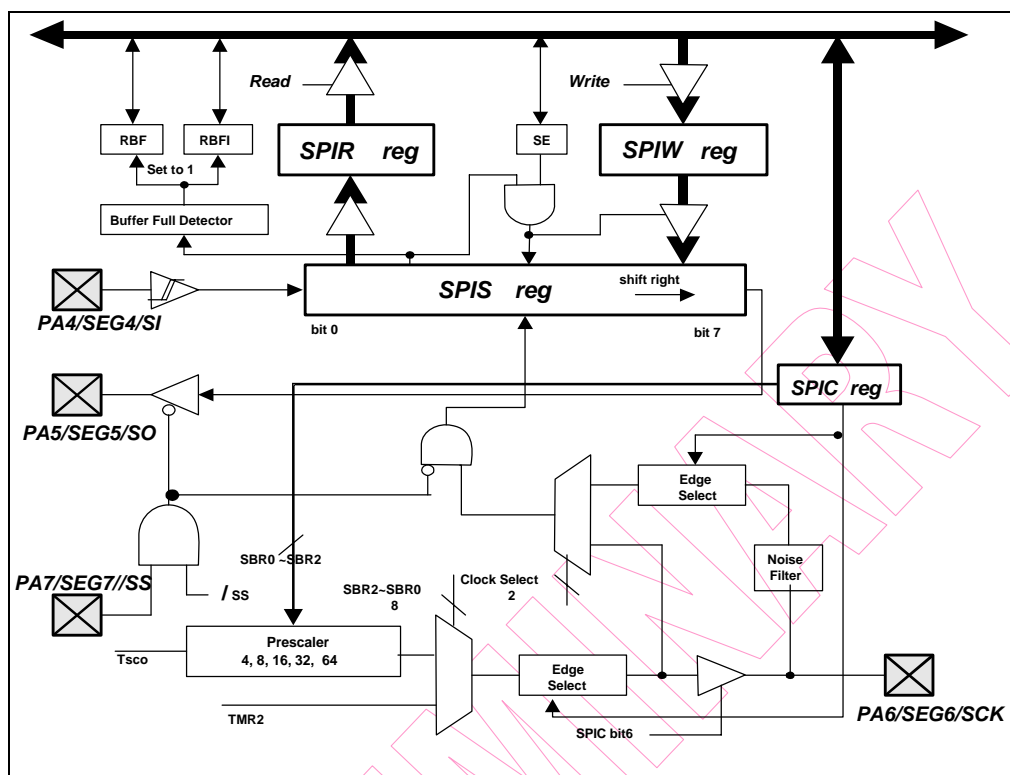


Fig. 6-22 SPI Block Diagram

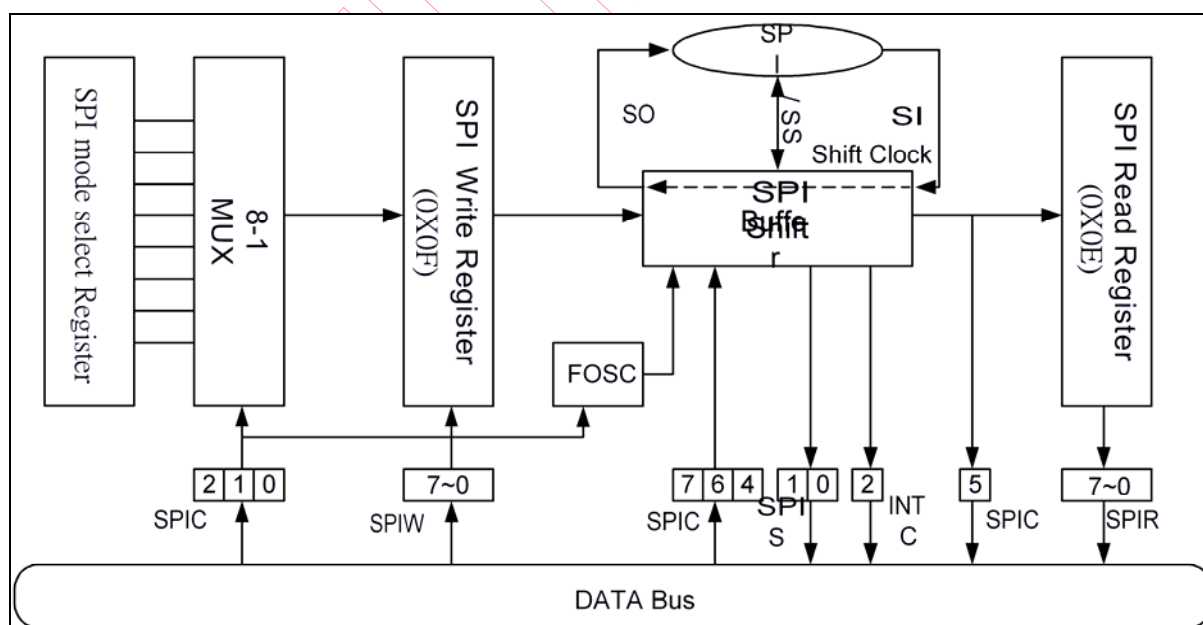


Fig. 6-23 The Function Block Diagram of SPI Transmission

Below are the functions of each block and explanations on how to carry out the SPI communication with the signals depicted in Fig.6-22 and Fig.6-23.

- PA4/SEG4/SI: Serial Data In
- PA5/SEG5/SO: Serial Data Out
- PA6/SEG6/SCK: Serial Clock
- PA7/SEG7//SS:/Slave Select (Option). This pin (/SS) may be required during a slave mode
- RBF: Set by Buffer Full Detector, and reset by software
- Buffer Full Detector: Set to 1 when an 8-bit shifting is completed.
- SSE: Loads the data in SPIS register, and begin to shift
- SPIS reg.: Shifting byte in and out. The MSB is shifted first. Both the SPIS and the SPIW registers are loaded at the same time. Once data are written, SPIS starts transmission / reception. The data received will be moved to the SPIR register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the RBFi (Read Buffer Full Interrupt) flag are then set.
- SPIR reg.: Read buffer. The buffer will be updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIR register reads.
- SPIW reg.: Write buffer. The buffer will deny any attempts to write until the 8-bit shifting is completed.

The SSE bit will be kept in "1" if the communication is still undergoing. This flag must be cleared as the shifting is completed. Users can determine if the next write attempt is available.

- SBRS2~SBRS0: Programming the clock frequency/rates and sources.
- Clock Select: Selecting either the internal or the external clock as the shifting clock.
- Edge Select: Selecting the appropriate clock edges by programming the CES bit

6.12.3 SPI Signal & Pin Description

The detailed functions of the four pins, SI, SO, SCK, and /SS are as follows:

PA4/SEG4/SI:

- Serial Data In,
- Receive sequentially, the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last,
- Defined as high-impedance, if not selected

- Program the same clock rate and clock edge to latch on both the master and slave devices
- The byte received will update the transmitted byte
- The RBF (located in Register 0x0C) will be set as the SPI operation is completed
- Timing is shown in Fig.6-23 and 6-24

PA5/SEG5/SO:

- Serial Data Out
- Transmit sequentially; the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last
- Program the same clock rate and clock edge to latch on both the master and slave devices
- The received byte will update the transmitted byte
- The CES (located in Register 0x0D) bit will be reset, as the SPI operation is completed
- Timing is shown in Fig.6-23 and 6-24

PA6/SEG6/SCK:

- Serial Clock
- Generated by a master device
- Synchronize the data communication on both the SI and SO pins
- The CES (located in Register 0x0D) is used to select the edge to communicate.
- The SBR0~SBR2 (located in Register 0x0D) is used to determine the baud rate of communication
- The CES, SBR0, SBR1, and SBR2 bits have no effect in slave mode
- Timing is show in Fig.6-23 and 6-24

PA7/SEG7//SS:

- Slave Select; negative logic
- Generated by a master device to signify the slave(s) to receive data
- Goes low before the first cycle of SCK appears, and remains low until the last (eighth) cycle is completed
- Ignores the data on the SI and SO pins while /SS is high, because the SO is no longer driven
- Timing is shown in Fig.6-23 and 6-24

Note:

1. The Priority of PA4/SEG4/SI Pin

| PA4/SEG4/SI Pin Priority | | |
|--------------------------|--------|-----|
| High | Medium | Low |
| SI | SEG4 | PA4 |

2. The Priority of PA5/SEG5/SO Pin

| PA5/SEG5/SO Pin Priority | | |
|--------------------------|--------|-----|
| High | Medium | Low |
| SO | SEG5 | PA5 |

3. The Priority of PA6/SEG6/SCK Pin

| PA6/SEG6/SCK Pin Priority | | |
|---------------------------|--------|-----|
| High | Medium | Low |
| SCK | SEG6 | PA6 |

4. The Priority of PA7/SEG7//SS PIN

| PA7/SEG7//SS Pin Priority | | |
|---------------------------|--------|-----|
| High | Medium | Low |
| /SS | SEG7 | PA7 |

6.12.4 Programming the Related Registers

Registers for the SPI Circuit

| R_BANK | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|---------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bank 2 | 0X0C | SPIS | DORD | TD1 | TD0 | - | OD3 | OD4 | - | RBF |
| | | | R/W | R/W | R/W | - | R/W | R/W | - | R |
| Bank 2 | 0X0D | SPIC | CES | SPIE | SRO | SSE | SDOC | SBR52 | SBR51 | SBR50 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 2 | 0X0E | SPIR | SRB7 | SRB6 | SRB5 | SRB4 | SRB3 | SRB2 | SRB1 | SRB0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 2 | 0X0F | SPIW | SWB7 | SWB6 | SWB5 | SWB4 | SWB3 | SWB2 | SWB1 | SWB0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| BANK 0 | 0x0E | IMR | T1IE | LVDIE | ADIE | SPIE | URTIE | EXIE9 | EXIE8 | TCIE |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x0F | ISR | T1IF | LVDIF | ADIF | SPIIF | URTIF | EXIF9 | EXIF8 | TCIF |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

As the SPI mode is defined, the related registers of this operation are shown.

Related Control Registers of the SPI Mode

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bank 2 0x0D | SPIC | CES | SPIE | SRO | SSE | SDOC | SBR2 | SBR1 | SBR0 |
| Bank 0 0x0E | IMR | T1IE | LVDIE | ADIE | SPIE | URTIE | EXIE9 | EXIE8 | TCIE |

SPIC: SPI Control Register

Bit 7 (CES): Clock Edge Select Bit

- 0** : Data shifts out on a rising edge, and shifts in on a falling edge. Data is on hold during a low-level.
- 1** : Data shifts out on a falling edge, and shifts in on a rising edge. Data is on hold during a high-level.

Bit 6 (SPIE): SPI Enable Bit

- 0** : Disable SPI mode
- 1** : Enable SPI mode

Bit 5 (SRO): SPI Read Overflow Bit

- 0** : No overflow
- 1** : A new data is received while the previous data is still being held in the SPIRB register. In the situation, the data in SPIR register will be destroyed. To avoid setting this bit, users are required to read the SPIRB register although only the transmission is implemented. This can only occur in slave mode.

Bit 4 (SSE): SPI Shift Enable Bit

- 0** : Resets as soon as the shift is completed, and the next byte is read to shift.
- 1** : Starts to shift, and remained on "1" while the current byte is still being transmitted.

Bit 3 (SDOC): SDO Output Status Control Bit

- 0** : After the serial data output, the SDO remain high.
- 1** : After the serial data output, the SDO remain low.

Bits 2~0 (SBR2~SBR0): SPI Baud Rate Select Bits

| SBR2 | SBR1 | SBR0 | Mode | SPI Baud Rate |
|------|------|------|--------|---------------|
| 0 | 0 | 0 | Master | Fosc/2 |
| 0 | 0 | 1 | Master | Fosc/4 |
| 0 | 1 | 0 | Master | Fosc/8 |
| 0 | 1 | 1 | Master | Fosc/16 |
| 1 | 0 | 0 | Master | Fosc/32 |
| 1 | 0 | 1 | Master | Timer2 |
| 1 | 1 | 0 | Slave | /SS enable |
| 1 | 1 | 1 | Slave | /SS disable |

IMR: Interrupt Mask Register

Bit 4 (SPIE): Interrupt Enable Bit

0 : disable SPIF interrupt

1 : enable SPIF interrupt

Related Status/Data Registers of the SPI Mode

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0X0C | SPIS | DORD | TD1 | TD0 | - | OD3 | OD4 | - | RBF |
| 0x0E | SPIR | SRB7 | SRB6 | SRB5 | SRB4 | SRB3 | SRB2 | SRB1 | SRB0 |
| 0x0F | SPIW | SWB7 | SWB6 | SWB5 | SWB4 | SWB3 | SWB2 | SWB1 | SWB0 |

SPIS: SPI Status Register

Bit 7 (DORD): Data Shift Control Bit

0 : Shift left (MSB first)

1 : Shift right (LSB first).

Bits 6~5 (TD1~TD0): SDO Status Output Delay Times Options

| TD1 | TD0 | Delay Time |
|-----|-----|------------|
| 0 | 0 | 8 CLK |
| 0 | 1 | 16 CLK |
| 1 | 0 | 24 CLK |
| 1 | 1 | 32 CLK |

Bit 4: Reserved

Bit 3 (OD3): Open-Drain Control Bit

1 : Open-drain enable for SDO

0 : Open-drain disable for SDO.

Bit 2 (OD4): Open-Drain Control Bit

1 : Open-drain enable for SCK

0 : Open-drain disable for SCK.

Bit 1: Reserved

Bit 0 (RBF): Read Buffer Full Flag

1 : Receiving completed, and SPIRB is fully exchanged.

0 : Receiving not completed, and SPIRB has not fully exchanged.

SPIRB: SPI Read Buffer. Once the serial data is received completely, it will load to SPIRB from SPIS register. The RBF bit in the SPIS register will also be set.

SPIWB: SPI Write Buffer. As a transmitted data is loaded, the SPIS register stands by and start to shift the data when sensing SCK edge with SSE set to "1".

6.12.5 SPI Mode Timing

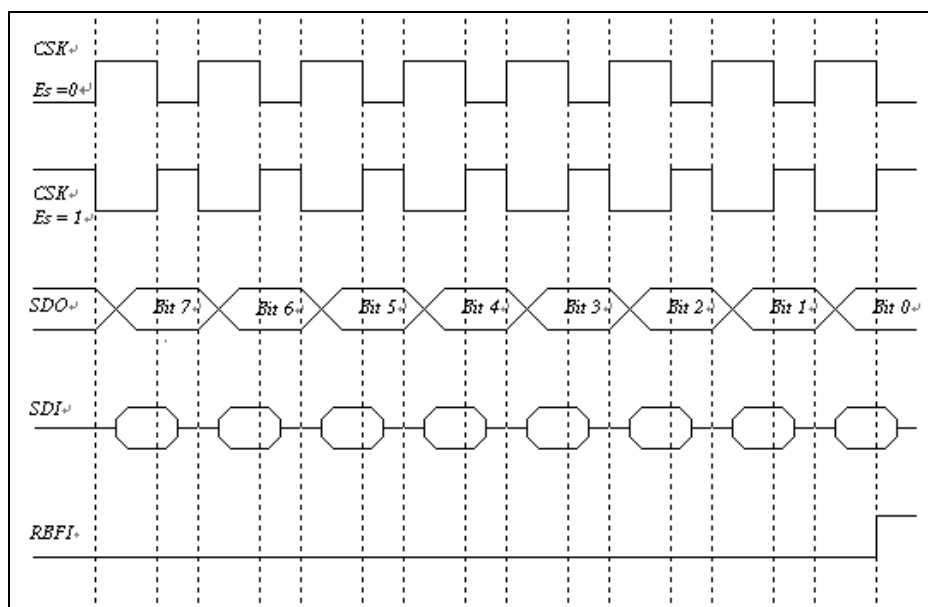


Fig. 6-24 SPI Mode with /SS Disabled

The SCK edge is selected by programming bit CES. The waveform shown in Fig.6-24 is applicable regardless of whether the EM78P510N is in master or slave mode with /SS disabled. However, the waveform in Fig.6-25 can only be implemented in slave mode with /SS enabled.

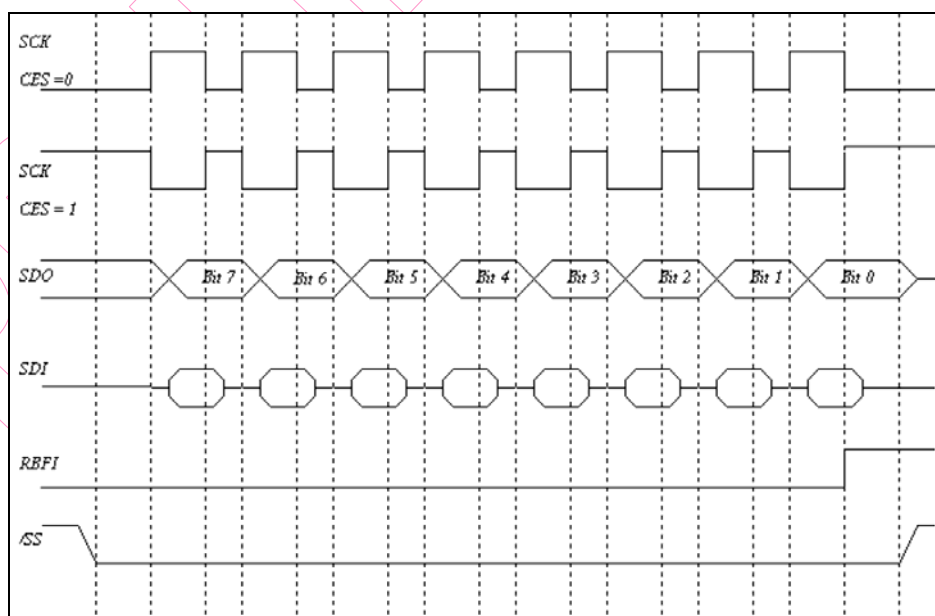


Fig. 6-25 SPI Mode with /SS Enabled

6.13 Timer/Counter 1

Registers for Timer/Counter 1 Circuit

| R_BANK | Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|---------|-------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Bank 2 | 0X05 | T1CR | TIS1 | TIS0 | T1MS2 | T1MS1 | T1MS0 | T1P2 | T1P1 | T1P0 |
| | | | W | W | W | W | W | W | W | W |
| Bank 2 | 0X06 | TSR | T1MOD | TRCB | T1CSS1 | T1CCS0 | T2CCS | T1EN | T1OMS | T1OC |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 2 | 0X07 | T1PD | PRD1[7] | PRD1[6] | PRD1[5] | PRD1[4] | PRD1[3] | PRD1[2] | PRD1[1] | PRD1[0] |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 2 | 0X08 | T1TD | TD1[7] | TD1[6] | TD1[5] | TD1[4] | TD1[3] | TD1[2] | TD1[1] | TD1[0] |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x0E | IMR | T1IE | LVDIE | ADIE | SPIE | URTI | EXIE9 | EXIE8 | TCIE |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 0 | 0x0F | ISR | T1IF | LVDIF | ADIF | SPIF | URTI | EXIF9 | EXIF8 | TCIF |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

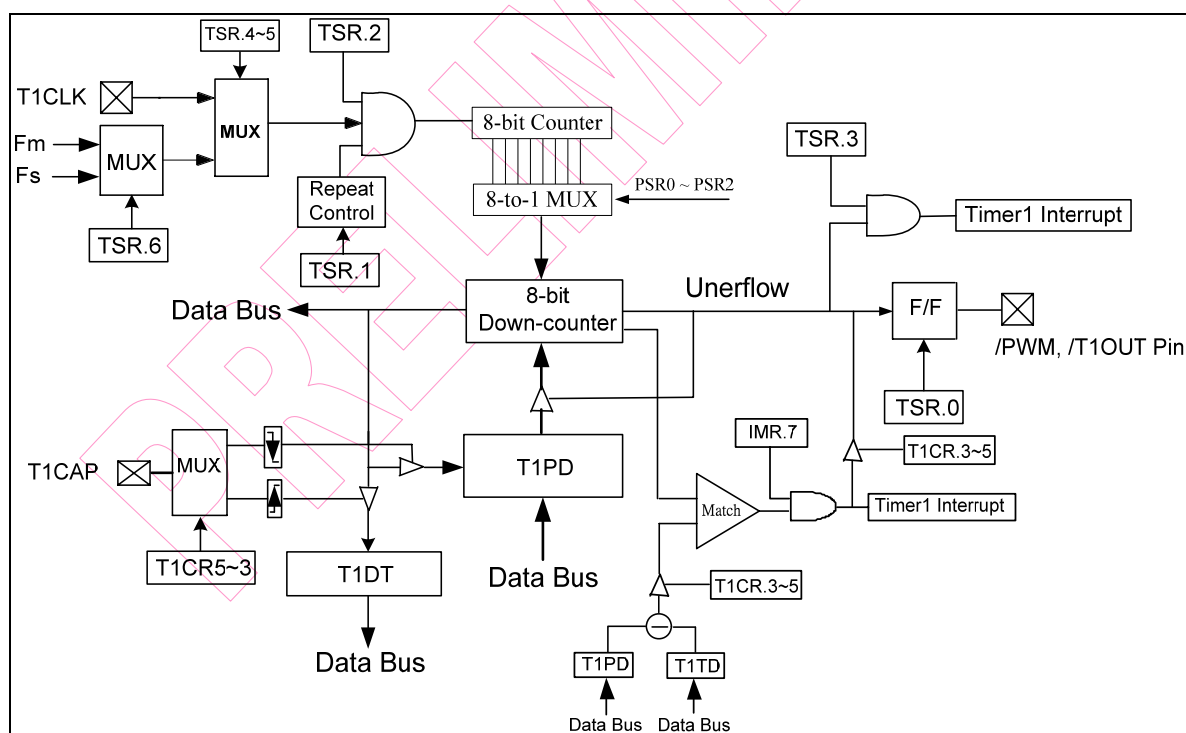


Fig. 6-26 Timer/Counter 1 Configuration

6.13.1 Timer Mode

In Timer mode, counting down is performed using the internal clock. The down-counter value auto reloads from T1PD. When the contents of the down-counter underflows, interrupt is generated and the counter is cleared. Counting down resumes after the counter is cleared.

6.13.2 T1OUT Mode

In Timer 1 underflow Output mode, counting down is performed using the internal clock with prescaler or External clock through T1CLK Pin or Sub Frequency with prescaler. The counter value is loaded from T1PD, when the counter underflows. The F/F output is toggled and the counter is auto-reloaded from T1PD, each time an overflow is found. The F/F output is inverted and output to /T1OUT pin. This mode can generate 50% duty pulse output. The program can initialize the F/F and it is initialized to "0" during a reset. A T1OUT interrupt is generated each time the /T1OUT output is toggled.

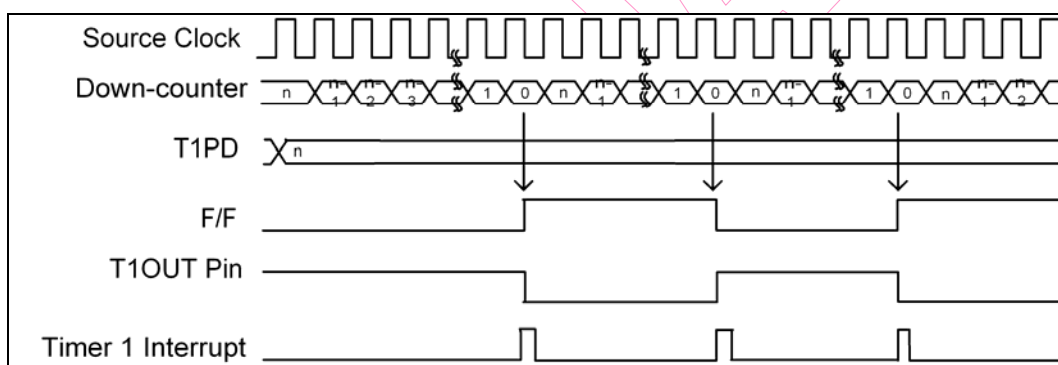


Fig 6-27 T1OUT Mode Timing Chart

6.13.3 Capture Mode

In Capture mode, the pulse width, period and duty of the T1CAP input pin are measured in this mode, which can be used in decoding the remote control signal. The counter is free running by the internal clock. On the rising (falling) edge of T1CAP pin input, the contents of the counter is loaded into T1PD, then the counter is cleared and interrupt is generated. On the falling (rising) edge of T1CAP pin input, the contents of the counter are loaded into T1TD. The counter is still counting, on the next rising edge of the T1CAP pin input, the contents of the counter are loaded into T1PD, counter is cleared and interrupt is generated again. If an overflow occurs before the edge is detected, the 00H is loaded into T1PD and an underflow interrupt is generated. During interrupt processing, it can be determined whether or not there is an overflow by checking whether the T1PD value is 00H. After an interrupt (capture to T1PD or overflow detection) is generated, capture and underflow detection are halted until T1PD is read out.

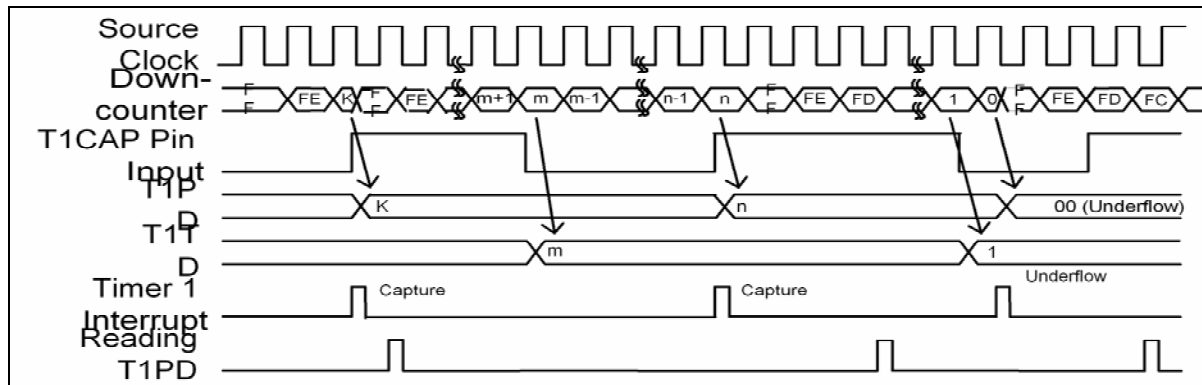


Fig 6-28 Capture Mode Timing Chart

6.13.4 PWM Mode

In Pulse Width Modulation (PWM) Output mode, counting down is performed using the internal clock with prescaler or external clock through T1CLK Pin or Sub Frequency with prescaler. The Duty of PWM1 control by T1TD, and the period of PWM1 control by T1PD. The pulse at the PWM1 pin is held to high level as long as the counter value of T1TD greater than or equal to zero, while the pulse is held to low level until the counter value of T1PD is underflow. The F/F is toggled when underflow. The counter is still counting, the F/F is toggled again when the counter underflows, then the counter is auto reload from T1PD. The F/F output is inverted and output to the /PWM pin. A Timer1 interrupt is generated each time an underflow occurs. T1PD is configured as a 2-stage shift register and, during output, will not switch until one output cycle is completed even if T1PD is overwritten. Therefore, the output can be changed continuously. T1PD is also shifted the first time by setting T1S to "1" after data is loaded to T1PD.

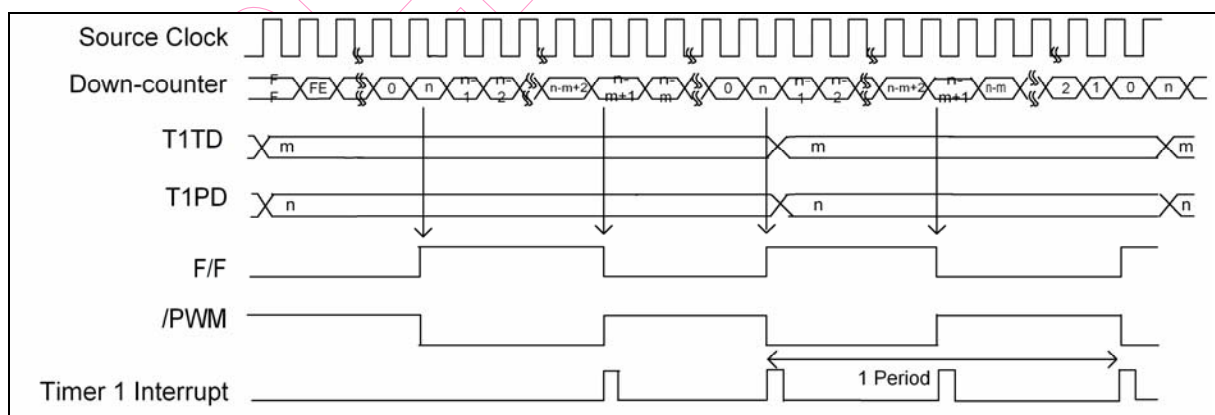


Fig 6-29 PWM Mode Timing Chart

6.13.5 16-Bit Mode

In 16-bit timer mode, all function in Timer 1 resolution become 16 bits.

6.14 Timer 2

Registers for Timer/Counter 2 Circuit

| R_BANK | Address | NAME | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|---------|------|---------|---------|---------|---------|---------|---------|---------|---------|
| Bank 2 | 0X06 | TSR | T1MOD | TRCB | T1CSS1 | T1CCS0 | T2CCS | T1EN | T1OMS | T1OC |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 2 | 0X09 | T2CR | T2IF | T2IE | T2EN | T2MS1 | T2MS0 | T2P2 | T2P1 | T2P0 |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 2 | 0X0A | T2PD | PRD2[7] | PRD2[6] | PRD2[5] | PRD2[4] | PRD2[3] | PRD2[2] | PRD2[1] | PRD2[0] |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bank 2 | 0X0B | T2TD | TD2[7] | TD2[6] | TD2[5] | TD2[4] | TD2[3] | TD2[2] | TD2[1] | TD2[0] |
| | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

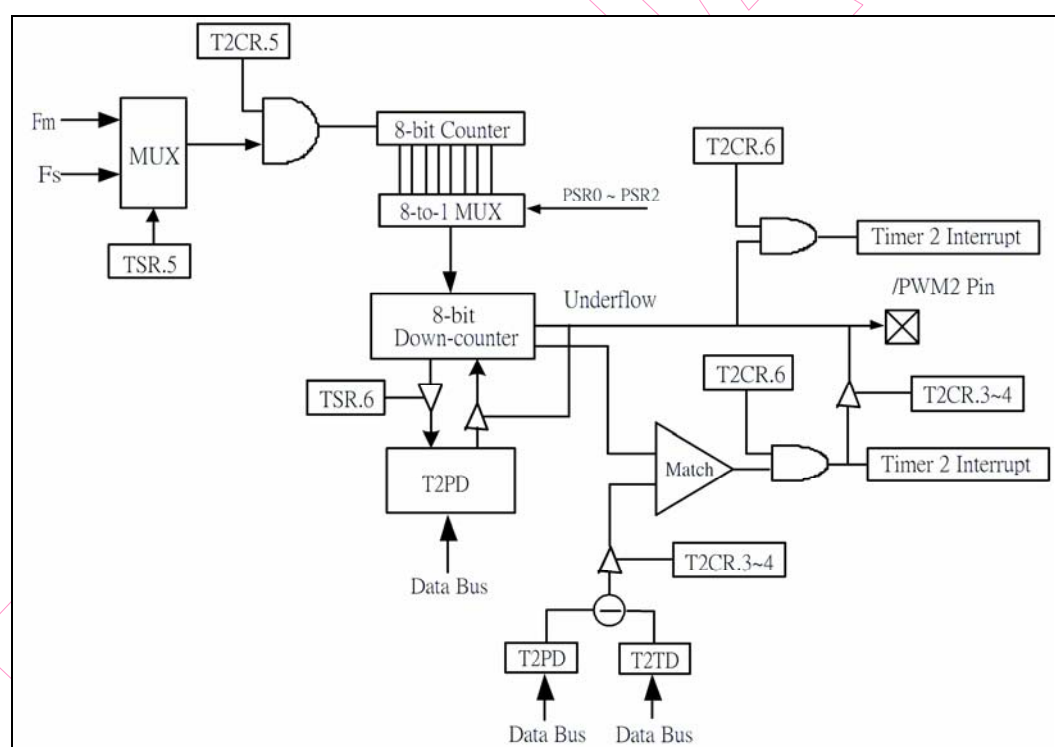


Fig 6-30 Timer 2 Configuration

6.14.1 Timer Mode

In Timer mode, counting down is performed using the internal clock with prescaler. When the counter value from T2PD underflows, interrupt is then generated and the counter is cleared. Counting down resumes after the counter is cleared. The counter value will automatically reload from T2PD.

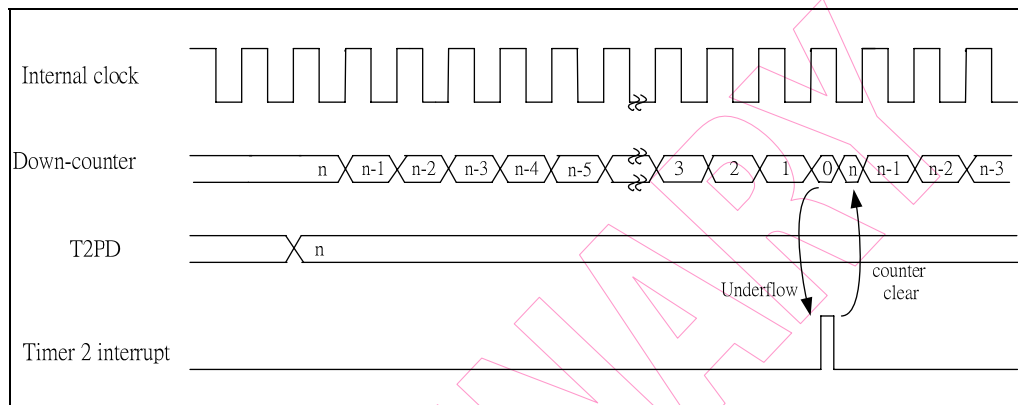


Fig 6-31 Timer Mode Timing Chart

6.14.2 PWM Mode

In Pulse Width Modulation (PWM) Output mode, counting down is performed using the internal clock with prescaler or Fsub with frequency. The PWM2 duty cycle is controlled by T2TD, and the PWM2 period is controlled by T2PD. The pulse at the PWM2 pin is held to high level as long as the T2TD counter value is greater than or equal to zero while the pulse is held to low level until the T2PD counter value underflows.

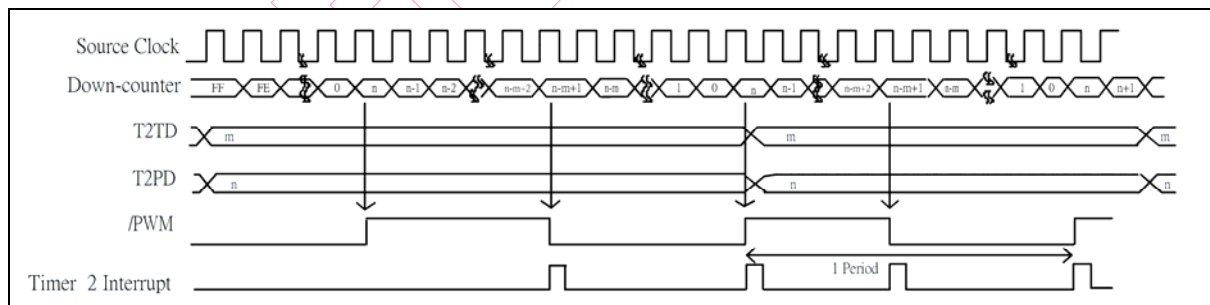


Fig 6-32 PWM Mode Timing Chart

6.15 Code Options

The EM78P510N has one Code Option word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

| Word 0 | Word1 | Word 2 |
|--------------|--------------|--------------|
| Bit 12~Bit 0 | Bit 12~Bit 0 | Bit 12~Bit 0 |

1. Code Option Register (Word 0)

| Word 0 | | | | | | | | | | | | |
|--------|--------|--------|-------|-------|--------|-------|-------|-------|-------|-------|-------|-------|
| Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| TYPE1 | TYPE0 | LVREN | LVR1 | LVR0 | ENWDTB | FSMD | FMMD1 | FMMD0 | HLP | PR2 | PR1 | PR0 |

Bits 12~11 (TYPE1~TYPE0): Type Selection for 48 pins or 44 pins or 42 pins or 32 pins.

| TYPE1 | TYPE0 | Type Selection |
|-------|-------|----------------------------------|
| 0 | 0 | EM78P510 (32-pin SDIP/SOP) |
| 0 | 1 | EM78P510 (42-pin DIP) |
| 1 | 0 | EM78P510 (44-pin LQFP/QFP) |
| 1 | 1 | EM78P510 (48-pin LQFP) (default) |

Bit 10 (LVREN): Low Voltage Reset Enable Bit

0 : Disable

1 : Enable

Bits 9~8 (LVR1~LVR0): Low Voltage Reset Voltage Select Bits

| LVR1 | LVR0 | Reset Voltage |
|------|------|---------------|
| 0 | 0 | 2.6V |
| 0 | 1 | 3.3 V |
| 1 | 0 | 3.9V |

Bit 7 (ENWDTB): Watchdog Timer Enable Bit

0 : Enable

1 : Disable

Bits 6~4 (FSMD, FMMD1~FMMD0): Oscillator Modes Selection Bits

| FSMD | FMMD1 | FMMD0 | Main clock | Sub-clock |
|------|-------|-------|----------------|----------------|
| 0 | 0 | 0 | RC type (ERIC) | RC type (ERIC) |
| 0 | 0 | 1 | Crystal type | RC type (ERIC) |
| 0 | 1 | 0 | PLL type | RC type (ERIC) |
| 0 | 1 | 1 | PLL type | RC type (ERIC) |
| 1 | 0 | 0 | RC type (ERIC) | Crystal type |
| 1 | 0 | 1 | Crystal type | Crystal type |
| 1 | 1 | 0 | PLL type | Crystal type |
| 1 | 1 | 1 | Crystal | None |

Bit 3 (HLP): Power Consumption Selection Bit

0 : Low power consumption, apply to working frequency at 4MHz or below 4MHz.

1 : High power consumption, apply to working frequency above 4MHz.

Bits 2~0 (PR2~PR0): Protect Bit

PR2~PR0 are protect bits, protect type are as follows:

| PR2 | PR1 | PR0 | Protect |
|-----|-----|-----|---------|
| 0 | 0 | 0 | Enable |
| 0 | 0 | 1 | Enable |
| 0 | 1 | 0 | Enable |
| 0 | 1 | 1 | Enable |
| 1 | 0 | 0 | Enable |
| 1 | 0 | 1 | Enable |
| 1 | 1 | 0 | Enable |
| 1 | 1 | 1 | Disable |

2. Code Option Register (Word 1)

| Word 1 | | | | | | | | | | | | |
|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|--------|
| Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| -- | -- | -- | -- | -- | -- | -- | HLFS | -- | -- | FCB0 | FCB1 | RESETB |

Bits 12~6 (Not used)

Bit 5 (HLFS): Main or Sub Oscillator Select Bit

0 : CPU is selected as sub-oscillator when a reset occurs

1 : CPU is selected as main-oscillator when a reset occurs

Bits 4~3 (Not used)

Bits 2~1 (FCB1~FCB0): Frequency Select Bit

| FCB1 | FCB0 | Operation Frequency |
|------|------|---------------------|
| 0 | 0 | 100k~1M |
| 0 | 1 | 1M~6M |
| 1 | 0 | 6M~12M |
| 1 | 1 | 12M~20M |

Bit 0 (RESETB): Reset Pin Enable Bit

0 : Enable, P81//RESET → RESET pin

1 : Disable, P81//RESET → P81

3. Customer ID Register (Word 2)

| Word 2 | | | | | | | | | | | | |
|-------------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Customer ID | | | | | | | | | | | | |

6.16 Instruction Set

Each instruction in the Instruction Set is a 13-bit word divided into an OP code and one or more operand. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2",). In this case, the execution takes two instruction cycles.

The following are executed within two instruction cycles; "LJMP", "LCALL", or conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") instructions which were tested to be true. Instructions written to the program counter are also executed within two instruction cycles.

In addition, the instruction set has the following features:

- (1) Every bit of any register can be set, cleared, or tested directly.
- (2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

Convention:

r = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

Bits 6 and 7 in R4 determine the selected register bank.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

| Binary Instruction | Hex | Mnemonic | Operation | Status Affected |
|--------------------|------|----------|--------------------------|-----------------|
| 0 0000 0000 0000 | 0000 | NOP | No Operation | None |
| 0 0000 0000 0001 | 0001 | DAA | Decimal Adjust A | C |
| 0 0000 0000 0011 | 0003 | SLEP | 0 → WDT, Stop oscillator | T, P |
| 0 0000 0000 0100 | 0004 | WDTC | 0 → WDT | T, P |
| 0 0000 0001 0000 | 0010 | ENI | Enable Interrupt | None |
| 0 0000 0001 0001 | 0011 | DISI | Disable Interrupt | None |
| 0 0000 0001 0010 | 0012 | RET | [Top of Stack] → PC | None |

| Binary Instruction | Hex | Mnemonic | Operation | Status Affected |
|--------------------|------|----------|--|-----------------|
| 0 0000 0001 0011 | 0013 | RETI | [Top of Stack] → PC, Enable Interrupt | None |
| 0 0000 01rr rrrr | 00rr | MOV R,A | A → R | None |
| 0 0000 1000 0000 | 0080 | CLRA | 0 → A | Z |
| 0 0000 11rr rrrr | 00rr | CLR R | 0 → R | Z |
| 0 0001 00rr rrrr | 01rr | SUB A,R | R-A → A | Z, C, DC |
| 0 0001 01rr rrrr | 01rr | SUB R,A | R-A → R | Z, C, DC |
| 0 0001 10rr rrrr | 01rr | DECA R | R-1 → A | Z |
| 0 0001 11rr rrrr | 01rr | DEC R | R-1 → R | Z |
| 0 0010 00rr rrrr | 02rr | OR A,R | A ∨ R → A | Z |
| 0 0010 01rr rrrr | 02rr | OR R,A | A ∨ R → R | Z |
| 0 0010 10rr rrrr | 02rr | AND A,R | A & R → A | Z |
| 0 0010 11rr rrrr | 02rr | AND R,A | A & R → R | Z |
| 0 0011 00rr rrrr | 03rr | XOR A,R | A ⊕ R → A | Z |
| 0 0011 01rr rrrr | 03rr | XOR R,A | A ⊕ R → R | Z |
| 0 0011 10rr rrrr | 03rr | ADD A,R | A + R → A | Z, C, DC |
| 0 0011 11rr rrrr | 03rr | ADD R,A | A + R → R | Z, C, DC |
| 0 0100 00rr rrrr | 04rr | MOV A,R | R → A | Z |
| 0 0100 01rr rrrr | 04rr | MOV R,R | R → R | Z |
| 0 0100 10rr rrrr | 04rr | COMA R | /R → A | Z |
| 0 0100 11rr rrrr | 04rr | COM R | /R → R | Z |
| 0 0101 00rr rrrr | 05rr | INCA R | R+1 → A | Z |
| 0 0101 01rr rrrr | 05rr | INC R | R+1 → R | Z |
| 0 0101 10rr rrrr | 05rr | DJZA R | R-1 → A, skip if zero | None |
| 0 0101 11rr rrrr | 05rr | DJZ R | R-1 → R, skip if zero | None |
| 0 0110 00rr rrrr | 06rr | RRCA R | R(n) → A(n-1), R(0) → C, C → A(7) | C |
| 0 0110 01rr rrrr | 06rr | RRC R | R(n) → R(n-1), R(0) → C, C → R(7) | C |
| 0 0110 10rr rrrr | 06rr | RLCA R | R(n) → A(n+1), R(7) → C, C → A(0) | C |
| 0 0110 11rr rrrr | 06rr | RLC R | R(n) → R(n+1), R(7) → C, C → R(0) | C |
| 0 0111 00rr rrrr | 07rr | SWAPA R | R(0-3) → A(4-7), R(4-7) → A(0-3) | None |
| 0 0111 01rr rrrr | 07rr | SWAP R | R(0-3) ↔ R(4-7) | None |
| 0 0111 10rr rrrr | 07rr | JZA R | R+1 → A, skip if zero | None |

| Binary Instruction | Hex | Mnemonic | Operation | Status Affected |
|------------------------------------|---------|----------|--|-------------------|
| 0 0111 11rr rrrr | 07rr | JZ R | $R+1 \rightarrow R$, skip if zero | None |
| 0 100b brrr rrrr | 0xxx | BC R,b | $0 \rightarrow R(b)$ | None |
| 0 101b brrr rrrr | 0xxx | BS R,b | $1 \rightarrow R(b)$ | None ¹ |
| 0 110b brrr rrrr | 0xxx | JBC R,b | if $R(b)=0$, skip | None |
| 0 111b brrr rrrr | 0xxx | JBS R,b | if $R(b)=1$, skip | None |
| 1 00kk kkkk kkkk | 1kkk | CALL k | $PC+1 \rightarrow [Stack]$, $(Page, k) \rightarrow PC$ | None |
| 1110 1010 kkkk k kkkk kkkk kkkk | 1EAKkkk | LCALL k | $PC+1 \rightarrow [Stack]$, $K \rightarrow PC$ | None |
| 1 01kk kkkk kkkk | 1kkk | JMP k | $(Page, k) \rightarrow PC$ | None |
| 1110 1011 kkkk k kkkk kkkk kkkk | 1EBkkkk | LJMP k | $K \rightarrow PC$ | None |
| 1 1000 kkkk kkkk | 18kk | MOV A,k | $k \rightarrow A$ | None |
| 1 1001 kkkk kkkk | 19kk | OR A,k | $A \vee k \rightarrow A$ | Z |
| 1 1010 kkkk kkkk | 1Akk | AND A,k | $A \& k \rightarrow A$ | Z |
| 1 1011 kkkk kkkk | 1Bkk | XOR A,k | $A \oplus k \rightarrow A$ | Z |
| 1 1100 kkkk kkkk | 1Ckk | RETL k | $k \rightarrow A$, $[Top\ of\ Stack] \rightarrow PC$ | None |
| 1 1101 kkkk kkkk | 1Dkk | SUB A,k | $k-A \rightarrow A$ | Z, C, DC |
| 1 1110 0kkk kkkk | 1E0K | BANK k | $k \rightarrow R5(2:0)$ | None |
| 1 1111 kkkk kkkk | 1Fkk | ADD A,k | $k+A \rightarrow A$ | Z, C, DC |

Note: ¹ This instruction cannot operate under an interrupt flag.

7 Absolute Maximum Ratings

| Items | Symbol | Condition | Rating | | Unit |
|----------------------------|-----------|----------------------------------|---------|---------|------|
| | | | Min. | Max. | |
| Supply voltage | V_{DD} | – | 2.3 | 5.5 | V |
| Input voltage | V_I | Port 7 ~ Port 9, Port A ~ Port C | GND-0.3 | VDD+0.3 | V |
| Output voltage | V_O | Port 7 ~ Port 9, Port A ~ Port C | GND-0.3 | VDD+0.3 | V |
| Operation temperature | T_{OPR} | – | -40 | 85 | °C |
| Storage temperature | T_{STG} | – | -65 | 150 | °C |
| Power dissipation | P_D | – | – | 500 | mW |
| Operating Frequency (2clk) | – | – | 32.768K | 16M | Hz |

8 DC Electrical Characteristics

8.1 DC Electrical Characteristics

■ $T_a = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5.0\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|--|------------------------------------|---------|--------|----------|---------------|
| Fc | Crystal: VDD to 5V | Two cycle with two clocks | 0.1 | | 16 | MHz |
| ERIC | ERIC: VDD to 5V | R: 51K Ω | F-20% | 2.2221 | F+20% | MHz |
| IIL | Input Leakage Current for input pins | $V_{IN} = V_{DD}, V_{SS}$ | -1 | 0 | 1 | μA |
| VIH1 | Input High Voltage (Schmitt Trigger) | Ports 7, 8, 9, A, B, C | 0.75VDD | – | VDD+0.3V | V |
| VIL1 | Input Low Voltage (Schmitt Trigger) | Ports 7, 8, 9, A, B, C | -0.3V | – | 0.25VDD | V |
| VIHT1 | Input High Threshold Voltage (Schmitt Trigger) | /RESET, INT | 0.75VDD | – | VDD+0.3V | V |
| VILT1 | Input Low Threshold Voltage (Schmitt Trigger) | /RESET, INT | -0.3V | – | 0.25VDD | V |
| VIHX1 | Clock Input High Voltage | OSCI in crystal mode | 0.75VDD | – | VDD+0.3V | V |
| VILX1 | Clock Input Low Voltage | OSCI in crystal mode | -0.3V | – | 0.25VDD | V |
| IOH1 | Output High Voltage (Port 9) LED enabled | $V_{OH} = V_{SS} + 2.1\text{V}$ | 8 | 10 | 15 | mA |
| IOH2 | Output High Voltage (Ports 7, 8, 9, A, B, C) | $V_{OH} = V_{DD} - 0.5\text{V}$ | 7 | 9 | 12 | mA |
| IOL1 | Output Low Voltage (Port 9) LED enabled | $V_{OL} = V_{DD} - 2.1$ | 8 | 10 | 15 | mA |
| IOL2 | Output Low Voltage (Ports 7, 8, 9, A, B, C) | $V_{OL} = V_{SS} + 0.5\text{V}$ | 16 | 18 | 21 | mA |
| IPH1 | Pull-high current | Pull-high active, input pin at VSS | -70 | -75 | -80 | μA |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|----------------------------------|---|------|------|------|---------------|
| ISB1 | Stop mode Power down current | All input and I/O pins at VDD, Output pin floating | – | 1.1 | – | μA |
| ISB2 | Stop mode Power down current | | | | | |
| ICC1 | Idle mode current | /RESET= 'High', CPU OFF, Sub-oscillator clock (32.768kHz) ON, Output pin floating, WDT disabled | – | 4.7 | – | μA |
| ICC2 | Idle mode current | /RESET= 'High', CPU OFF, Sub-oscillator clock (32.768kHz) ON, Output pin floating, WDT enabled, | – | 10.3 | – | μA |
| ICC3 | Idle mode current | /RESET= 'High', CPU OFF, Sub-oscillator clock (32.768kHz) ON, Output pin floating, WDT disabled, LCD enabled | – | 23.7 | – | μA |
| ICC4 | Green mode current | /RESET= 'High', CPU ON, used Sub-oscillator clock (32.768kHz), Output pin floating, WDT enabled, | – | 21.4 | – | μA |
| ICC5 | Normal mode | /RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled | – | 1.48 | – | mA |
| ICC6 | Normal mode | /RESET= 'High', Fosc=16MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled | – | 3.45 | – | mA |
| RLCD | LCD Voltage Dividing Resistor | Ta = 25 °C | – | 80 | – | K Ω |
| ILCD1 | All LCD lighting | VLCD=5V, exclude CPU core operation current (not panel) | – | 23.3 | – | μA |
| ILCD2 | All LCD lighting | VLCD=3V, exclude CPU core operation current (not panel) | – | 12.9 | – | μA |

* Typical values are based on characterization results at 25 °C

8.2 A/D Converter Characteristic

■ Vdd=2.5V to 5.5V, Vss=0V, Ta=-40 to 85 °C

| Symbol | | Parameter | Condition | Min | Typ | Max | Unit |
|--------|-------|--|--|------|------|-------|------|
| VAREF | | Analog reference voltage | VAREF - VASS ≥ 2.5V | 2.5 | – | Vdd | V |
| VASS | | | | Vss | – | Vss | V |
| VAI | | Analog input voltage | – | VASS | – | VAREF | V |
| IAI1 | Ivdd | Analog supply current | Vdd=VAREF=5.0V, VASS = 0.0V (V reference from Vdd) | 750 | 850 | 1000 | μA |
| | Ivref | | | -10 | 0 | +10 | μA |
| IAI2 | Ivdd | Analog supply current | Vdd=VAREF=5.0V, VASS = 0.0V (V reference from VREF) | 500 | 600 | 820 | μA |
| | Ivref | | | 200 | 250 | 300 | μA |
| RN | | Resolution | Vdd=VAREF=5.0V, VASS = 0.0V | 11 | 12 | – | Bits |
| LN | | Linearity error | Vdd = 2.5 to 5.5V Ta=25°C | 0 | ±4 | ±8 | LSB |
| DNL | | Differential non-linear error | Vdd = 2.5 to 5.5V Ta=25°C | 0 | ±0.5 | ±0.8 | LSB |
| FSE | | Full scale error | Vdd=VAREF=5.0V, VASS = 0.0V | ±0 | ±4 | ±8 | LSB |
| OE | | Offset error | Vdd=VAREF=5.0V, VASS = 0.0V | ±0 | ±2 | ±4 | LSB |
| ZAI | | Recommended impedance of analog voltage source | – | 0 | 8 | 10 | KΩ |
| ADIV | | A/D input voltage range | VDD =VAREF=5.0V, VASS = 0.0V | 0 | – | VAREF | V |
| ADOV | | A/D output voltage swing | VDD =VAREF=5.0V, VASS = 0.0V, RL=10KΩ | 0 | 0.2 | 0.3 | V |
| | | | | 4.7 | 4.8 | 5 | |
| TAD | | A/D clock period | Vdd=VAREF=5.0V, VASS = 0.0V | 4 | – | – | μs |
| TCN | | A/D conversion time | Vdd=VAREF=5.0V, VASS = 0.0V | 14 | – | 14 | TAD |
| PSR | | Power Supply Rejection | Vdd=5.0V±0.5V | ±0 | – | ±2 | LSB |

8.3 Phase Lock Loop Characteristic

8.3.1 PLL DC Electrical Characteristic

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|------------------------|-----------|-----|-----|-----|------|
| VD | Digital Supply Voltage | – | 2.3 | – | 5.5 | V |

8.3.2 AC Electrical Characteristic

| Parameter | Condition | | | Min | Typ | Max | Unit |
|---------------------|-----------------|------|------|-----|--------|-----|------|
| Input Clock | – | | | – | 32.768 | – | kHz |
| Output Clock | CLK2 | CLK1 | CLK0 | – | – | – | – |
| | 0 | 0 | 0 | – | 3.997 | – | MHz |
| | 0 | 0 | 1 | – | 1.998 | – | MHz |
| | 0 | 1 | 0 | – | 0.999 | – | MHz |
| | 0 | 1 | 1 | – | 499.7 | – | KHz |
| | 1 | 0 | 0 | – | 7.995 | – | MHz |
| | 1 | 0 | 1 | – | 11.99 | – | MHz |
| | 1 | 1 | X | – | 15.99 | – | MHz |
| Current Consumption | Normal | | | – | – | 500 | μA |
| | Power Down Mode | | | – | – | 1 | μA |
| Lock Up Time | – | | | – | – | 200 | μs |
| Frequency Accuracy | – | | | -30 | – | +30 | ppm |

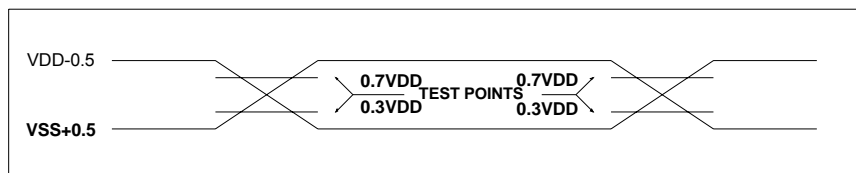
9 AC Electrical Characteristics

■ (Ta = -40 °C ~ 85 °C, VDD = 5V ± 5%, GND = 0V)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------------------------------|---------------|------|------|------|------|
| Dclk | Input CLK duty cycle | – | 45 | 50 | 55 | % |
| Tins | Instruction cycle time (CLKS="0") | Crystal type | 100 | – | DC | ns |
| | | RC type | 500 | – | DC | ns |
| Tdrh | Device reset hold time | Ta = 25 °C | 11.3 | 16.2 | 21.6 | ms |
| Trst | /RESET pulse width | Ta = 25 °C | 2000 | – | – | ns |
| Twdt | Watchdog timer period | Ta = 25 °C | 11.3 | 16.2 | 21.6 | ms |
| Tset | Input pin setup time | – | – | 0 | – | ns |
| Thold | Input pin hold time | – | – | 20 | – | ns |
| Tdelay | Output pin delay time | Cload = 20pF | – | 50 | – | ns |
| Tiod | I/O delay for EMI enable | Cload = 150pF | 4 | 5 | 6 | ns |

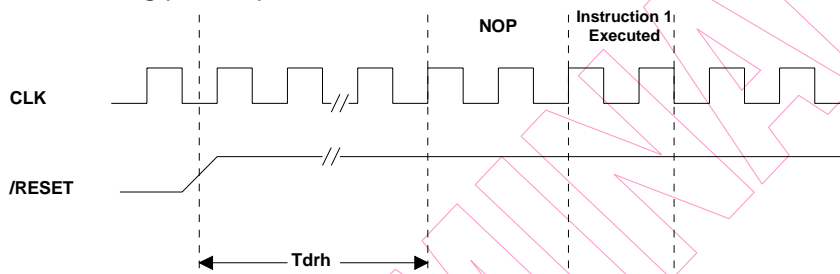
10 Timing Diagrams

AC Test Input/Output Waveform

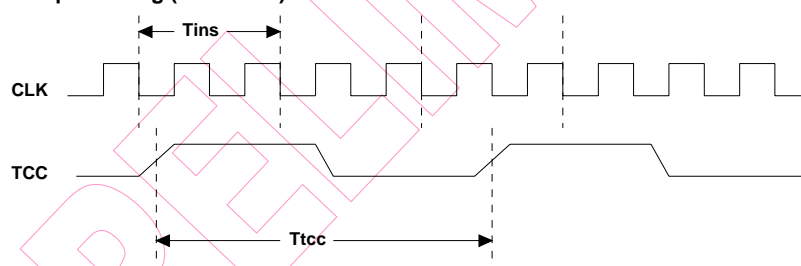


AC Testing : Input is driven at 2.4V for logic "1", and 0.4V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



* n = 0, 2, 4, 6

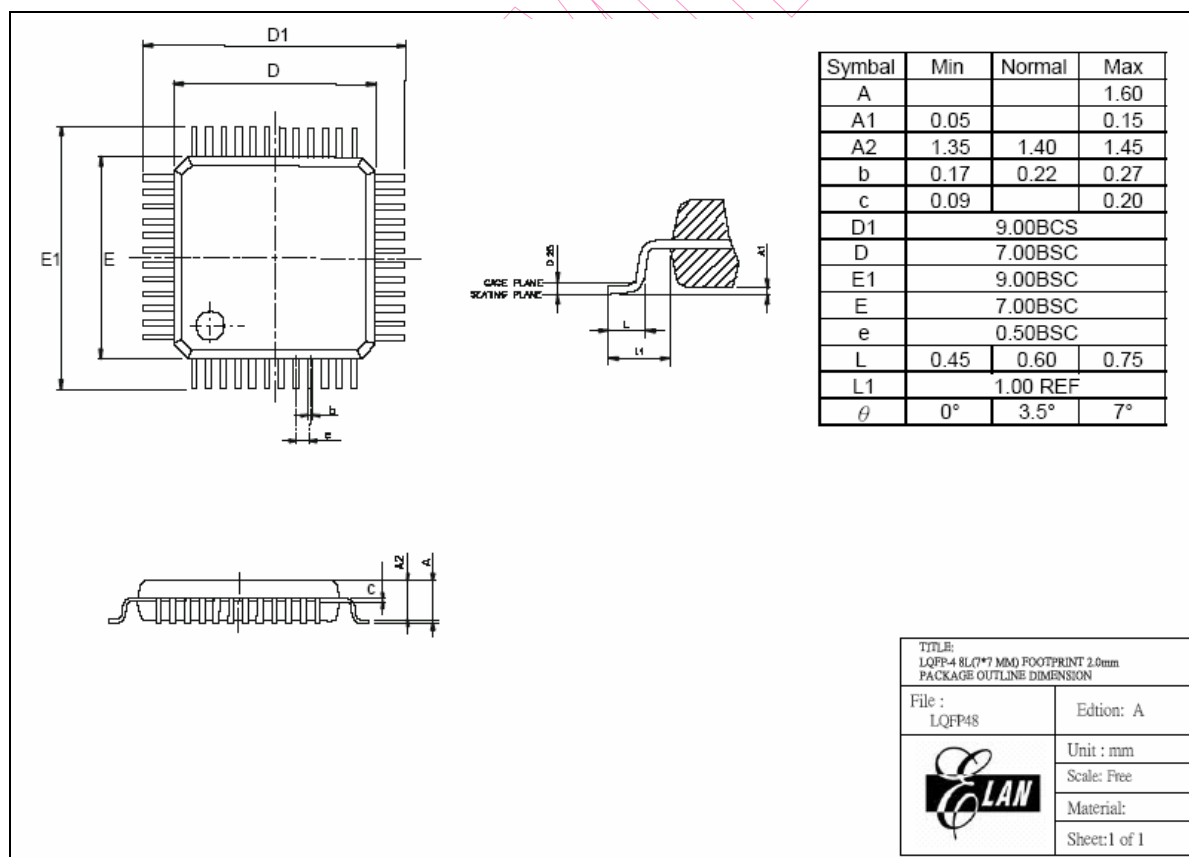
APPENDIX

A Package Type

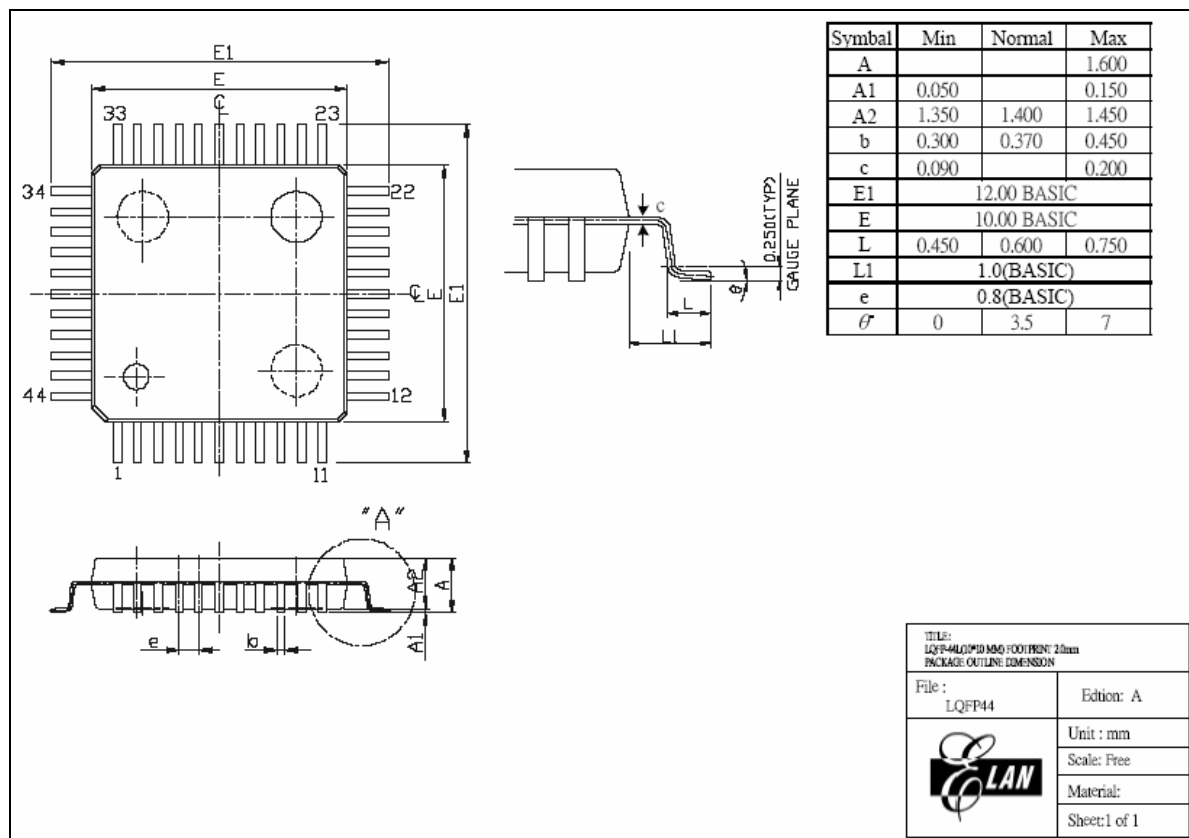
| OTP MCU | Package Type | Pin Count | Package Size |
|---------------|--------------|-----------|---------------|
| EM78P510NQ | LQFP | 48 | 7 mm x 7 mm |
| EM78P510NAQ | LQFP | 44 | 10 mm x 10 mm |
| EM78P510NBQ | QFP | 44 | 10 mm x 10 mm |
| EM78P510NP | DIP | 42 | 600 mil |
| EM78P510NK/AK | SDIP | 32 | 400 mil |
| EM78P510NM/AM | SOP | 32 | 450 mil |

B Package Information

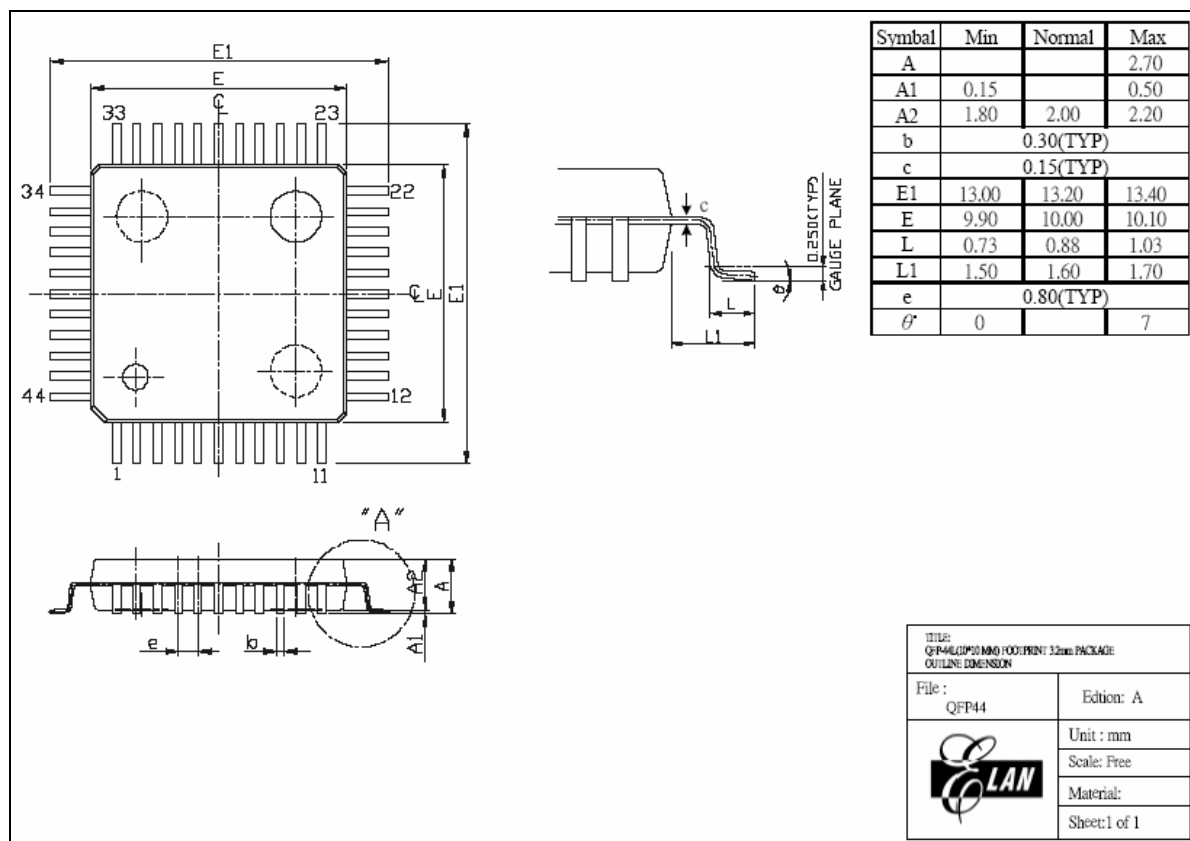
B.1 48-Lead Low Profile Quad Flat Package (LQFP)



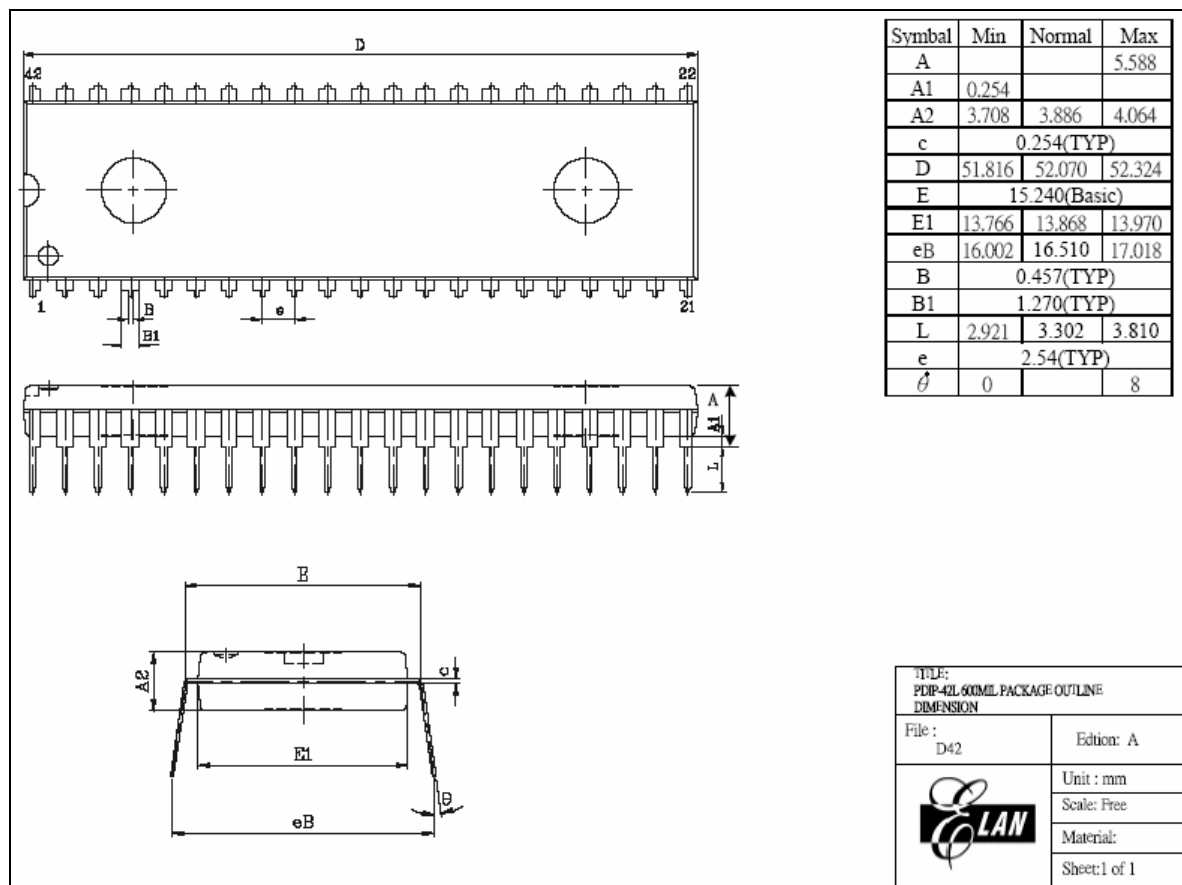
B.2 44-Lead Low Profile Quad Flat Package (LQFP)



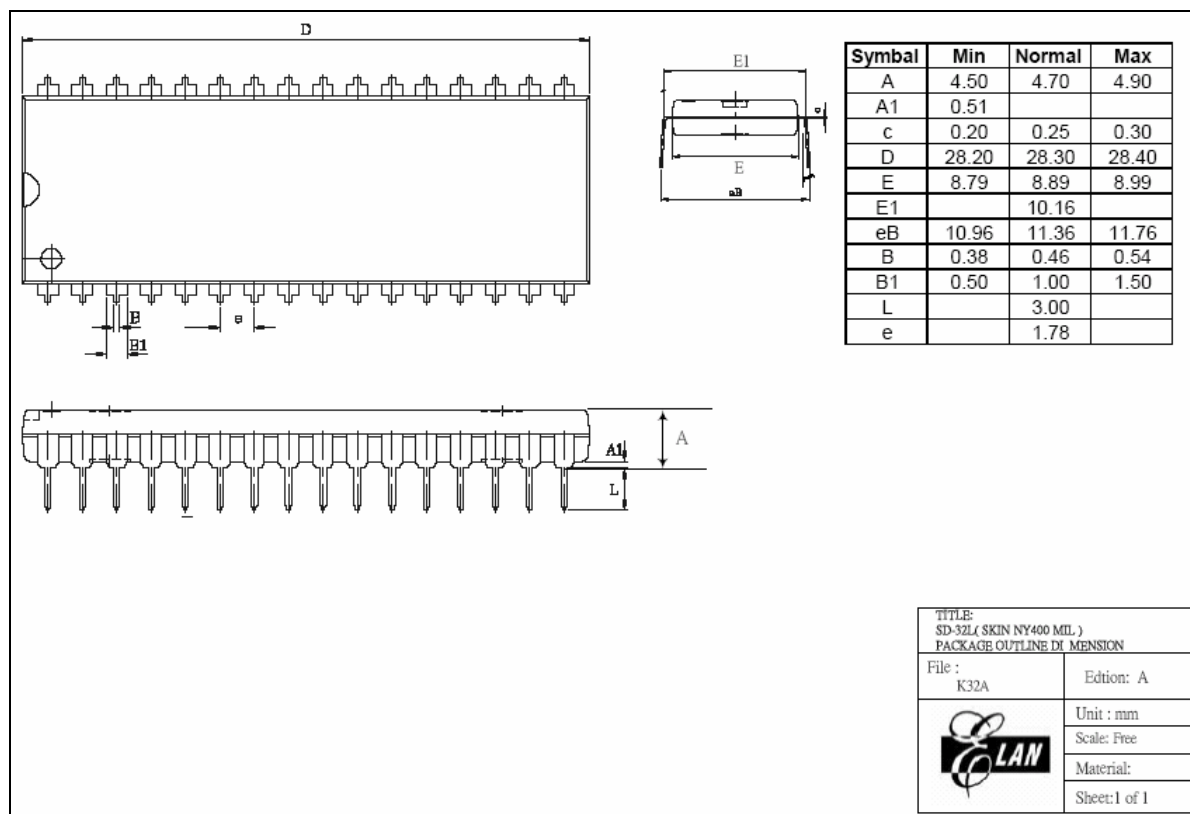
B.3 44-Lead Quad Flat Package (QFP)



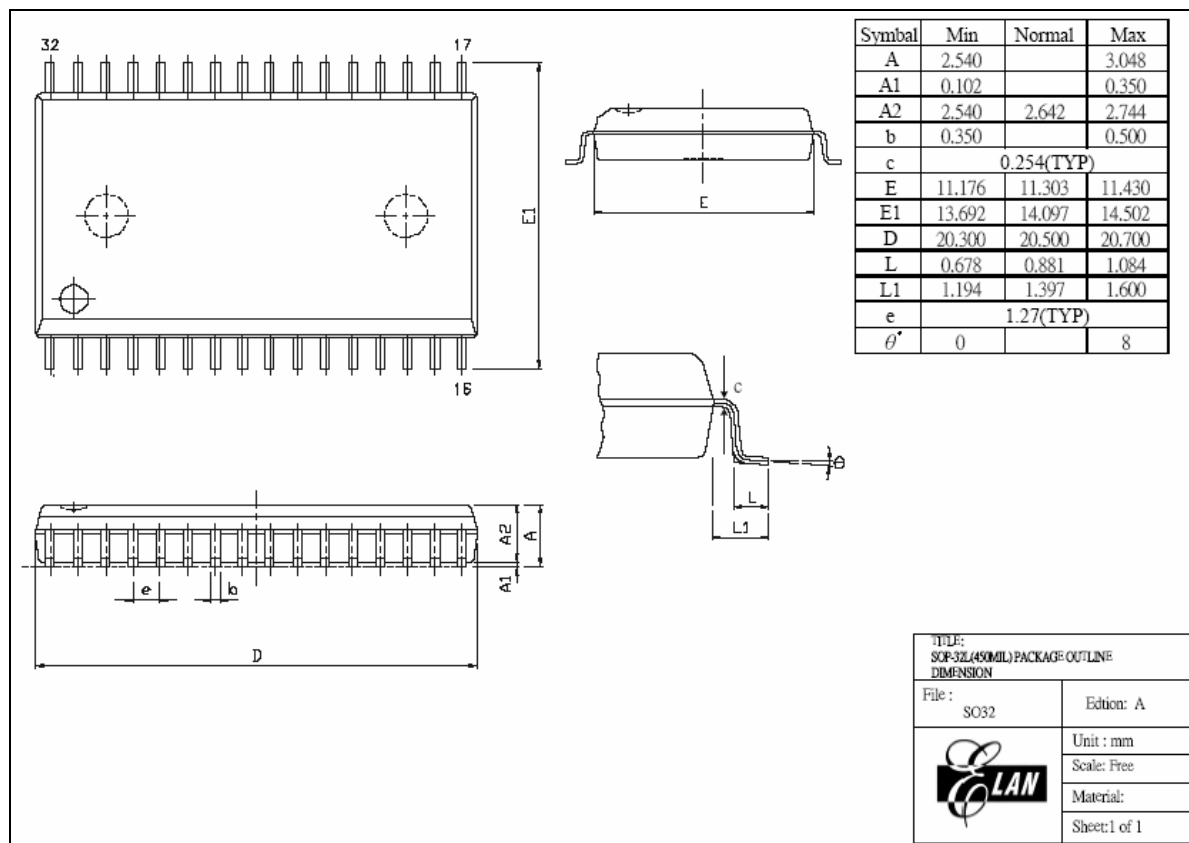
B.4 42-Lead Dual Inline Package (DIP)



B.5 32-Lead Shrink Dual Inline Package (SDIP)



B.6 32-Lead Small Outline Package (SOP)



C EM78P510N Program Pin List

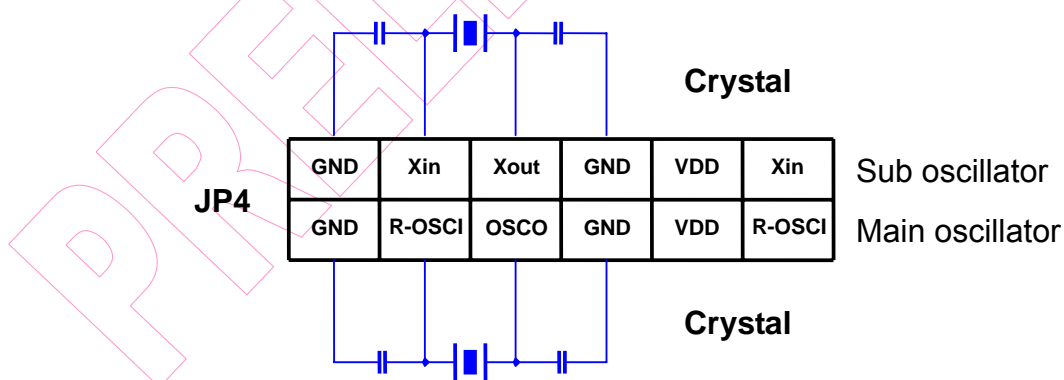
DWTR is used to program the EM78P510N IC's. The connector of DWTR is selected by CON3 (EM78P447). The software is selected by EM78P510.

| Program Pin Name | IC Pin Name | LQFP-48 Pin Number | L/QFP-44 Pin Number | DIP-42 Pin Number | SDIP/SOP-32 Pin Number |
|------------------|-------------|-----------------------|------------------------|----------------------|---------------------------|
| Pin #31 | P75 | 2 | 2 | 8 | 29 |
| Pin #30 | P76 | 3 | 3 | 9 | 30 |
| Pin #28 | P77 | 4 | 4 | 10 | 31 |
| Pin #8 | VDD | 5 | 5 | 11 | 32 |
| Pin #10 | VSS | 6 | 6 | 12 | 1 |
| Pin #34 | TEST | 9 | 9 | 15 | 4 |
| Pin #29 | PC2 | 10 | 10 | 16 | 5 |
| Pin #32 | PC3 | 11 | 11 | 17 | 6 |

D ICE 510 Oscillator circuit (JP4)

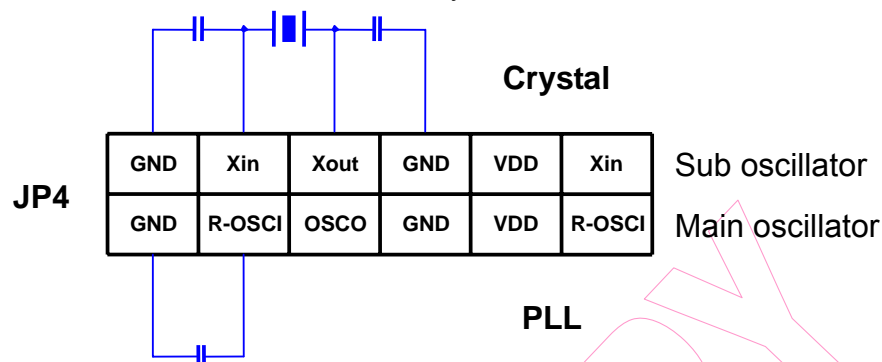
D.1 Mode 1

Main oscillator: Crystal mode, Sub oscillator: Crystal mode



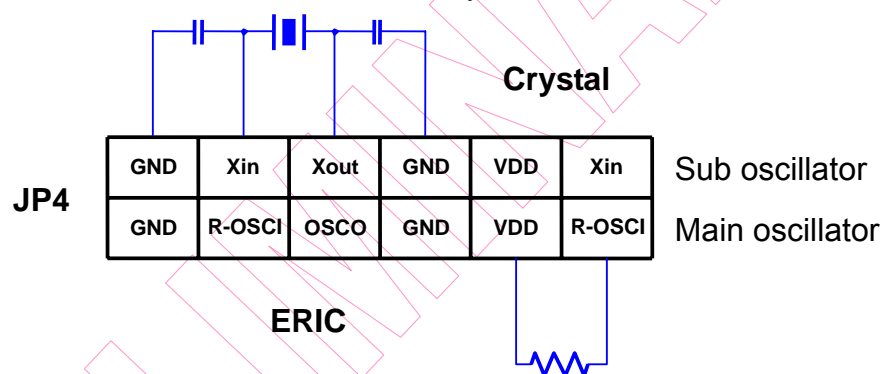
D.2 Mode2

Main oscillator: PLL mode, Sub oscillator: Crystal mode



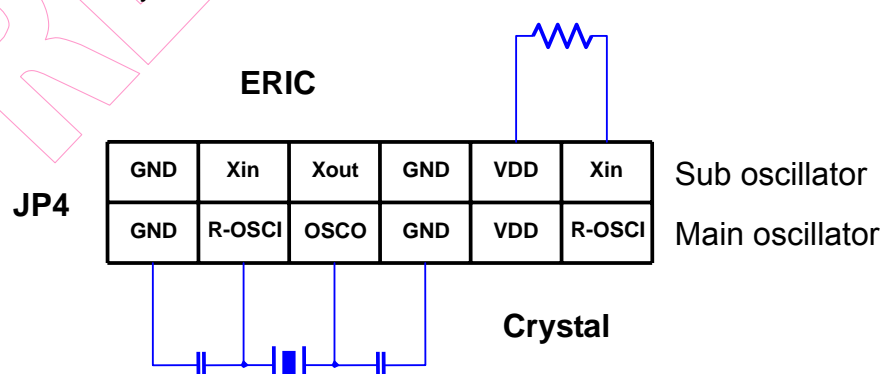
D.3 Mode3

Main oscillator: ERIC mode, Sub oscillator: Crystal mode



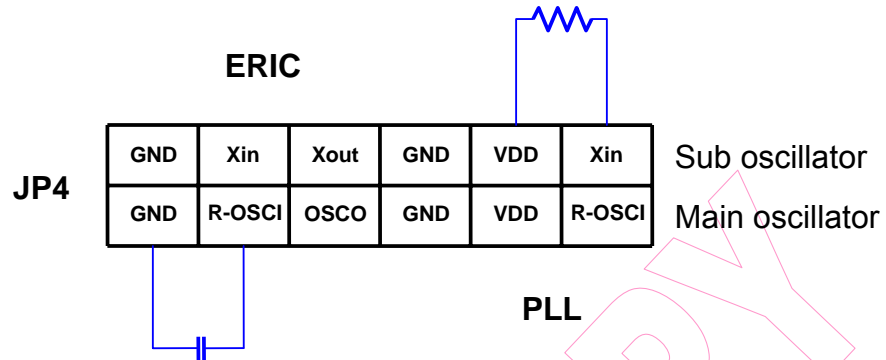
D.4 Mode4

Main oscillator: Crystal mode, Sub oscillator: ERIC mode



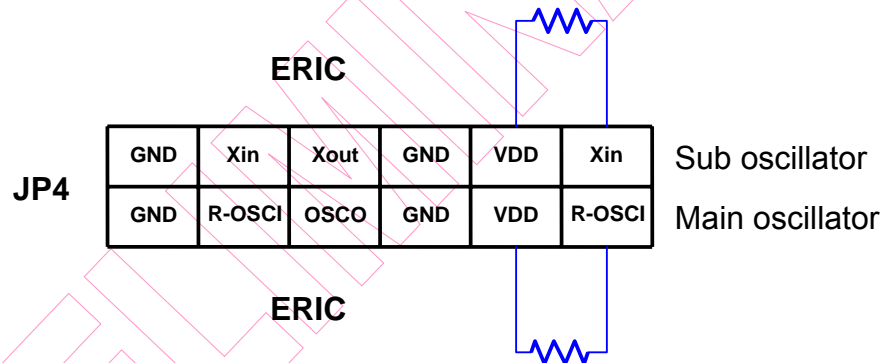
D.5 Mode5

Main oscillator: PLL mode, Sub oscillator: RC mode



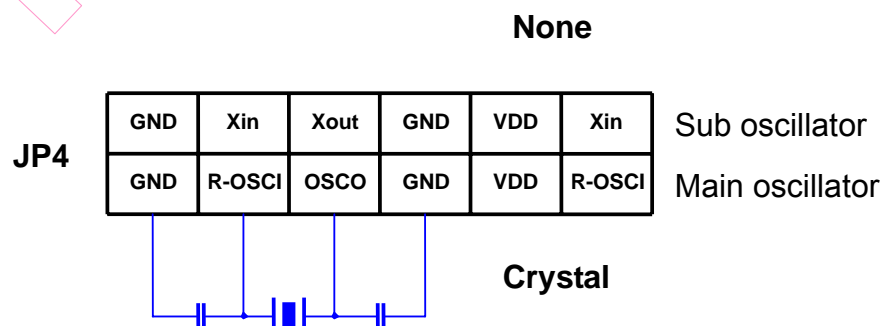
D.6 Mode6

Main oscillator: RC mode, Sub oscillator: RC mode



D.7 Mode7

Main oscillator: Crystal mode, Sub oscillator: None



E ICE 510 Output Pin Assignment (JP 3)

