QST108

Capacitive touch sensor device
8 keys with individual key state outputs or I2C interface

Not For New Design

Features

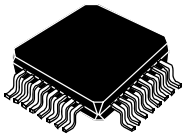
- Patented charge-transfer design
- Up to 8 independent QTouch™ keys supported
- Individual key state outputs or I^2C interface
- Fully “debounced” results
- Patented AKS™ Adjacent Key Suppression
- Self-calibration and auto drift compensation
- Spread-spectrum bursts to reduce EMI
- Up to 5 general-purpose outputs
- ECOPACK® (RoHS compliant) package

Applications

This device specifically targets human interfaces and front panels for a wide range of applications such as PC peripherals, home entertainment systems, gaming devices, lighting and appliance controls, remote controls, etc.

QST devices are designed to replace mechanical switching/control devices and the reduced number of moving parts in the end product provides the following advantages:

- Lower customer service costs
- Reduced manufacturing costs
- Increased product lifetime



LQFP32 (7x7 mm)

Description

The QST108 is the ideal solution for the design of capacitive touch sensing user interfaces.

Touch-sensitive controls are increasingly replacing electromechanical switches in home appliances, consumer and mobile electronics, and in computers and peripherals. Capacitive touch controls allow designers to create stylish, functional, and economical designs which are highly valued by consumers, often at lower cost than the electromechanical solutions they replace.

The QST108 QTouch™ sensor IC is a pure digital solution based on Quantum's patented charge-transfer (QProx™) capacitive technology.

QTouch™ and QProx™ are trademarks of the Quantum Research Group.

Table 1. Device summary

Feature	Order codes
	QST108KT6
Operating supply voltage	2.4 to 5.5 V
Supported interfaces	Individual key state outputs or I^2C Interface
Operating temperature	-40° to +85° C
Package	LQFP32 (7x7 mm)

Contents

1 Device overview

The QST108 capacitive touch sensor IC is a pure digital solution based on Quantum's patented charge-transfer (QProx™) capacitive technology.

This technology allows users to create simple touch panel sensing electrode interfaces for conventional or flexible printed circuit boards (PCB/FPCB). Sensing electrodes are part of the PCB layout (copper pattern or printed conductive ink) and may be used in various shapes (circle, rectangular, etc.).

By implementing the QProx™ charge-transfer algorithm, the QST108 detects finger presence (human touch) near electrodes behind a dielectric (glass, plastic, wood, etc.). Only one external sampling capacitor by channel is used in the measuring circuitry to control the detection.

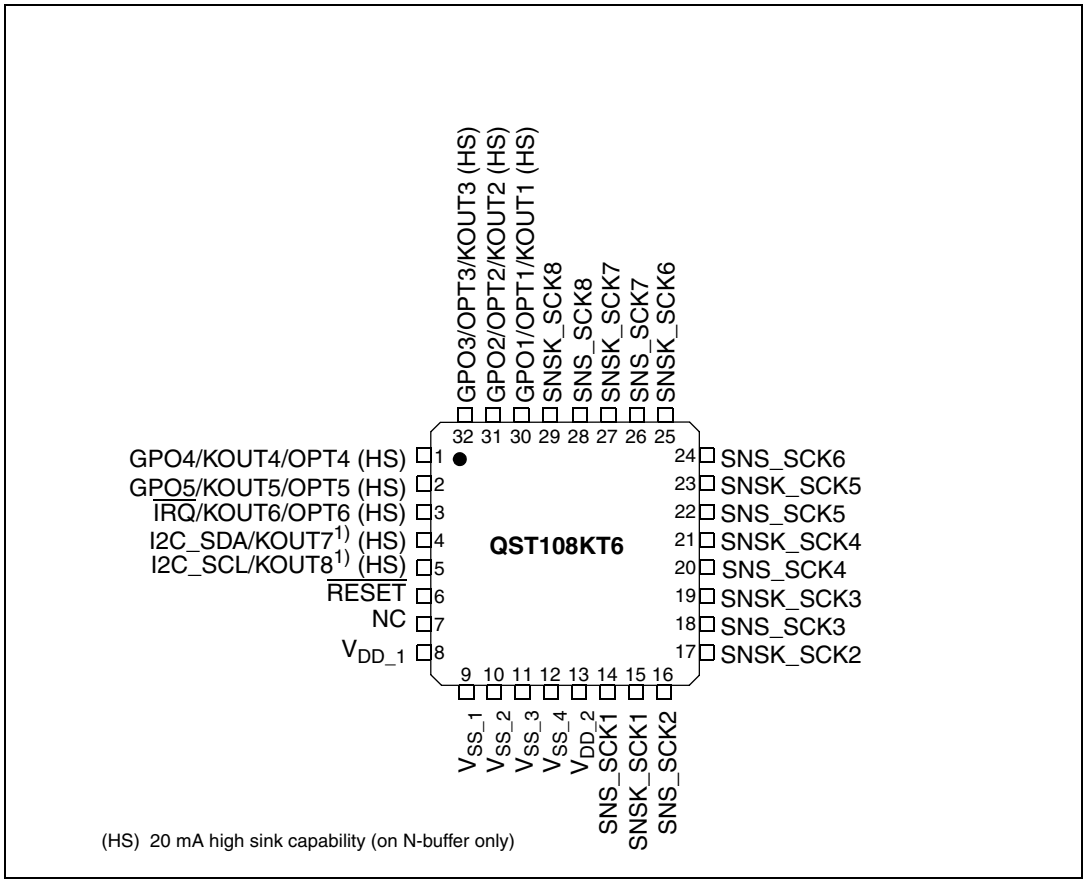
QST technology also incorporates advanced processing techniques such as drift compensation, auto-calibration, noise filtering, and Quantum's patented Adjacent Key Suppression™ (AKS™) to ensure maximum usability and control integrity.

In order to meet environmental requirements, ST offers this device in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

2 Pin description

Figure 1. 32-pin package pinout



1. An external pull-up is required on these pins.

Table 2. Device pin description

Pin	Pin name	Type (1)	Stand-alone mode function	I²C mode function	If unused
1	GPO4/OPT4/KOUT4 (2)	PP (HS)	Key 4 output / BCD output 4 and MOD_0 option resistor	General purpose output 4 and I²C address bit 2 option resistor	Option resistor
2	GPO5/OPT5/KOUT5 (2)	PP (HS)	Key 5 output and MOD_1 option resistor	General purpose output 5	Open or option resistor
3	OPT6/KOUT6/$\overline{IRQ}$ (2)	PP/OD (HS)	Key 6 output and OM_0 option resistor	Interrupt line (active low)	Open or option resistor
4	KOUT7/I2C_SDA(3)	TOD (HS)	Key 7 output	I²C serial data	Open
5	KOUT8/I2C_SCL(3)	TOD (HS)	Key 8 output	I²C serial clock	Open

Table 2. Device pin description (continued)

Pin	Pin name	Type (1)	Stand-alone mode function	I^2C mode function	If unused
6	$\overline{RESET}$	BD	Reset (active low)		10nF capacitor to ground
7	NC		Not connected		
8	V_{DD_1}	S	Supply voltage		
9	V_{SS_1}	S	Ground voltage		
10	V_{SS_2}	S	Ground voltage		
11	V_{SS_3}	S	Ground voltage		
12	V_{SS_4}	S	Ground voltage		
13	V_{DD_2}	S	Supply voltage		
14	SNS_SCK1	SNS	Key 1 sense pin to Cs		Open
15	SNSK_SCK1	SNS	Key 1 sense pin to Cs/Rs		Open
16	SNS_SCK2	SNS	Key 2 sense pin to Cs		Open
17	SNSK_SCK2	SNS	Key 2 sense pin to Cs/Rs		Open
18	SNS_SCK3	SNS	Key 3 sense pin to Cs		Open
19	SNSK_SCK3	SNS	Key 3 sense pin to Cs/Rs		Open
20	SNS_SCK4	SNS	Key 4 sense pin to Cs		Open
21	SNSK_SCK4	SNS	Key 4 sense pin to Cs/Rs		Open
22	SNS_SCK5	SNS	Key 5 sense pin to Cs		Open
23	SNSK_SCK5	SNS	Key 5 sense pin to Cs/Rs		Open
24	SNS_SCK6	SNS	Key 6 sense pin to Cs		Open
25	SNSK_SCK6	SNS	Key 6 sense pin to Cs/Rs		Open
26	SNS_SCK7	SNS	Key 7 sense pin to Cs		Open
27	SNSK_SCK7	SNS	Key 7 sense pin to Cs/Rs		Open
28	SNS_SCK8	SNS	Key 8 sense pin to Cs		Open
29	SNSK_SCK8	SNS	Key 8 sense pin to Cs/Rs		Open
30	GPO1/OPT1/KOUT1 (2)	PP (HS)	Key 1 output / BCD output 1 and MODE option resistor	General purpose output 1 and MODE option resistor	Option resistor
31	GPO2/OPT2/KOUT2 (2)	PP (HS)	Key 2 output / BCD output 2 and AKS option resistor	General purpose output 2 and I^2C address bit 0 option resistor	Option resistor
32	GPO3/OPT3/KOUT3 (2)	PP (HS)	Key 3 output / BCD output 3 and LP option resistor	General purpose output 3 and I^2C address bit 1 option resistor	Option resistor

1. S: supply pin, BD: bidirectional pin, SNS: capacitive sensing pin, PP: Output push-pull, OD: Output open-drain, TOD: Output true open-drain and HS: 20mA high sink capability (on N-buffer only)
2. During the reset phase, these pins are floating and their state depends on the option resistor.
3. An external pull-up is required on these pins.

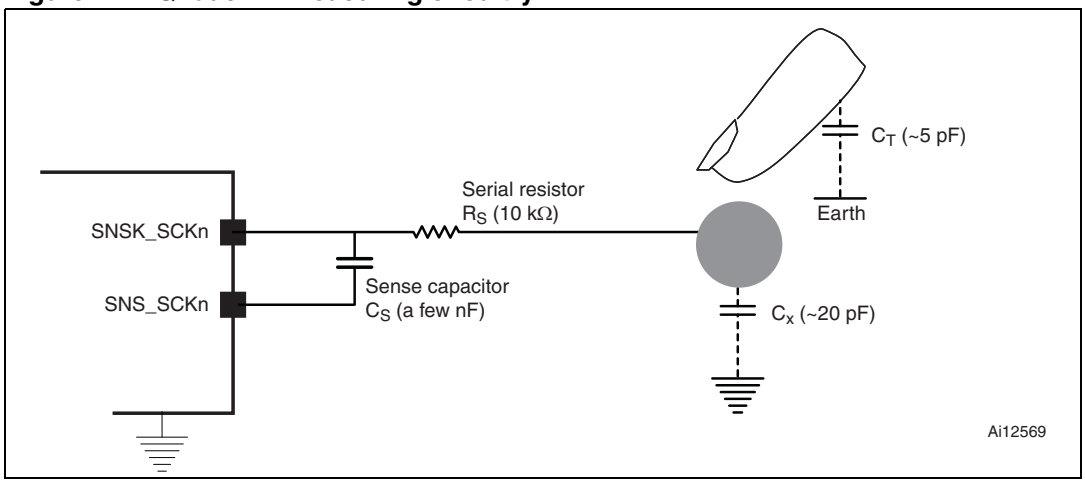
3 QST touch sensing technology

3.1 Functional description

QST devices employ bursts of charge-transfer cycles to acquire signals. Burst mode permits low power operation, dramatically reduces RF emissions, lowers susceptibility to RF fields, and yet permits excellent speed. Signals are processed using algorithms pioneered by Quantum which are specifically designed to provide reliable, trouble-free operation over the life of the product.

The QST switches and charge measurement hardware functions are all internal to the device. An external C_S capacitor accumulates the charge from sense-plate C_X, which is then measured. Larger values of C_X cause the charge transferred into C_S to rise more rapidly, reducing available resolution. As a minimum resolution is required for proper operation, this can result in dramatically reduced gain. Larger values of C_S reduce the rise of differential voltage across it, increasing available resolution by permitting longer QST bursts. The value of C_S can thus be increased to allow larger values of C_X to be tolerated. The device is responsive to both C_X and C_S, and changes in either can result in substantial changes in sensor gain.

Figure 2. QTouch™ measuring circuitry



3.2 Spread-spectrum operation

The bursts operate over a spread of frequencies, so that external fields will have minimal effect on key operation and emissions are very weak. Spread-spectrum operation works with the Detection Integrator mechanism (DI) to dramatically reduce the probability of false detection due to noise.

3.3 Faulty and unused keys

Any sensing channel that does not have its sense capacitor (C_S) fitted is assumed to be either faulty or unused. This channel takes no further part in operation unless a Master-commanded recalibration operation shows it to have an in-range burst count again. Faulty, unused or disabled keys are still bursted but not processed to avoid modifying the sensitivity of active keys.

This is important for sensing channels that have an open or short circuit fault across C_S. Such channels would otherwise cause very long acquire bursts, and in consequence would slow the operation of the entire QST device.

To optimize touch response time and device power consumption, if some keys are not used, we recommend to try suppressing the ones which belong to the same burst. Bursts which do not have any keys implemented will then not be processed.

3.4 Detection threshold levels

The key capacitance change induced by the presence of a finger is sensed by the variation in the number of charge transfer pulses to load the capacitor. The difference in the pulse count number is compared to a threshold in order to detect the key as pressed or not.

Two different thresholds, one for detection and one for the end of detection, create an hysteresis in order to prevent erratic behavior.

The default threshold levels and hysteresis values are described in *Section 6.6: Capacitive sensing characteristics on page 35*.

3.5 Detection integrator filter

The Detection Integrator (DI) filter mechanism works together with spread spectrum operation to dramatically reduce the effects of noise on key states. The DI mechanism requires a specified number of measurements that qualify as detections (and these must occur in a row) or the detection will not be reported.

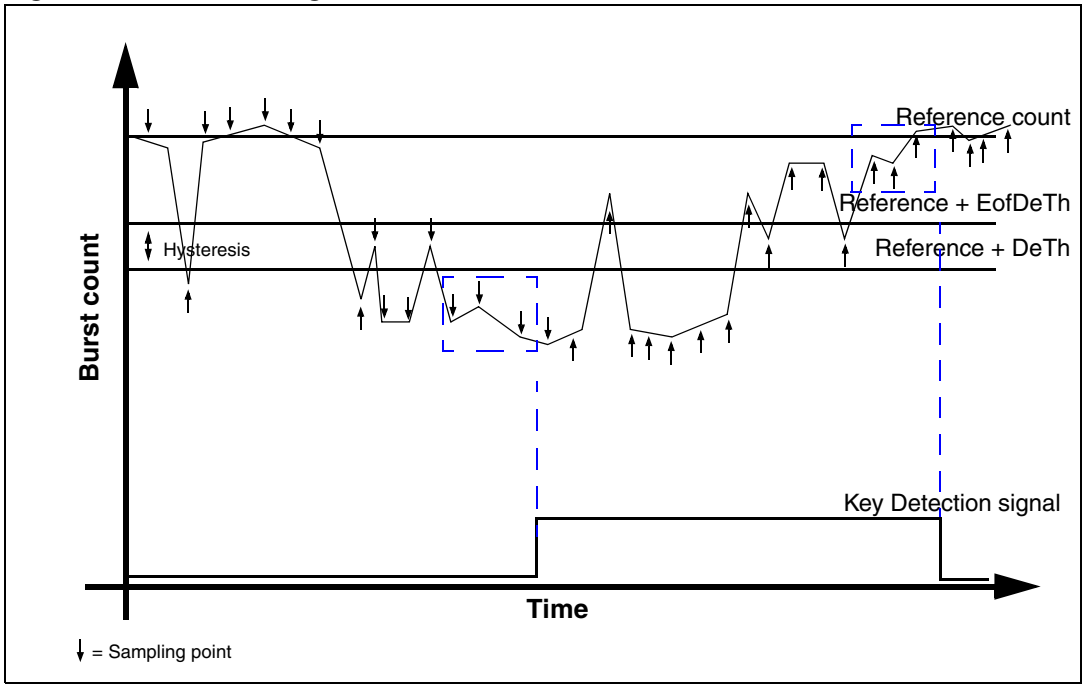
In a similar manner, the end of a touch (loss of signal) also has to be confirmed over several measurements. It is called the End of Detection Integrator (EDI).

This process acts as a type of “debounce” mechanism against noise.

The default DI and EDI values for confirming start of touch and end of touch are described in *Section 6.6: Capacitive sensing characteristics on page 35*.

Figure 3 shows an example of detection with DI=2 and EDI=2 meaning 3 consecutive samples are necessary to trigger the key detection or end of detection

Figure 3. Detection signals



3.6 Self-calibration

On power-up, all keys are self-calibrated to provide reliable operation under almost any conditions. The calibration phase is used to compute a reference value per key which is then used by the process determining if a key is touched or not. The reference is an average of 8 single acquisitions. As a result, the calibration time of the system can be simply calculated using the following formula: t_{CAL} = 8 * Burst_Period. The methodology used to measure the burst period is described in application note AN2547. For a maximum calibration duration (t_{CAL}), please refer to *Section 6.6: Capacitive sensing characteristics on page 35*.

3.7 Fast positive recalibration

The device autorecalibrates a key when its signal reflects a decrease in capacitance higher than a fixed threshold (PosRecalTh) for a defined number of acquisitions (PosRecalI).

3.8 Forced key recalibration

A recalibration of the device may be issued at any time by sending to the QST device the appropriate I^2C command or by tying the $\overline{RESET}$ pin to ground.

It is possible to recalibrate independently any individual key using an I^2C command.

3.9 Max On-Duration

The device can time out and automatically recalibrate each key independently after a fixed duration of continuous touch detection. This prevents the keys from becoming ‘stuck on’ due to foreign objects or other sudden influences. This is known as the Max On-Duration feature.

After recalibration, the key will continue to operate normally, even if partially or fully obstructed. Max On-Duration works independently per channel: a timeout on one channel has no effect on another channel.

Infinite timeout is useful in applications where a prolonged detection can occur and where the output must reflect the detection no matter how long. In infinite timeout mode, the designer should take care to ensure that drift in C_S, C_X, and V_{DD} do not cause the device to remain “stuck on” inadvertently even when the touching object is removed from the sense field. Timeout durations are not accurate and can vary substantially depending on V_{DD} and temperature values, and should not be relied upon for critical functions.

3.10 Drift compensation

Signal drift can occur because of changes in C_X, C_S, and V_{DD} over time. Depending on the C_S type and quality, the signal may vary substantially with temperature and veiling. If keys are subject to extremes of temperature or humidity, the signal can also drift. It is crucial that drift be compensated, otherwise false detections, non detections, and sensitivity shifts will follow.

Drift compensation slowly corrects the reference level of each key while no detection is in effect. The rate of reference adjustment must be performed slowly or else legitimate detections can also be ignored. The device compensates drift on each channel independently using a maximum compensation rate to the reference level.

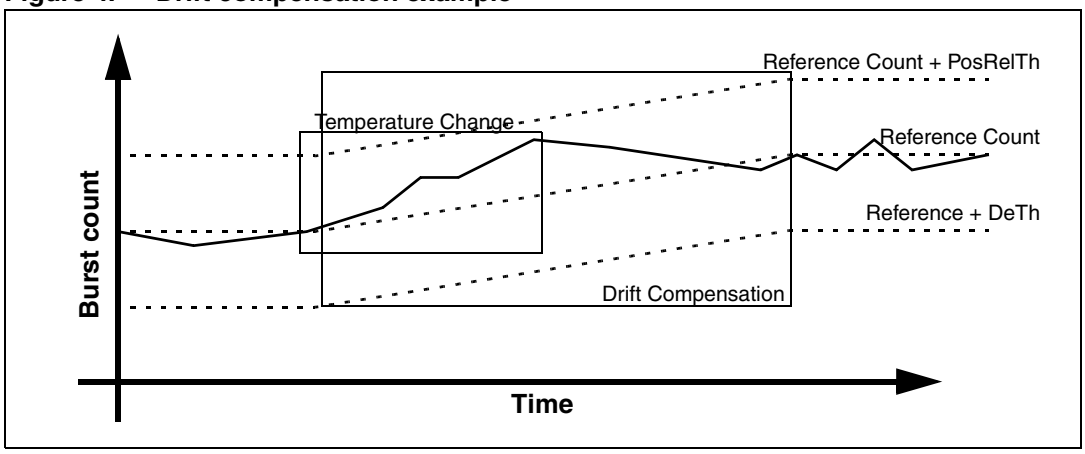
Once a touch is sensed, the drift compensation mechanism ceases since the signal is legitimately high, and therefore should not cause the reference level to change.

The signal drift compensation is “asymmetric”: the reference level compensates drift in one direction faster than it does in the other. Specifically, it compensates faster for increasing signals than for decreasing signals. Decreasing signals should not be compensated for quickly, since an approaching finger could be compensated for partially or entirely while approaching the sense electrode. However, an obstruction over the sense pad, for which the sensor has already made full allowance, could suddenly be removed leaving the sensor with an artificially elevated reference level and thus become insensitive to touch. In this latter case, the sensor will compensate for the object's removal very quickly, usually in only a few seconds.

Caution: When only one key is enabled or if keys are very close together, the common drift compensation must be disabled or its rate must be reduced to ensure correct device operation.

Figure 4 illustrates an example of the drift compensation algorithm following a temperature change.

Figure 4. Drift compensation example



3.11 Adjacent key suppression (AKS™)

Adjacent key suppression (AKS™) is a Quantum-patented feature which prevents multiple keys from responding to a single touch. This can happen with closely spaced keys, or a scroll wheel that has buttons very near it.

The QST108 supports two AKS modes:

- Locking AKS

  Once a key is considered as “touched”, all other keys are locked in an untouched state. To unlock these keys, the touched key must return to an untouched state. Then, the key having the lowest key ID number is declared as the “touched” one.

- Unlocking AKS

  On each acquisition, the signal strengths from each key are compared and the key with the highest signal level is declared as the “touched” one.

In I^2C mode, up to 8 AKS groups can be specified.

Note: All keys belonging to the same AKS group must have the same AKS mode.

4 Device operating modes

4.1 Reset and power-up

At power-up, the device configures itself according to the pull-up or pull-down option resistors present on pins OPT1 to OPT6. The device start-up and configuration may take up to t_{Setup}.

When the power is established, it is possible to force a new device configuration by applying a negative pulse on the $\overline{\text{RESET}}$ pin.

The $\overline{\text{RESET}}$ pin is a bidirectional pin with an internal pull-up. The line is forced low when the device resets itself (through an I²C command, for example).

A 10nF capacitor is recommended on the $\overline{\text{RESET}}$ pin to ensure reliable start-up and noise immunity.

4.2 Burst operation

The device operates in “Burst” mode. Each key touch is acquired using a burst of charge-transfer sensing pulses whose count varies depending on the value of the sense capacitor C_S and the load capacitance C_X. Key touches are acquired using two successive bursts of pulses:

- Burst A: Keys 1, 2, 3, and 4
- Burst B: Keys 5, 6, 7, and 8

Bursts always operate in an A-B sequence. If Keys 5 to 8 are not implemented, the QST device will not perform the Burst B to improve the response time and reduce the power consumption when in Low Power (LP) mode.

In Low Power mode, the device sleeps in an ultra-low current state between bursts to conserve power.

4.3 Low power mode

In order to reduce the device power consumption, the QST family include scalable low power modes.

- Standard low power mode

  When the device is in standard low power mode, a window with very low power consumption is inserted between the acquisition of the last active key and the following acquisition of the first active key.

  This window duration is programmable as the 'sleep duration time'.

  Note that the sleep window insertion is cancelled in the following conditions:

  – If a change is detected on a key, in order to speed up the DI process, the sleep window insertion is skipped until the end of the DI process.

  – In I^2C mode, when a key change is actually detected and reported with a negative pulse on the $\overline{\text{IRQ}}$ pin. In this case, the low power mode is disabled until a command is received from the host.

  – Inside an I^2C command, between the Write and the Read I^2C frames, the sleep period is skipped.

- Free run in detect

  The behavior in this mode is the same as in the standard low power mode except that the sleep window insertion is always skipped if any of the active keys is detected as touched.

  This is useful to improve the wheel response time.

- Deep Sleep mode

  In Deep Sleep mode, the device enters a very low power mode indefinitely. The device resumes its operations after receiving an I^2C frame with any address or a reset.

Caution: If an I^2C frame is received while in Sleep or Deep Sleep mode, the device wakes up but does not acknowledge the frame (even if it has an I^2C frame with the device address). The host must therefore send again the frame until it is taken in account and acknowledged.

4.4 Mode selection

The device options are configured by connecting pull-up or pull-down resistors on OPTn pins. The device operating mode is selected using option pin 1 (OPT1) while the device settings are configured using option pins OPT2 to OPT6 (*Table 3*). Option pins are sampled at power-up and after a reset.

To fit most applications, the QST108 device offers two different operating modes:

- Stand-alone mode

  This mode allows the user to simply replace existing mechanical switches with a capacitive sensing solution. It is designed for maximum flexibility and can accommodate most popular sensing requirements via option resistors (AKS, Low power, Max On-Duration and output modes).

  In this mode, the 8 output pins reflect the status of the 8 sensing channels.

- I^2C mode

  In this mode, which is the most open one, the device is driven using the I^2C interface. To avoid polling, the QST device features an output interrupt pin ($\overline{IRQ}$). The $\overline{IRQ}$ line reports all key changes to the Master device. The QST (Slave) device can drive up to five general-purpose outputs.

Table 3. Operating modes

OPT1: Mode selection		Option resistor function				
		OPT2	OPT3	OPT4	OPT5	OPT6
Pin OPT1 is high at start-up	Stand-alone mode	AKS	LP	MOD_0	MOD_1	OM
Pin OPT1 is low at start-up	I^2C mode	ADD0	ADD1	ADD2	Unused	Unused

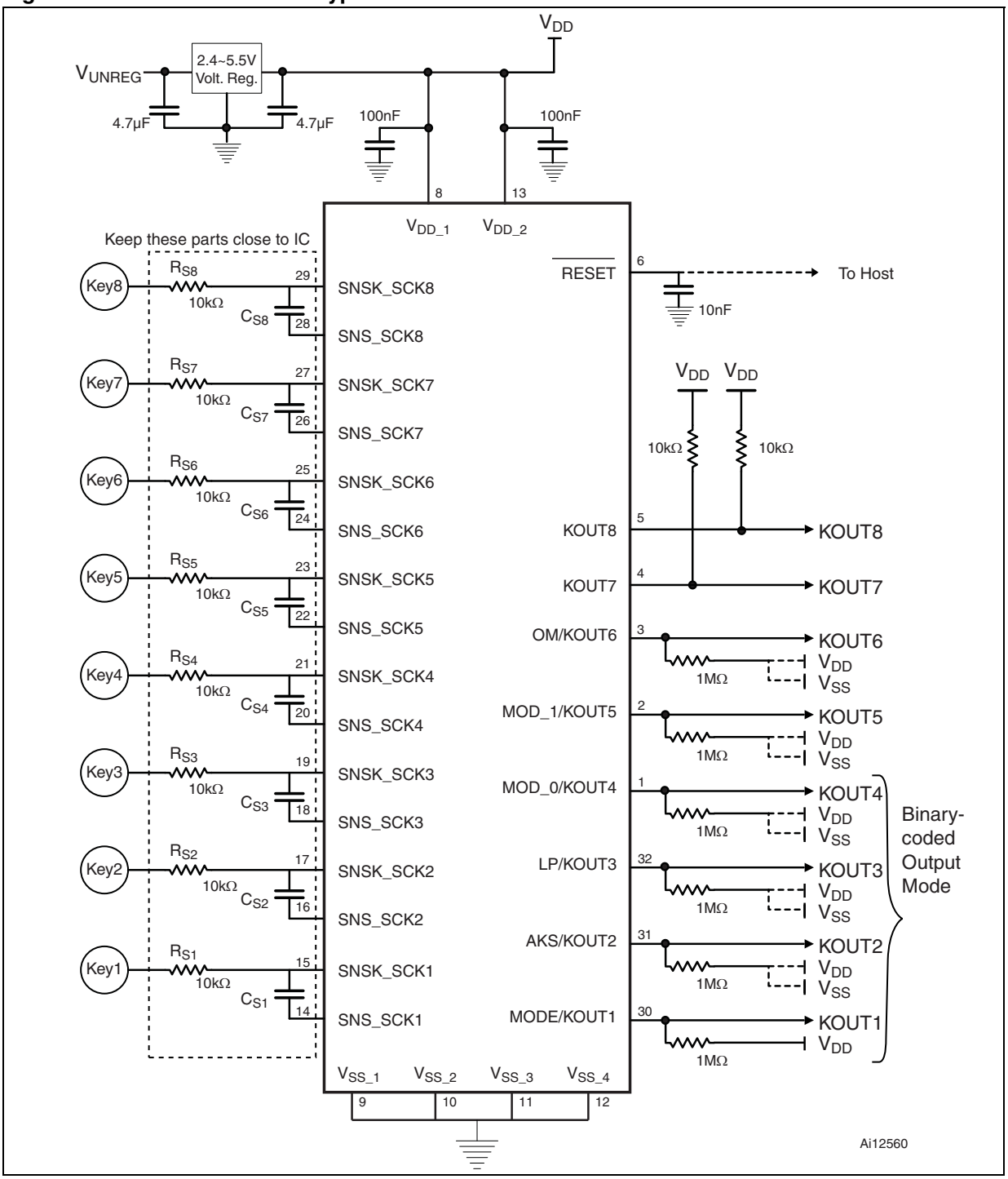
4.5 Stand-alone mode

This mode allows the user to simply replace existing mechanical switch interface with a capacitive sensing solution. It is designed for maximum flexibility and can accommodate most popular sensing requirements via option resistors (see *Figure 5*).

4.5.1 Main features

- Pins KOUT1 to KOUT8 directly reflect the state of keys
- Selectable global adjacent key suppression (AKS™)
- Selectable sleep duration
- Selectable Max On-Duration values
- Selectable BCD mode

Figure 5. Stand-alone mode typical schematic



4.5.2 KOUT outputs

KOUTn outputs directly reflect the state of keys. These pins are push-pull outputs except for pins KOUT7 and KOUT8 which are true open-drain outputs. Under RESET, these pins are floating and their state depends on the option resistors. Pins KOUTn are active high meaning that when a key is “touched”, the corresponding KOUT pin outputs a ‘1’.

4.5.3 Option descriptions

Adjacent key suppression (AKS™)

The QST108 features an adjacent key suppression (AKS™) function.

This function is enabled using the AKS option resistor (OPT2) in standard output mode as described in *Table 4*. In BCD output mode, the AKS function is always enabled, regardless of the option resistor configuration.

Table 4. AKS truth table

OPT2/AKS	Description
V_{SS}	Disabled
V_{DD}	Global locking AKS on all available keys

Low Power mode option

This option resistor (OPT3) selects whether the device is always sensing the keys or if a low power consumption phase is introduced between bursts as described in *Table 5*.

In Low Power mode, a very low consumption (sleep) phase of 100ms is inserted between the Group B burst and the Group A burst. This significantly reduces the overall consumption of the device. Sleep duration is not accurate and can vary substantially depending on V_{DD} and temperature values.

Note: In Low Power mode, the response time is increased.

Table 5. Low power (LP) mode truth table

OPT3/LP	Description
V_{SS}	Free running mode
V_{DD}	100ms sleep duration

Max On-Duration

There are four recalibration timing options (“Max On-Duration”). The recalibration option resistors (OPT4 and OPT5) control how long it takes for a continuous detection to trigger a recalibration on a key as described in *Table 6*. When such an event occurs, only the “stuck” key is recalibrated.

Table 6. Max On-Duration (MOD) truth table

OPT4/MOD_0	OPT5/MOD_1	Description
V_{SS}	V_{SS}	Infinite
V_{SS}	V_{DD}	60s
V_{DD}	V_{SS}	20s
V_{DD}	V_{DD}	10s

Output mode option

The QST108 offers several outputs mode to fit any existing application.

Table 7. Output mode (OM) truth table

OPT6/OM	Description
V_{SS}	Individual key state output mode: One output per sensing channel
V_{DD}	BCD output mode: Binary-coded touched key number (see *Table 8*)(1)

1. In BCD mode, the AKS function must be enabled.

Table 8. Binary code truth table

KOUT4	KOUT3	KOUT2	KOUT1	Description
0	0	0	0	All released
0	0	0	1	Key 1 pressed
0	0	1	0	Key 2 pressed
0	0	1	1	Key 3 pressed
0	1	0	0	Key 4 pressed
0	1	0	1	Key 5 pressed
0	1	1	0	Key 6 pressed
0	1	1	1	Key 7 pressed
1	0	0	0	Key 8 pressed
Other				Not used

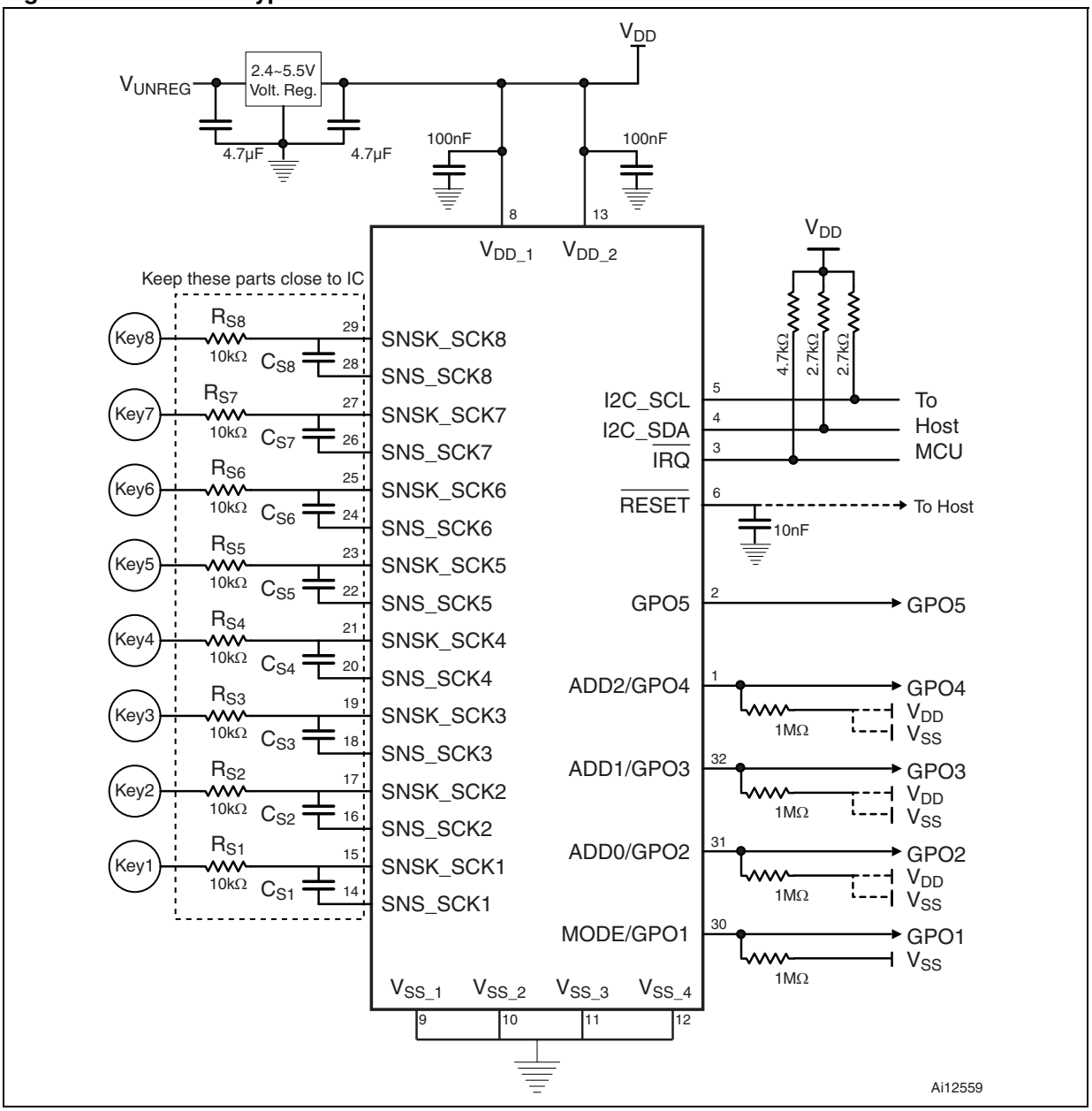
4.6 I²C mode

The I²C mode offers the largest configurability and functionality of the QST108.

4.6.1 Main features

- 5 general-purpose outputs
- Configuration of up to 8 AKS groups
- Additional low power modes
- Accessible internal capacitive sensing parameters
- Continuous range of Max On-Duration

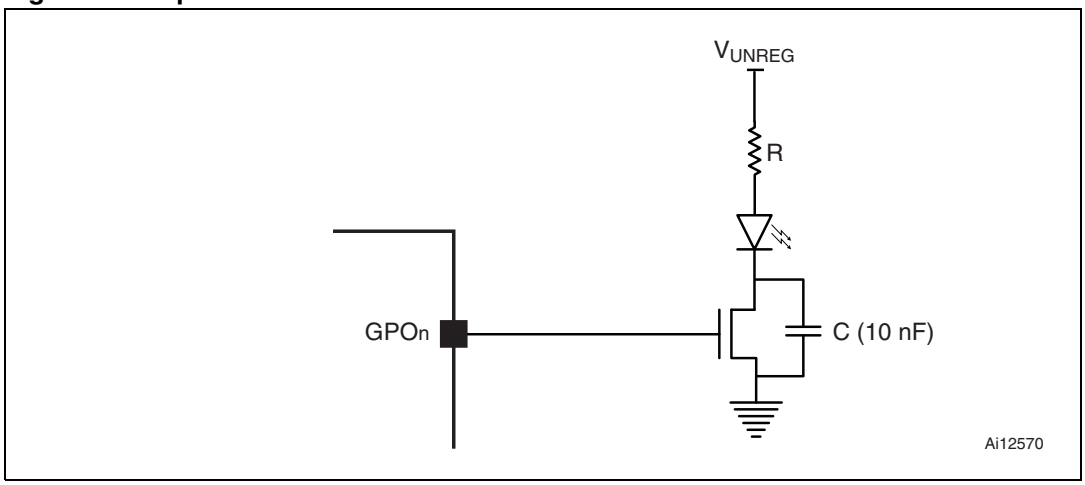
Figure 6. I²C mode typical schematic



4.6.2 General-purpose outputs

I²C mode allows to drive up to 5 general-purpose outputs. These output pins are configured in output push pull mode 0 by default. Their state can be changed using the SET_GPIO_STATE I²C command.

Figure 7. Optional LED schematic



4.6.3 $\overline{\text{IRQ}}$ pin

The $\overline{\text{IRQ}}$ pin is an open drain output with an internal pull-up. It can be used to inform the Master device about any change in the key status. The $\overline{\text{IRQ}}$ line is pulled low every time the state of any of the enabled keys changes. This includes any change in the touch state of the key, a faulty key or a new calibration of one or more keys. The reported changes may then be accessed by the Master device by using the GET_KEY_STATE command.

To improve communication response time, this signal suspends Low Power mode until the Master device has issued a communication with the QST device.

4.6.4 Communication packet

The communication between the Master device and the QST108 (Slave) consists of two standard I²C frames.

The first frame is sent by the Master device using the QST108 device address with the write bit set. The data bytes consist of the command byte which is eventually followed by the parameters and a checksum byte.

The second one is sent by the Master device using the QST108 device address with the write bit reset. The QST108 completes the frame with data according to the command previously sent by the Master device. The device finishes the frame by sending a checksum byte for communication integrity verification.

If the read frame is omitted, the command may not be taken into account.

To initiate the communicate with the QST108, the Master device must send the GET_DEVICE_INFO command in order to unlock access to all the other commands.

4.6.5 I²C address selection

The QST108 slave address is programmable using the option resistors mapped on pins OPT2 to OPT4 (see *Table 9*).

Table 9. I²C address versus option resistor

Option configuration			I²C Address				
OPT4	OPT3	OPT2	ADD[6:3]	ADD2	ADD1	ADD0	Hex value
V_{SS}	V_{SS}	V_{SS}	0101	0	0	0	0x28
V_{SS}	V_{SS}	V_{DD}		0	0	1	0x29
V_{SS}	V_{DD}	V_{SS}		0	1	0	0x2A
V_{SS}	V_{DD}	V_{DD}		0	1	1	0x2B
V_{DD}	V_{SS}	V_{SS}		1	0	0	0x2C
V_{DD}	V_{SS}	V_{DD}		1	0	1	0x2D
V_{DD}	V_{DD}	V_{SS}		1	1	0	0x2E
V_{DD}	V_{DD}	V_{DD}		1	1	1	0x2F

4.7 Supported commands

Table 10 lists the supported I²C commands and available arguments.

Note: For more information on the supported commands and I²C protocol, please refer to the QST standard communication protocol reference manual.

Table 10. Supported commands

I²C commands		Description
CALIBRATE_KEY (All keys)		
Write	0x98	Forces the recalibration of all keys. *ErrCode*: Standard Error code (see *Table 11*)
Read	ErrCode	
CALIBRATE_KEY (Single key)		
Write	0x9B KeyID Checksum	Forces the recalibration of a single key. *KeyId:* Binary-coded key number (see *Table 14*) *ErrCode*: Standard Error code (see *Table 11*)
Read	ErrCode	
GET_DEBUG_INFO		
Write	0xF7 KeyID Checksum	Returns the debug info of the single KeyID channel. *KeyDbgState*: Current Key Debug state (see *Table 19*) *RefMSB*: Reference Count MSB *RefLSB*: Reference Count LSB *BCMSB*: Burst Count MSB *BCLSB*: Burst Count LSB
Read	0x0B KeyDbgState RefMSB RefLSB BCMSB BCLSB Checksum	

Table 10. Supported commands (continued)

I^2C commands		Description
GET_DEVICE_INFO		
Write	0x85	Returns the QST108 device version and ASCII-coded device name. This command must be sent first to enable the communication flow. *MainVers*: Device main version *SubVer*: Device sub-version *NbSCkey*: 0x08 single-channel keys *NbMCkey*: 0x00 multi-channel keys **Q S T 1 0 8**: ASCII-coded device name
Read	0x15 MainVers SubVers NbSCkey NbMCkey 'Q' 'S' 'T' '1' '0' '8' Checksum	
GET_KEY_ERROR		
Write	0xC4	Returns the error information on each key. *KeyErrorN*: KeyError byte description (see *Table 12*)
Read	0x10 KeyError1 KeyError2 ... KeyError8 CheckSum	
GET_KEY_STATE		
Write	0xC1	Returns the state of all keys. *AllKeyState*: Touched/untouched state for all 8 keys. Refer to *Table 13: AllKeyState*. *KeyError:* Refer to *Table 12: KeyError byte description*
Read	0x04 AllKeyState KeyError Checksum	
GET_PROTOCOL_VERSION		
Write	0x80	Returns the QST108 protocol version. *MainVers*: Protocol main version *SubVer*: Protocol sub-version *I2CSpeed*: 0x00 (100 kHz maximum)
Read	0x07 MainVers SubVer I2CSpeed Checksum	
RESET_DEVICE		
Write	0xFD	Restarts the device (options Read and Calibration) after reading the ErrCode (see *Table 11*).
Read	ErrCode	
SET_DETECT_INTEGRATORS		
Write	0x03 0x04 0x00 DI EDI PosRecalI CheckSum	Sets the detection, End Of Detection and Positive Recalibration Integrators for all keys. *DI*: Detection Integrator [1) 3)] *EDI*: End of Detection Integrator [1) 3)] *PosRecalI*: Positive Recalibration Integrator [1) 3)] *ErrCode*: Standard Error code (see *Table 11*)
Read	ErrCode	
SET_GPIO_STATE		
Write	0x08 0x01 GPOState Checksum	Controls the state of the general-purpose outputs. *GPOState:* State of general-purpose outputs (see *Table 16*) *ErrCode*: Standard Error code (see *Table 11*)
Read	ErrCode	

Table 10. Supported commands (continued)

I²C commands		Description
SET_KEY_ACTIVATION (see *Note 4*)		
Write	0x97 KeyActivation Checksum	Enables or disables a single key. *KeyActivation*: Byte containing the key number selection and requested state. *ErrCode*: Standard Error code (see *Table 11*)
Read	ErrCode	
SET_KEY_GROUP		
Write	0x00 0x09 AKSGrpMode Key1Grp Key2Grp ...Key8Grp CheckSum	Defines the AKS groups for each key. *AKSGrpMode*: AKS mode selection of each group (see *Table 17*) *KeynGrp*: AKS group selection for key n (see *Table 18*) *ErrCode*: Standard Error code (see *Table 11*)
Read	ErrCode	
SET_LOW_POWER_MODE		
Write	0x92 LowPowerMode Checksum	Selects standard or Low Power mode. *LowPowerMode:* Configure Low Power mode (see *Table 15*) *ErrCode*: Standard Error code (see *Table 11*)
Read	ErrCode	
SET_MAX_ON_DURATION		
Write	0x8A MaxOnDuration Checksum	Sets the maximum detected ON time before triggering an automatic recalibration. *MaxOnDuration:* Time, in second (0 for infinite) *ErrCode*: Standard Error code (see *Table 11*)
Read	ErrCode	
SET_SCKEY_PARAMETERS		
Write	0x01 0x04 0x00 DeTh EofDeTh PosRecalTh Checksum	Sets the Detection, End Of Detection and Positive Recalibration Thresholds for a single key. *DeTh*: Detection Threshold [1) 2)] *EofDeTh*: End of Detection Threshold [1) 2)] *PosRecalTh*: Positive Recalibration Threshold [1) 2)] *ErrCode*: Standard Error code (see *Table 11*)
Read	ErrCode	

Note: 1 See Section 6.6: Capacitive sensing characteristics on page 35 for default values.

2 The value is a signed character (0x80...0x7F <=> -128 ... +128).

3 The value is an unsigned number (0x01..0xFF <=> 1 ... 255).

4 Enabling or disabling keys triggers a new calibration of all enabled keys.

Error codes

Table 11 lists the I^{2}C error codes.

Table 11. ErrCode

ErrCode	Description
0x01	No Error
0x83	Command not supported
0x85	Parameter not supported
0xA1	Parity Error
0xA3	Checksum Error
0xE0	Initialization process (GET_FIRMWARE_INFO command not received)

KeyError byte description

Table 12. KeyError byte description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Key State	0	0	0	0	Key error codes		

Key state (Bit 7)

When set to ‘1’, the corresponding key is touched. This bit is always cleared for the GET_KEY_STATE command.

Key error codes (Bits 2:0)

When answering the GET_KEY_STATE command, the key error code corresponds to the error codes of all the keys ORed toghether. When answering the GET_KEY_ERROR command, each key error code describes the errors of one defined key.

Bit 0: When set to ‘1’, calibration in progress
Bit 1: When set to ‘1’, maximum count reached
Bit 2: When set to ‘1’, minimum count not reached

All key state description

Table 13. AllKeyState

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Key 8 State	Key 7 State	Key 6 State	Key 5 State	Key 4 State	Key 3 State	Key 2 State	Key 1 State

Key n state

When set to ‘1’, the corresponding key is touched.

Key activation description

Table 14. KeyActivation

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Key Activation	0	0	0	Key ID (binary coded)			

Key activation (Bit 7)

0: Key disabled
1: Key enabled

Key identifier (Bits 3:0)

0000: All keys
0001: Key 1
0010: Key 2
0011: Key 3
0100: Key 4
0101: Key 5
0110: Key 6
0111: Key 7
1000: Key 8

Low power mode description

Table 15. SetLowPower

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Free Run in Detect	Sleep Duration Factor					

Free Run in Detect (Bit 6)

0: Low Power mode is always enabled, whatever the state of the keys.
1: Low Power mode is automatically suspended when any key is in Detect state. Low Power mode is automatically resumed when no key is in Detect state.

Sleep Duration Factor (Bits 5 to 0)

0x00 or 0x1A to 0x3E: Low power mode is disabled.

0x01 to 0x19: Low Power mode. The sleep duration is 'Sleep Duration Factor' x 20 milliseconds (20 ms to 500 ms)
0x3F: Deep Sleep mode is entered immediately. A reset or any I2C communication can be used to exit Deep Sleep mode.

Note: When the device is in Sleep or Deep Sleep, any I^2C bus activity will wake-up the device.

The I^2C QST device address is not acknowledged but forces the QST device to exit from Low Power mode. The Master device will have to repeat the command to ensure that it is taken in account.

GPO state description

Table 16. GPOState

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	GPO 5 state	GPO 4 state	GPO 3 state	GPO 2 state	GPO 1 state

GPOState

Defines the state of the selected general-purpose output pin. For more information, see *Section 4.6.2: General-purpose outputs on page 20*.

0: GPO state is ‘0’
1: GPO state is ‘1’

AKS group mode description

Table 17. AKSGrpnMode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AKSGrp8 Mode	AKSGrp7 Mode	AKSGrp6 Mode	AKSGrp5 Mode	AKSGrp4 Mode	AKSGrp3 Mode	AKSGrp2 Mode	AKSGrp1 Mode

AKSGrpnMode

Defines the type of AKS for the Group n:

0: Locking AKS: First key pressed within the group locks out all other keys.

1: Unlocking AKS: Most heavily pressed key (highest signal level) is selected over all other keys in the group.

AKS group selection description

Table 18. KeynGrp

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Grp8	Grp7	Grp6	Grp5	Grp4	Grp3	Grp2	Grp1

Grpx

The selected key is a member of AKS Group x.

Key debug state description

Table 19. KeyDbgState

Value	Description
0x01	On-going calibration
0x02	Key released
0x04	Key touched
0x08	Key in error
0x11	Key calibration filter triggered (PosRecall)
0x14	Key detection filter triggered (DI)
0x24	Key end of detection filter triggered (EDI)

5 Design guidelines

5.1 C_S sense capacitor

The C_S sense capacitors accumulate the charge from the key electrodes and determine sensitivity. Higher values of C_S make the corresponding sensing channel more sensitive. The values of C_S can differ for each channel, permitting differences in sensitivity from key to key or to balance unequal sensitivities. Unequal sensitivities can occur due to key size and placement differences and stray wiring capacitances. More stray capacitance on a sense trace will desensitize the corresponding key. Increasing the C_S for that key will compensate for the loss of sensitivity.

The C_S capacitors can be virtually any plastic film or low- to medium-K ceramic capacitor. The normal C_S range is 1nF to 50nF depending on the sensitivity required: larger values of C_S require better quality to ensure reliable sensing. In certain circumstances the normal C_S range may be exceeded. Acceptable capacitor types for most uses include PPS film, polypropylene film, and NP0 and X5R / X7R ceramics. Lower grades than X5R or X7R are not recommended.

5.2 Sensitivity tuning

Sensitivity can be altered to suit various applications and situations on a channel-by-channel basis. The easiest and most direct way to impact sensitivity is to alter the value of each C_S: more C_S yields higher sensitivity. Each channel has its own C_S value and can therefore be independently adjusted.

5.2.1 Increasing sensitivity

Sensitivity can also be increased by using larger electrode areas, reducing panel thickness, or using a panel material with a higher dielectric constant.

5.2.2 Decreasing sensitivity

In some cases the circuit may be too sensitive. Gain can be lowered further by a number of strategies:

- making the electrode smaller
- making the electrode into a sparse mesh using a high space-to-conductor ratio
- decreasing the C_S capacitors

5.2.3 Key balance

A number of factors can cause sensitivity imbalances. Notably, SNS wiring to electrodes can have differing stray amounts of capacitance to ground. Increasing load capacitance will cause a decrease in gain. Key size differences, and proximity to other metal surfaces can also impact gain.

The keys may thus require “balancing” to achieve similar sensitivity levels. This can be best accomplished by trimming the values of the C_S capacitors to achieve equilibrium. The R_S resistors have no effect on sensitivity and should not be altered. Load capacitances to ground can also be added to overly sensitive channels to reduce their gain.

These should be in the order of a few picofarads.

5.3 Power supply

If the power supply fluctuates slowly with temperature, the QST device compensates automatically for these changes with only minor changes in sensitivity. However, if the supply voltage drifts or shifts quickly, the drift compensation mechanism is not able to keep up, causing sensitivity anomalies or false detections.

The power supply should be locally regulated, using a three-terminal regulator. If the supply is shared with another electronic system, care should be taken to ensure that the supply is free of digital spikes, sags and surges which can cause adverse effects. It is not recommended to include a series inductor in the power supply to the QST device.

For proper operation, a 0.1 µF or greater bypass capacitor must be used between V_{DD} and V_{SS}. The bypass capacitor should be routed with very short tracks to the device's V_{DD} and V_{SS} pins.

The PCB should, if possible, include a copper pour under and around the device, but not extensively under the SNS lines.

5.4 ESD protection

In normal environmental conditions, only one series resistor is required for ESD suppression. A 10 kOhm R_S resistor in series with the sense trace is sufficient in most cases. The dielectric panel (glass or plastic) usually provides a high degree of isolation to prevent ESD discharge from reaching the circuit. R_S should be placed close to the chip. If the C_X load is high, R_S can prevent total charge and transfer and as a result gain can deteriorate. If a reduction in R_S increases gain noticeably, the lower value should be used. Conversely, increasing the R_S can result in added ESD and EMC benefits, provided that the increase does not decrease sensitivity.

5.5 Crosstalk precautions

Adjacent sense traces might require intervening ground traces in order to reduce capacitive cross bleed if high sensitivity is required or high values of delta-C_X are anticipated (for example, from direct human touch to an electrode connection). In normal touch applications behind plastic panels, this is rarely a problem regardless of how the electrodes are wired.

Higher values of R_S will make crosstalk problems worse; try to keep R_S to 22 kOhm or less if possible. In general try to keep the QST device close to the electrodes and reduce the adjacency of the sense wiring to ground planes and other signal traces; this will reduce the C_x load, reduce interference effects, and increase signal gain. The one and only valid reason to run ground near SNS traces is to provide crosstalk isolation between traces, and then only on an as-needed basis.

5.6 PCB layout and construction

The PCB traces, wiring, and any components associated with or in contact with either SNS pin will become touch sensitive and should be treated with caution to limit the touch area to the desired location.

Multiple touch electrodes connected to any sensing channel can be used, for example, to create control surfaces on both sides of an object.

It is important to limit the amount of stray capacitance on the SNS terminals, for example by minimizing trace lengths and widths to allow for higher gain without requiring higher values of C_S. Under heavy delta-C_X loading of one key, cross coupling to another key's trace can cause the other key to trigger. Therefore, electrode traces from adjacent keys should not be run close to each other over long runs in order to minimize cross-coupling if large values of delta-C_X are expected, for example when an electrode is directly touched. This is not a problem when the electrodes are working through a plastic panel with normal touch sensitivity.

For additional information on PCB layout and construction, please contact your local ST Sales Office for a list of available application notes.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5 V (for the 4.5V ≤ V_{DD} ≤ 5.5 V voltage range) and V_{DD} = 3.3 V (for the 3.0 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

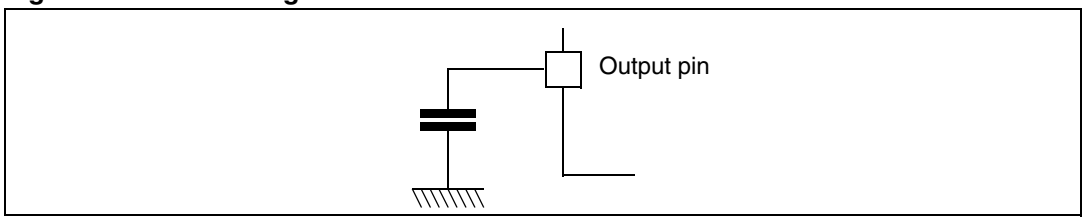
6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

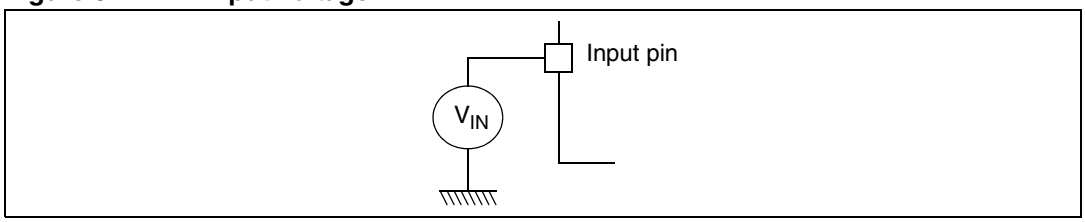
Figure 8. Pin loading conditions



6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 9. Pin input voltage



6.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature		

Table 21. Voltage characteristics

Symbol	Ratings	Maximum value	Unit
$V_{DD} - V_{SS}$	Supply voltage	7.0	V
V_{IN}	Input voltage on any pin (1)(2)	V_{SS}–0.3 to V_{DD}+0.3	

1. Directly connecting the $\overline{\text{RESET}}$ and I/O pins to V_{DD} or V_{SS} could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs. To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7kΩ for $\overline{\text{RESET}}$, 10kΩ for I/Os).
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected.

Table 22. Current characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	75	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by $\overline{\text{RESET}}$ pin	20	
	Output current sunk by output pin	40	
	Output current source by output pin	– 25	
$I_{INJ(PIN)}$(2)(3)	Injected current on $\overline{\text{RESET}}$ pin	± 5	
	Injected current output pin	± 5	
$\Sigma I_{INJ(PIN)}$(2)	Total injected current (sum of all I/O and control pins)	± 20	

1. All power (V_{DD}) and ground (V_{SS}) lines must always be connected to the external supply.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly ensured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterisation with $\Sigma I_{INJ(PIN)}$ maximum current injection on four KOUT pins of the device.

6.3 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

6.3.1 Functional EMS (electro magnetic susceptibility)

The product is stressed by two electro magnetic events until a failure occurs:

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Table 23. Functional EMS

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5V, T_A=+25°C, complies with IEC 1000-4-2	3B
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{DD} pins to induce a functional disturbance	V_{DD}=5V, T_A=+25°C complies with IEC 1000-4-4	4A

6.3.2 Electro magnetic interference (EMI)

The product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 24. EM emissions

Symbol	Parameter	Conditions	Monitored Frequency Band	f_{DEVICE} = 4 MHz (1)	Unit
S_{EMI}	Peak level	V_{DD}=5V, T_A=+25°C, complies with SAE J 1752/3	0.1 MHz to 30 MHz	20	dBµV
			30 MHz to 130 MHz	20	
			130 MHz to 1 GHz	13	
			SAE EMI Level	2.5	-

1. Data based on characterization results, not tested in production.

6.3.3 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electro-static discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Charge Device Model. These tests comply with JESD22-A114A/A115A specifications.

Table 25. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	4000	V
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charge Device Model)	T_A=+25°C	500	V

1. Data based on characterization results, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each I/O pin) are performed on each sample. This test complies with EIA/JESD 78 IC latch-up specifications.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the MCU is running to assess the latch-up performance in Dynamic mode. Power supplies are set to the typical values and the component is put in Reset mode. This test complies with IEC1000-4-2 and SAEJ1752/3 specifications.

For more details, refer to the application note AN1181.

Table 26. Electrical sensitivities

Symbol	Parameter	Conditions	Class (1)
LU	Static latch-up class	T_A=+125°C	A
DLU	Dynamic latch-up class	V_{DD}=5.5V, f_{DEVICE} = 4MHz, T_A=+25°C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

6.4 Operating conditions

Table 27. Operating conditions

Symbol	Feature	Value	Unit
V_{DD}	Operating supply voltage	2.4 to 5.5	V
T_A	Operating temperature	-40° to +85°	C

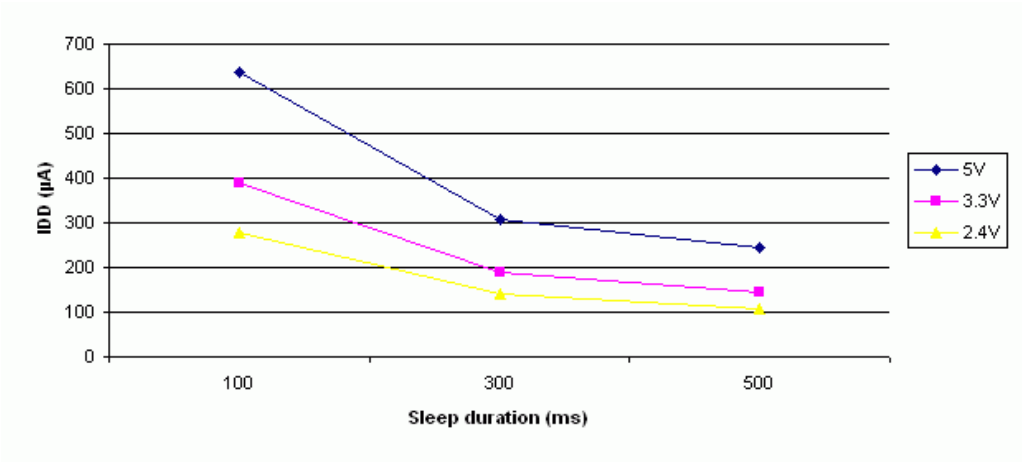
6.5 Supply current characteristics

Table 28. Supply current characteristics

Symbol	Parameter	Conditions	Min.	Typ. (1)	Max.	Unit
I_{DD} (FR)	Average suppy current Free Run mode	V_{DD} = 2.4 V		1.71		mA
		V_{DD} = 3.3 V		2.17		
		V_{DD} = 5 V		3.35		
I_{DD} (Sleep 100ms)	Average suppy current 100ms Sleep mode	V_{DD} = 2.4 V		276		µA
		V_{DD} = 3.3 V		389		
		V_{DD} = 5 V		637		
I_{DD} (Sleep 500ms)	Average suppy current 500ms Sleep mode	V_{DD} = 2.4 V		108		µA
		V_{DD} = 3.3 V		144		
		V_{DD} = 5 V		246		
I_{DD} Deep Sleep	Average suppy current Deep Sleep mode				5	µA

1. The results are based on C_S = 2.7nF and C_X = 12.5pF

Figure 10. IDD Sleep mode current characteristics



6.6 Capacitive sensing characteristics

Table 29. External sensing components

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_S	Sense capacitor			100	nF
C_X	Equivalent electrode capacitor			100	pF
C_T	Equivalent touch capacitor		5		pF
R_S	Serial resistor		10	22	kOhm

Table 30. Capacitive sensing parameters

Symbol	Parameter	Min.	Default	Max.	Unit
t_{CAL}	Calibration duration			2	s
t_{Setup}	Setup duration		100		ms
DI	Detection integrator	1	2	255	Samples
DeTh	Detection threshold	-128	-10	-1	Counts
EDI	End of detection integrator	1	2	255	Samples
EofDeTh	End of detection threshold	-128	-6	-1	Counts
PosRecalI	Positive recalibration integrator	1	2	255	Samples
PosRecalTh	Positive recalibration threshold	1	15	127	Counts
MaxOnDuration	Max on-duration delay	1	Infinite	255	s
PosDiffDrift	Positive differential drift compensation rate	0.1	1	25.5	s/level
NegDiffDrift	Negative differential drift compensation rate	0.1	1	25.5	s/level
PosComDrift	Positive common drift compensation rate	0.1	0.2	25.5	s/level
NegComDrift	Negative common drift compensation rate	0.1	0.2	25.5	s/level
PosDriftI	Positive drift integrator	0	10	255	
NegDriftI	Negative drift integrator	0	10	255	
ComFact	Common time step factor	0	2	255	
DiffFact	Differential time step factor	0	10	255	
BurstCount	Burst length	20		2000	Counts

6.7 KOUTn/OPTn/GPOn pin characteristics

6.7.1 General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 31. General characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage (1)		V_{SS} –0.3		0.3x V_{DD}	V
V_{IH}	Input high level voltage (1)		0.7x V_{DD}		V_{DD} + 0.3	
V_{Hys}	Schmitt trigger voltage hysteresis(2)			400		mV
I_L	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA
C_{IO}	I/O pin capacitance			5		pF
$t_{f(IO)out}$	Output high to low level fall time (2)	C_L = 50 pF Between 10% and 90%		25		ns
$t_{r(IO)out}$	Output low to high level rise time (2)			25		

1. Not tested in production, guaranteed by characterization.
2. Data based on validation/design results.

6.7.2 Output pin characteristics

Subject to general operating conditions for V_{DD}, f_{CPU}, and T_A unless otherwise specified.

Table 32. Output pin current

Symbol	Parameter	Conditions		Min.	Max.	Unit
V_{OL}(1)	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time (*Figure 16*)	V_{DD} = 5V	I_{IO} = +20mA		1.3	V
			I_{IO} = +8mA		0.75	
V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time (*Figure 21*)		I_{IO} = -5mA	V_{DD}–1.5		
			I_{IO} = -2mA	V_{DD}–0.8		
V_{OL}(1)(3)	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time	V_{DD} = 3.3V	I_{IO} = +8mA		0.5	
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 4 pins are sourced at same time (*Figure 19*)		I_{IO} = -2mA	V_{DD}–0.8		
V_{OL}(1)(3)	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time	V_{DD} = 2.4V	I_{IO} = +8mA		0.6	
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 4 pins are sourced at same time		I_{IO} = -2mA	V_{DD}–0.9		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 22* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 22* and the sum of I_{IO} (output and $\overline{\text{RESET}}$ pins) must not exceed I_{VDD}..
3. Not tested in production, based on characterization results.

Figure 11. Typical V_{OL} at V_{DD} = 2.4 V

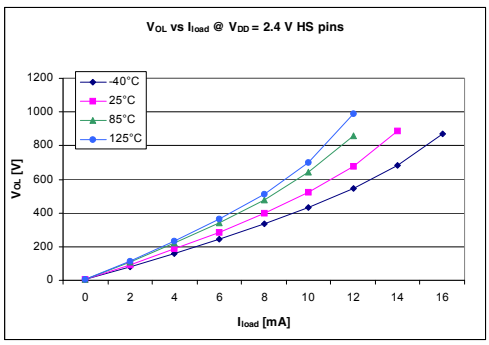


Figure 12. Typical V_{OL} vs V_{DD} at I_{load} = 2 mA

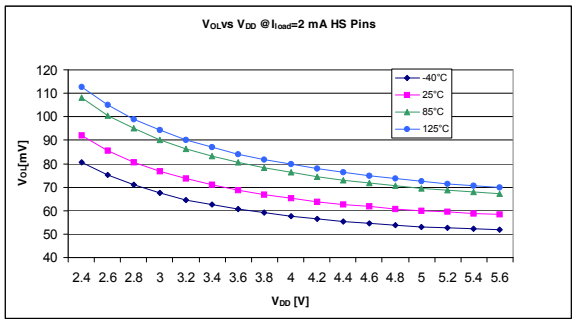


Figure 13. Typical V_{OL} at V_{DD} = 3 V

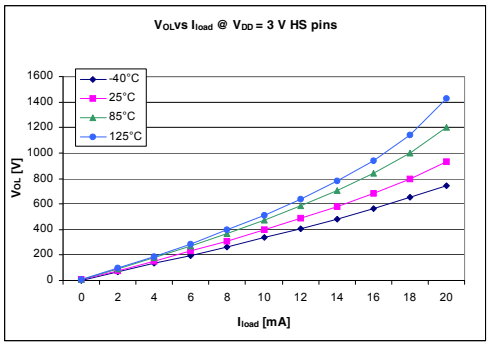


Figure 14. Typical V_{OL} vs V_{DD} at I_{load} = 8 mA

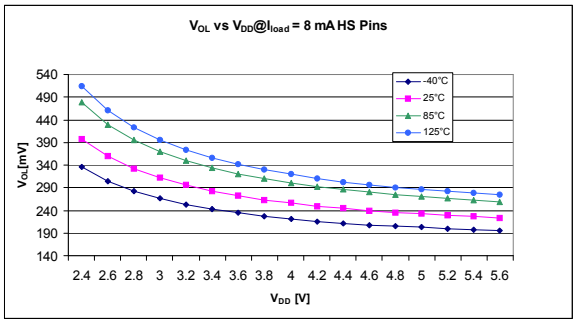


Figure 15. Typical V_{OL} at V_{DD} = 5 V

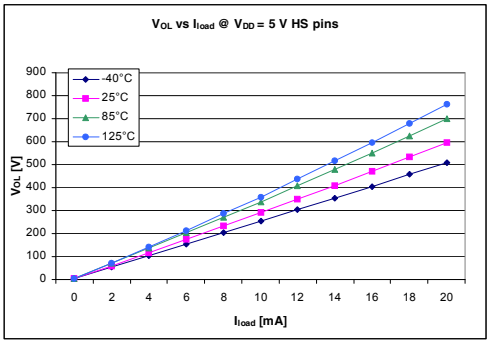


Figure 16. Typical V_{OL} vs V_{DD} at I_{load} = 12 mA

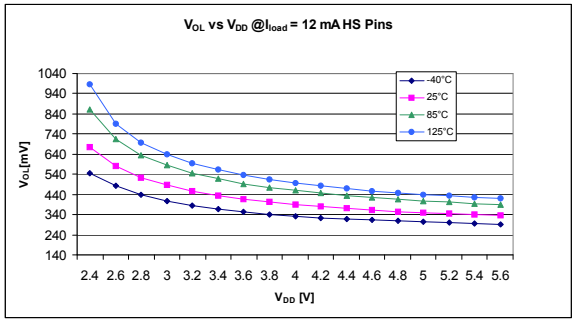


Figure 17. Typical V_{DD}-V_{OH} vs. I_{load} at V_{DD} = 2.4 V

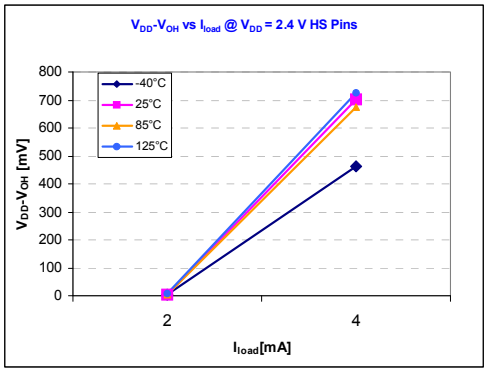


Figure 18. Typical V_{DD}-V_{OH} vs. V_{DD} at I_{load} = 2 mA

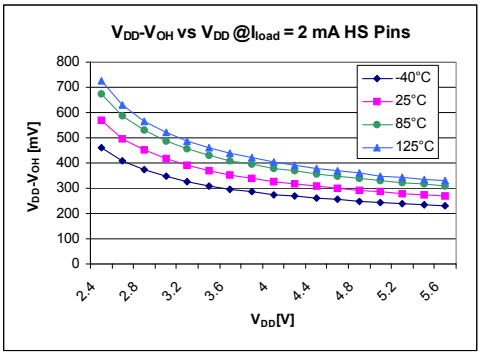


Figure 19. Typical V_{DD}-V_{OH} vs. I_{load} at V_{DD} = 3 V

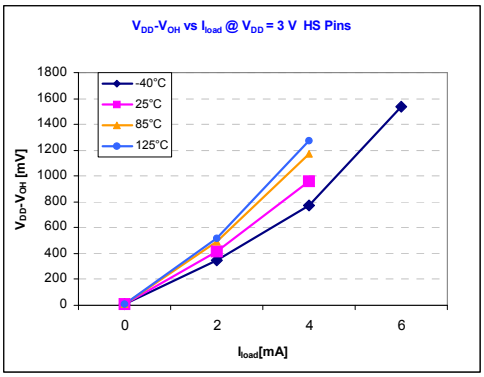


Figure 20. Typical V_{DD}-V_{OH} vs. V_{DD} at I_{load} = 4 mA

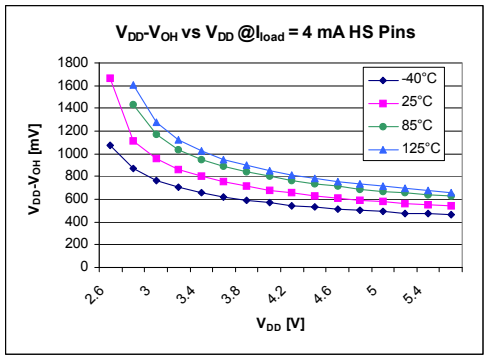
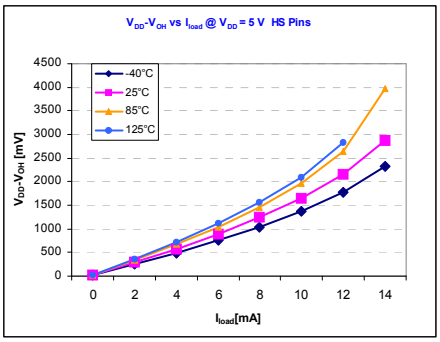


Figure 21. Typical V_{DD}-V_{OH} vs. I_{load} at V_{DD} = 5 V



6.8 $\overline{\text{RESET}}$ pin

T_A = -40°C to 125°C, unless otherwise specified.

Table 33. RESET pin characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage			V_{SS} – 0.3		0.3x V_{DD}	V
V_{IH}	Input high level voltage			0.7 x V_{DD}		V_{DD} + 0.3	
V_{hys}	Schmitt trigger voltage hysteresis(1)				2		V
V_{OL}	Output low level voltage(2)	V_{DD} = 5V	I_{IO} = +2mA		200		mV
R_{ON}	Pull-up equivalent resistor(3)	$V_{IN} = V_{SS}$	V_{DD} = 5V	30	50	70	kΩ
			V_{DD} = 3V		90(1)		
$t_{w(RSTL)out}$	Generated reset pulse duration	Internal reset sources			90(1)		µs
$t_{h(RSTL)in}$	External reset pulse hold time(4)			20			µs
$t_{g(RSTL)in}$	Filtered glitch duration				200		ns

1. Data based on characterization results, not tested in production.
2. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 22: Current characteristics on page 31* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The R_{ON} pull-up equivalent resistor is based on a resistive transistor. Specified for voltages on $\overline{\text{RESET}}$ pin between V_{ILmax} and V_{DD}.
4. To guarantee the reset of the device, a minimum pulse has to be applied to the $\overline{\text{RESET}}$ pin. All short pulses applied on $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.

6.9 I²C control interface

Subject to general operating conditions for V_{DD}, and T_A unless otherwise specified.

The QST108 I²C interface meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 34. I²C characteristics (100 kHz speed)

Symbol	Parameter	Min. (1)	Max. (1)	Unit
$t_{w(SCLL)}$	SCL clock low time	4.7		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		
$t_{su(SDA)}$	SDA setup time	250		ns
$t_{h(SDA)}$	SDA data hold time	0 (2)		
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	
$t_{h(STA)}$	START condition hold time	4.0		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		
$t_{su(STO)}$	STOP condition setup time	4.0		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		µs
C_b	Capacitive load for each bus line		400	pF

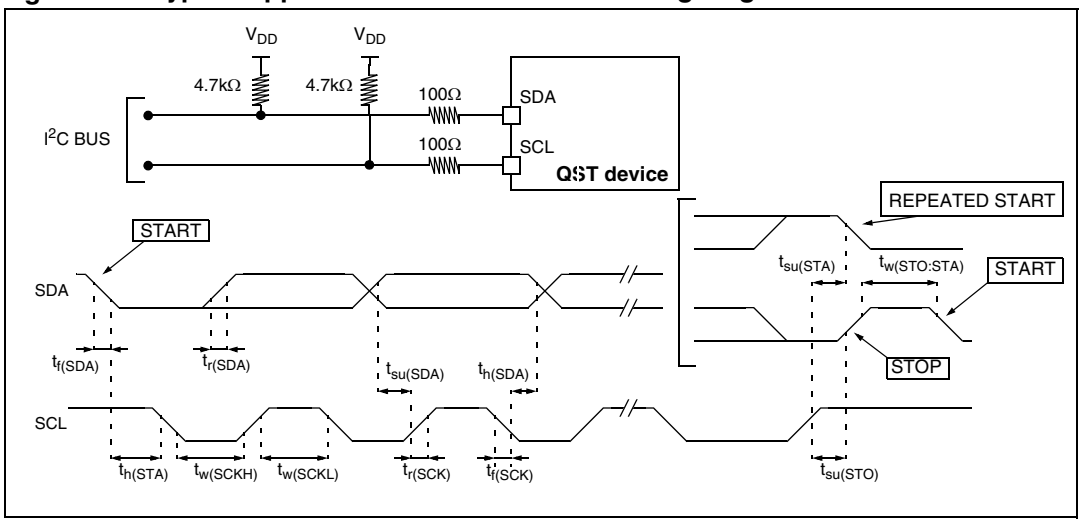
1. Data based on standard I2C protocol requirement, not tested in production.
2. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of the SCL signal.

Table 35. $\overline{IRQ}$ specific pin characteristics (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{W(IRQ)}$	$\overline{IRQ}$ pulse width		10		15	µs
R_{IRQ}	$\overline{IRQ}$ internal pull-up (2)	V_{DD} = 5V	100	120	140	kΩ
		V_{DD} = 3V		300		

1. For additional pin parameters, please use the pin description in *Section 6.7: KOUTn/OPTn/GPOn pin characteristics on page 36*.
2. The $\overline{IRQ}$ pull-up equivalent resistor is based on a resistive transistor.

Figure 22. Typical application with I²C bus and timing diagram



7 Package mechanical data

Figure 23. 32-pin low profile quad flat package (7x7) outline

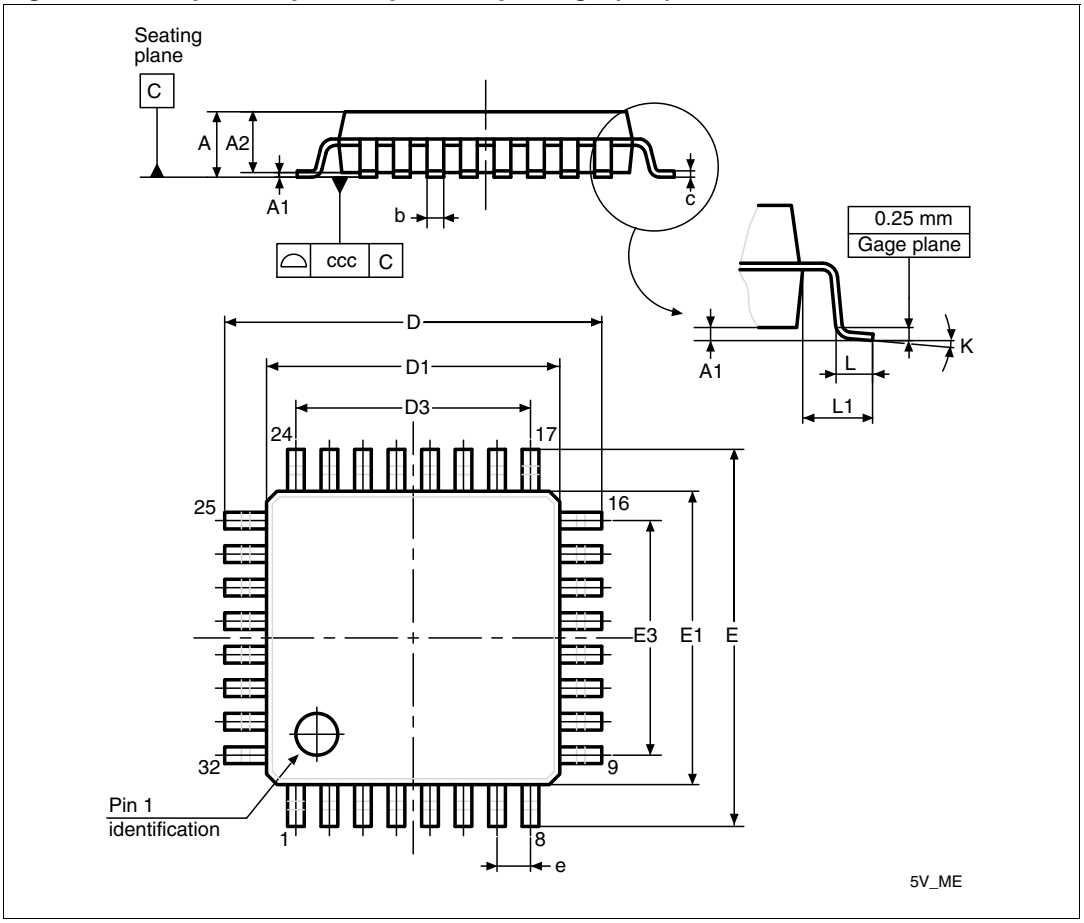
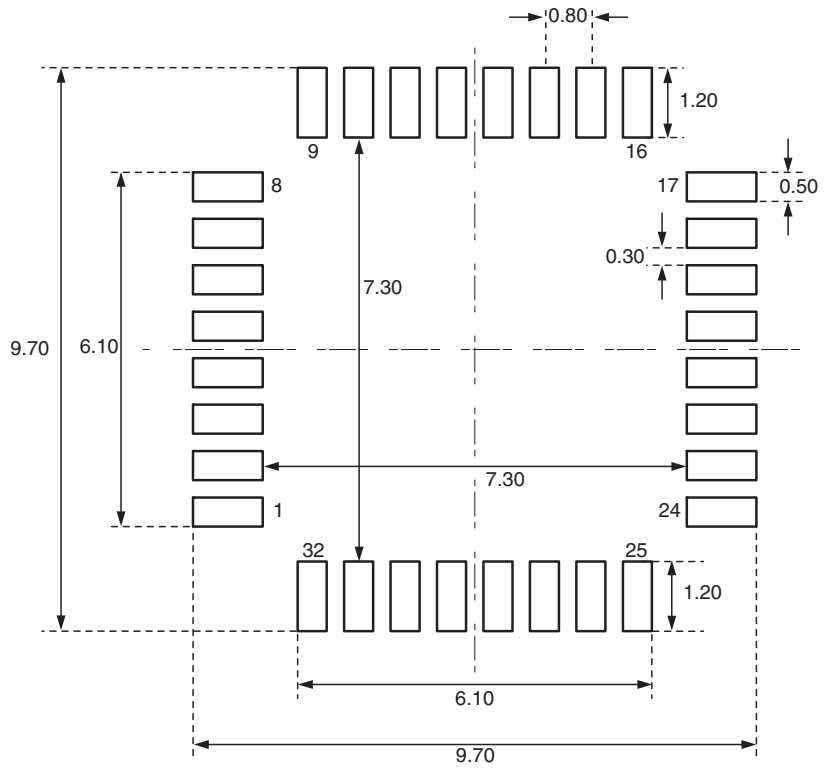


Table 36. 32-pin low profile quad flat package mechanical data

Dim.		mm			inches[1]	
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.600			0.2205	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.600			0.2205	
e		0.800			0.0315	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
K	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
	Tolerance (mm)			Tolerance (inches)		
ccc	0.10			0.0039		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 24. 32-pin LQFP32 (7x7 mm) recommended footprint



7.1 Soldering information

In accordance with the RoHS European directive, all STMicroelectronics packages have been converted to lead-free technology, named ECOPACK™.

- ECOPACK™ packages are qualified according to the JEDEC STD-020C compliant soldering profile.
- Detailed information on the STMicroelectronics ECOPACK™ transition program is available on www.st.com/stonline/leadfree/, with specific technical Application notes covering the main technical aspects related to lead-free conversion (AN2033, AN2034, AN2035, and AN2036).

Backward and forward compatibility

The main difference between Pb and Pb-free soldering process is the temperature range.

- ECOPACK™ LQFP, SDIP, SO and DFN8 packages are fully compatible with Lead (Pb) containing soldering process (see application note AN2034).
- LQFP, SDIP and SO Pb-packages are compatible with Lead-free soldering process, nevertheless it's the customer's duty to verify that the Pb-packages maximum temperature (mentioned on the Inner box label) is compatible with their Lead-free soldering temperature.

Table 37. Soldering Compatibility (wave and reflow soldering process

Package	Plating material devices	Pb solder paste	Pb-free solder paste (1)
SDIP & PDIP	Sn (pure Tin)	Yes	Yes
DFN8	Sn (pure Tin)	Yes	Yes
TQFP and SO	NiPdAu (Nickel-palladium-Gold)	Yes	Yes

1. Assemblers must verify that the Pb-package maximum temperature (mentioned on the Inner box label) is compatible with their Lead-free soldering process.

8 Part numbering

Table 38. Ordering information scheme

Example: QST 1 08 K T 6

Device type

QST = Capacitive touch sensor

Device sub-family

1: QTouch (3 to 5 V)
5: QMatrix (3 to 5 V)
6: QSlide/QWheel (3 to 5 V)
11: QTouch (1.8 to 3.6 V)
15: QMatrix (1.8 to 3.6 V)
16: QSlide/QWheel (1.8 to 3.6 V)

Channel count

Number of channels

Pin count

A: 8 pins
Y: 16 pins
K: 32 pins
S: 44 pins
C: 48 pins
M: 80 pins

Package

B: DIP (dual in-line)
H: BGA (ball grid array)
M: SO (small outline)
N: TSSOP (thin-shrink small outline package)
T: LQFP (thin quad flat)
U: QFN (dual quad flat no lead)

Temperature range

0: +25°C
1: 0 to +70°C
5: –10°C to +85°C
6: –40°C to +85°C
7: –40°C to +105°C
9: –40°C to + 125°C

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

9 Device revision information

9.1 Device revision identification

The marking on the right side of the second line (Line B) of the package top face identifies the device revision.

Figure 25. Device revision identification (TQFP package)

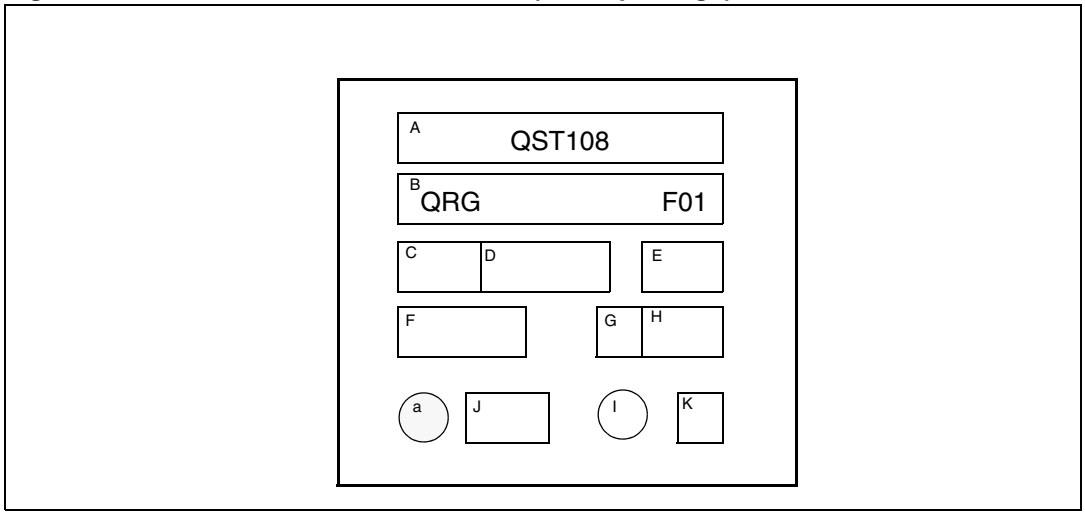


Table 39. Device revision identification

Marking	Device revision
F00	V 2.1
F01	V 2.3

The device revision can also be obtained using the GET_DEVICE_INFO I^2C command. For more information, refer to *Section 4.9: Supported commands on page 16*.

9.2 Device revision history

This section identifies the device deviations from the present specification for each device revision.

9.2.1 Revision 2.1

Engineering samples. For more information regarding this revision, please contact your local ST sales office.

9.2.2 Revision 2.3

- When the device enters Low Power mode, an additional sleep time is inserted after each burst, instead of once after every complete burst cycle. As a result, if only one burst is required, the sleep duration during Low Power mode is doubled. And if two bursts are required, the sleep duration is tripled.

  In Standalone mode, the 100ms sleep duration low power becomes either a 200ms or 300ms sleep duration depending on the number of bursts required.

  In I2C mode, it is required to program a sleep duration for one half or a third of the desired sleep duration depending on the number of bursts required.
- GET_PROTOCOL_VERSION returns 0x01 as I2CSpeed byte when it should return 0x00 (maximum speed is 100 kHz).
- If a command is sent with an incorrect parity bit, the device reports an unsupported command instead of a parity error.
- In I2C mode, it is recommended to set the fast positive recalibration threshold to 5 using the SET_SCKEY_PARAMETERS command in order to ensure a reliable behavior on low sensitivity keys.
- AKS should be always enabled in BCD mode. The AKS pull-up option resistor should be connected to pin KOUT2.

10 Revision history

Table 40. Document revision history

Date	Revision	Changes
8-Jun-2007	1	Initial release.
15-Jun-2007	2	Datasheet status changed to Preliminary Data.
26-Sep-2007	3	Removed Beeper function. Changed LED output pins to GPO pins. Updated pin names and functions in *Section 2: Pin description on page 5* and added *Figure 2: QTouch™ measuring circuitry on page 7*. Changed order of chapters in Section 3 for better comprehension. Removed Simplified independent output mode from *Section 4: Device operating modes on page 11*. Independent output mode renamed Stand-alone mode. Added *Section 4.2: Reset and power-up on page 11* and removed *Power supply option* chapter from *Section 4.4.2: Option descriptions on page 14*. Updated *Table 6: Max On-Duration (MOD) truth table on page 14* and *Table 7: Output mode (OM) truth table on page 15*. Updated *Figure 3: Stand-alone mode typical schematic on page 13* and *Figure 4: I2C mode typical schematic on page 16*. Updated *Table 9: I²C address versus option resistor on page 18*. Added *Figure 5: Optional LED schematic on page 17*. Updated *Section 4.5: I2C mode on page 15*. Added *Section 5.2.3: Key balance on page 25*. Updated *Section 6.4: Supply current characteristics on page 31*. Added *Section 6.5: Capacitive sensing characteristics on page 32*. and *Section 6.7: RESET pin on page 36*. Updated *Table 30: I²C characteristics on page 37*.
22-Nov-2007	4	Document status promoted from Preliminary Data to Datasheet. Added ECOPACK® information. Updated C_X value in *Figure 2: QTouch™ measuring circuitry on page 7*. Added Caution note in *Section 3.10: Drift compensation on page 11*. Added *Section 4.3: Low power mode on page 13*. Updated hex values in *Table 9: I²C address versus option resistor on page 21*. Updated *Table 28: Supply current characteristics on page 34*, *Table 30: Capacitive sensing parameters on page 35* and added *Figure 10: IDD Sleep mode current characteristics on page 34*. Added *Table 35: IRQ specific pin characteristics on page 40*. Added *Section 9: Device revision information on page 47*.

Table 40. Document revision history (continued)

Date	Revision	Changes
11-Jul-2008	5	Changed datasheet status to Not for new design. Updated *Figure 2: QTouch™ measuring circuitry* to add R_S sense resistor.* Updated *Section 3.5: Detection integrator filter on page 9* and added *Figure 3: Detection signals on page 10*. Added *Figure 4: Drift compensation example on page 12*. GET_KEY_ERROR and GET_KEY_STATE read values updated in *Table 10: Supported commands on page 21* and updated note 3. Updated bit values for *Key activation description on page 25*. Added *Section 6.3: EMC characteristics on page 32*. Updated *Table 30: Capacitive sensing parameters on page 35*. Added *Figure 24: 32-pin LQFP32 (7x7 mm) recommended footprint on page 44*. Added *Section 7.1: Soldering information on page 45*. Added *Section 9.2.2: Revision 2.3 on page 48*.

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