PRELIMINARY

FastEdge™ Series
CY2PP3115
1:15 Differential Fanout Buffer

Features

- **Fifteen ECL/PECL differential outputs grouped in four banks**
- **Two ECL/PECLdifferential inputs**
- **Hot-swappable/-insertable**
- **50-ps output-to-output skew**
- **< 200-ps device-to-device skew**
- **Less than 2-pS intrinsic jitter**
- **< 500-ps propagation delay (typical)**
- **Operation up to 1.5 GHz**
- **PECL mode supply range: V_{CC} = 2.375V to 3.465V with V_{EE} = 0V**
- **ECL mode supply range: V_{EE} = –2.375V to –3.465V with V_{CC} = 0V**
- **Industrial temperature range: –40°C to 85°C**
- **52-pin 1.4mm TQFP package**
- **Temperature compensation like 100K ECL**

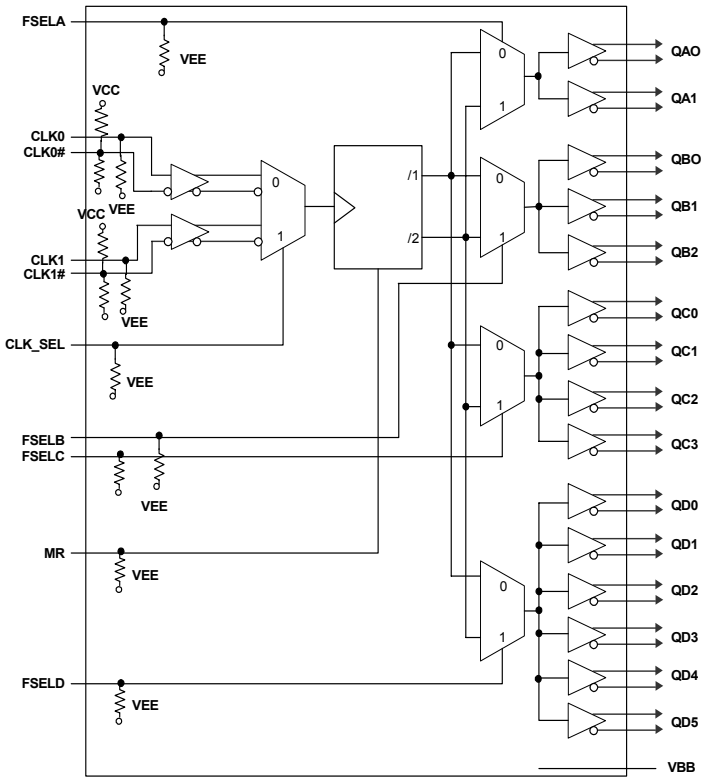
Description

The CY2PP3115 is a low-skew, low propagation delay 1-to-15 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on SiGe technology and has a fully differential internal architecture that is optimized to achieve low-signal skews at operating frequencies of up to 1.5 GHz.

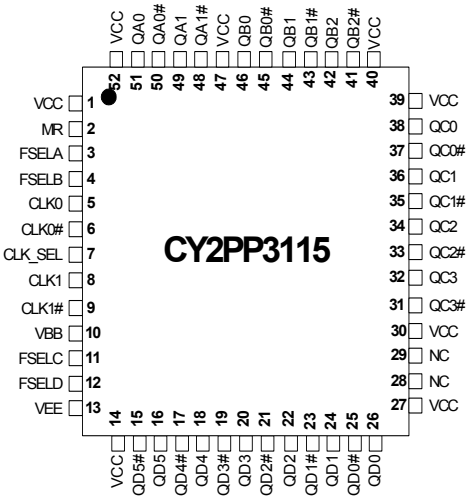
The device features two differential input paths which are multiplexed internally. This mux is controlled by the CLK_SEL pin. The CY2PP3115 may function not only as a differential clock buffer but also as a signal level translator and fanout on ECL/PECL single-ended signal to 15 ECL/PECL differential loads. An external bias pin, VBB, is provided for this purpose. In such an application, the VBB pin should be connected to either one of the CLKA# or CLKB# inputs and bypassed to V_{CC} via a 0.01-μF capacitor.

Since the CY2PP3115 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high frequency, high precision clocks across back-planes and boards in communication systems. Furthermore, advanced circuit design schemes, such as internal temperature compensation, ensure that the CY2PP3115 delivers consistent, guaranteed performance over differing platforms.

Block Diagram



Pin Configuration



Pin Description

Pin No.	Name[2,3]	I/O[1]	Type	Description
1,14,27, 30, 39, 40, 47, 52	VCC	+PWR	POWER	Power Supply, positive connection
2	MR	I,PD	ECL/PECL	Reset
3,4,11,12	FSEL(A,B,C,D)	I,PD	ECL/PECL	Output Divider Selects
5,8	CLK(0:1)	I,PD	ECL/PECL	Differential Clock Inputs – TRUE
6,9	CLK(0:1)#	I,PC	ECL/PECL	Differential Clock Inputs – COMPLIMENT
10	VBB	O	Bias	DC Bias Source
13	VEE	–PWR	POWER	Power Supply, Negative Connection
28,29	NC			No Connect. Pad Only
7	CLK_SEL	I,PD	ECL/PECL	Clock Input Select
26,24,22,20,18,16	QD(0:5)	O,OE	ECL/PECL	Bank D True Output
25,23,21,19,17,15	QD(0:5)#	O,OE	ECL/PECL	Bank D Compliment Output
38,36,34,32	QC(0:3)	O,OE	ECL/PECL	Bank C True Output
37,35,33,31	QC(0:3)#	O,OE	ECL/PECL	Bank C Compliment Output
46,44,42	QB(0:2)	O,OE	ECL/PECL	Bank B True Output
45,43,41	QB(0:2)#	O,OE	ECL/PECL	Bank B Compliment Output
51,49	QA(0:1)	O,OE	ECL/PECL	Bank A True Output
50,48	QA(0:1)#	O,OE	ECL/PECL	Bank A Compliment Output

Table 1. Function Table

Control Pin	0	1
FSELA (Asynchronous)	÷1	÷2
FSELB (Asynchronous)	÷1	÷2
FSELC (Asynchronous)	÷1	÷2
FSELD (Asynchronous)	÷1	÷2
CLK_SEL (Asynchronous)	CLK0	CLK1
MR (Asynchronous)	Active	Reset (QX = L and QX# = H)

Governing Agencies

The following agencies provide specifications that apply to the CY2PP3115. The agency name and relevant specification is listed below.

Agency Name	Specification
JEDEC	JESD 51 (Theta JA) JESD 8–2 (ECL) JESD 65–A (skew,jitter)
IEEE	1596.3 (Jitter specs)
UL	94 (Flammability Grading)
Mil–Spec	883E Method 1012.1 (Thermal Theta JC)

Notes:

1. In the I/O column, the following notation is used: I for Input, O for Output, PD for Pull-down, PU for Pull-up, PC for Pull Center, O for output, OE for open emitter and PWR for Power.
2. In ECL mode (negative power supply mode), V_{EE} is either –3.3V or –2.5V and V_{CC} is connected to GND (0V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}) and are between VCC and VEE.
3. V_{BB} is available for use for single ended bias mode when V_{CC} is +3.3V.

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Supply Voltage	Non-Functional	–0.3	4.6	VDC
V_{CC}	Operating Voltage	Functional	2.5 – 5%	3.3 + 5%	VDC
V_{BB}	Output Reference Voltage	Relative to V_{CC}	V_{CC}–1.620	Vcc–1.220	VDC
I_{BB}	Output Reference Current	Relative to V_{BB}		200	uA
VTT	Output Termination Voltage	Relative to V_{CC}		V_{CC}–2	VDC
V_{IN}	Input Voltage	Relative to V_{CC}	–0.3	V_{CC}+0.3	VDC
V_{OUT}	Output Voltage	Relative to V_{CC}	–0.3	V_{CC}+0.3	VDC
LU_I	Latch-up Immunity	Functional	300		mA
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
$Ø_{Jc}$	Dissipation, Junction to Case	Functional	40	60	°C/W
$Ø_{Ja}$	Dissipation, Junction to Ambient	Functional	40	100	°C/W
ESD_h	ESD Protection (Human Body Model)		2000		V
M_{SL}	Moisture Sensitivity Level		3		N.A.
G_{ATES}	Total Functional Gate Count	Assembled Die	50		Ea.
UL–FLM	Flammability Rating	@ 1/8 in.	V–0		N.A.

PECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Control (FSEL(A,B,C),CLK_SEL, MR and FSELD) (PECL Single-ended)					
$V_{CC2.5V}$	2.5 Operating Voltage	2.5V ± 5%, V_{EE} = 0.0V	2.375	2.625	V
$V_{CC3.3V}$	3.3 Operating Voltage	3.3V ± 5%, V_{EE} = 0.0V	3.135	3.465	V
V_{IL}	Input Voltage, Low		V_{CC}–1.945	V_{CC}–1.625	V
V_{IH}	Input Voltage, High		V_{CC}–1.165	V_{CC}–0.880	V
I_{IN}	Input Current[4]	V_{IL} = V_{IL}min. or V_{IH} = V_{IH}max at V_{CC} = 3.6V		I150I	uA
Clock input pair CLK0, CLK0#,CLK1,CLK1# (PECL Differential Signals)					
V_{PP}	Differential input voltage[5]	Differential operation	0.1	1.3	V
V_{CMR}	Differential cross point voltage[6]	Differential operation	1.2	V_{CC}	V
I_{IN}	Input Current[4]	V_{IL} = V_{IL}min. or V_{IH} = V_{IH}max at V_{CC} = 3.6V		I150I	uA
PECL Outputs QA((0:1),#),QB((0:2),#),QC((0:3),#),QD((0:5),#)(PECL Differential Signals)					
V_{OH}	Output High Voltage	I_{OH} = –30 mA[7]	V_{CC}–1.2	V_{CC}–0.7	V
V_{OL}	Output Low Voltage V_{CC} = 3.3V ± 5%, V_{CC} = 2.5V ± 5%	I_{OL} = –5 ma[7]	V_{CC}–1.945 V_{CC} –1.945	V_{CC}–1.5 V_{CC}–1.3	V
Supply Current and VBB					
I_{EE}	Maximum Quiescent Supply Current without output termination current[8]	V_{EE} pin	–	200	mA
V_{BB}[9]	Output reference voltage	I_{BB} = 200 uA[12]	V_{CC}–1.620	V_{CC}–1.220	V
C_{IN}	Input pin capacitance		–	2.0	pF
L_{IN}	Pin Inductance		–	1.0	nH

Notes:

4. Input have internal pull-up/pull-down or biasing resistors which affect the input current.
5. VPP (DC) is the minimum differential input voltage swing required to maintain device functionality.
6. VCMR (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the VCMR (DC) range and the input swing lies within the VPP (DC) specification.
7. Equivalent to a termination of 50 Ω to VTT.
8. ICC Calculation: ICC = (number of differential output pairs used) x (I_{OH} + I_{OL}) + I_{EE} orI_{CC} = (number of differential output pairs used) x (V_{OH}–VTT)/Rload + (V_{OL}–-VTT)/Rload +IEE.
9. VBB is limited to VCC of 3.3V only. See note 17.

ECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Control (FSEL(A,B,C),CLK_SEL, MR and FSELD) (ECL single-ended)					
$V_{EE2.5}$	–2.5 Negative Power Supply	–2.5V ± 5%, V_{EE} = 0.0V	–2.375	–2.625	V
$V_{EE3.3}$	–3.3 Negative Power Supply	–3.3V ± 5%, V_{EE} = 0.0V	–33.135	–3.465	V
V_{IL}	Input Voltage, Low		–1.945	–1.625	V
V_{IH}	Input Voltage, High		–1.165	–0.880	V
I_{IN}	Input Current[10]	V_{IN} = V_{IL} or V_{IN} = V_{IH}		I150I	uA
Clock input pair CLK0, CLK0#,CLK1,CLK1# (ECL differential signals)					
V_{PP}	Differential input voltage[11]	Differential operation	0.1	1.3	V
V_{CMR}	Differential cross point voltage[12]	Differential operation	V_{EE}+1.2	–0.5	V
I_{IN}	Input Current[10]	V_{IN} = V_{IL} or V_{IN} = V_{IH}		I150I	uA
ECL Outputs QA((0:1),#),QB((0:2),#),QC((0:3),#),QD((0:5),#)(ECL differential signals)					
V_{OH}	Output High Voltage	I_{OH} = –30 mA[13]	–1.2	–0.7	V
V_{OL}	Output Low Voltage V_{EE} = –3.3V ± 5%,V_{EE} = –2.5V ± 5%	I_{OL} = –5 ma[13]	–1.945 –1.945	–1.5 –1.3	V
Supply current and VBB					
I_{EE}	Maximum Quiescent Supply Current without output termination current[14]	V_{EE} pin	–	180	mA
V_{BB}	Output reference voltage	I_{BB} = 200 uA	–1.620	–1.220	V

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Clock input pair CLK0, CLK0#,CLK1,CLK1#(PECL or ECL differential signals)					
V_{PP}	Differential input voltage[16]	Differential operation	0.1	1.3	V
V_{CMR}	Differential cross point voltage[17]	Differential operation	V_{EE} + 1.2	0	V
F_{CLK}	Input Frequency[18]	50% duty cycle Standard load		1500	MHz
T_{PD}	Propagation Delay CLK0 or CLK1 to QA(0:1),QB(0:2),QC(0:3),QD(0:5) pair	660 MHz 50% duty cycle Standard load Differential Operation. See *Table 2*	600	1200	ps
ECL/PECL Clock Outputs QA((0:1),#),QB((0:2),#),QC((0:3),#),QD((0:5),#) (differential)					
$Vo_{(P-P)}$	Differential output voltage (peak-to-peak)	Differential PRBS fo < 50 MHz fo < 0.8 GHz fo < 1.0 GHz fo < 1.5 GHz	 0.45 0.4 0.375 0.3		V
VMCR	Common Voltage Range		V_{CC}–1.425		ps
$tsk_{(O)}$	Output-to-output skew	660 MHz 50% duty cycle Standard load Differential Operation	–	50	ps
$tsk_{(O)}$	Output-to-output skew (different frequency)	660 MHz 50% duty cycle Standard load Differential Operation	–	60	ps

Notes:

10. Input have internal pullup / pulldown or biasing resistors which affect the input current.
11. VPP (DC) is the minimum differential input voltage swing required to maintain device functionality.
12. VCMR (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the VCMR (DC) range and the input swing lies within the VPP (DC) specification.
13. Equivalent to a termination of 50 Ω to VTT.
14. I_{CC} Calculation: ICC = (number of differential output pairs used) x (I_{OH} + I_{OL}) + IEE or I_{CC} = (number of differential output pairs used) x (V_{OH} –VTT)/Rload + (V_{OL} –VTT)/Rload +I_{EE}.
15. AC characteristics apply for parallel output termination of 50 Ω to VTT.
16. VPP (AC) is the minimum differential ECL/PECL input swing required to maintain AC characteristics including tpd and device-to-device skew.
17. VCMR (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the VCMR(AC) range and the input swing lies within the VPP(AC) specification. Violation of VCMR(AC) or VPP(AC) impacts the device propagation delay, device and part-to-part skew.
18. The CY2PP3115 is fully operation up to 1.5 GHz.

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
$tsk_{(PP)}$	Output-to-output skew (part-to-part)	50% duty cycle Standard load Differential Operation	–	200	ps
$T_{JIT(CC)}$	Output cycle-to-cycle jitter (deterministic/Intrinsic) All outputs /1	500 MHz 50% duty cycle Standard load Differential Operation	–	2	ps
	Output cycle-to-cycle jitter (deterministic/Intrinsic) All outputs /2	660 MHz 50% duty cycle Standard load Differential Operation	–	2	ps
	Output cycle-to-cycle jitter (deterministic/Intrinsic) All outputs Bank(A and C)/1, Bank(B and D)/2	660 MHz 50% duty cycle Standard load Differential Operation	–	2	ps
	Output cycle-to-cycle jitter (deterministic/Intrinsic) All outputs Bank A/1, Bank(B,C and D)/2	660 MHz 50% duty cycle Standard load Differential Operation	–	2	ps
$tsk_{(P)}$	Output pulse skew [19]	660 MHz 50% duty cycle Standard load Differential Operation	–	75	ps
T_R,T_F	Output Rise / Fall time	660 MHz 50% duty cycle Differential 20% to 80%	–	0.3	ns
TTB	Total Timing Budget	500 MHz 50% duty cycle Standard load	–	250	ps

Table 2. TPD–Propagation Delay 66-MHz 50% Duty Cycle

TPD		CLK_SEL		Unit
		0	1	
FSELA	0	0.900	0.974	ns
	1	0.979	0.982	ns
FSELB	0	0.951	0.974	ns
	1	0.962	0.966	ns
FSELC	0	0.952	0.974	ns
	1	1.019	1.021	ns
FSELD	0	0.986	0.980	ns
	1	1.018	1.022	ns

Timing Definitions

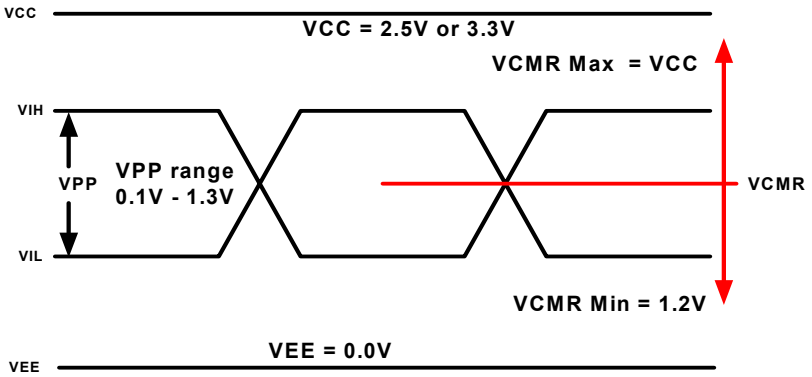


Figure 1. PECL Waveform Definitions

Note:
19. Output pulse skew is the absolute difference of the propagation delay times: | tPLH – tPHL |.

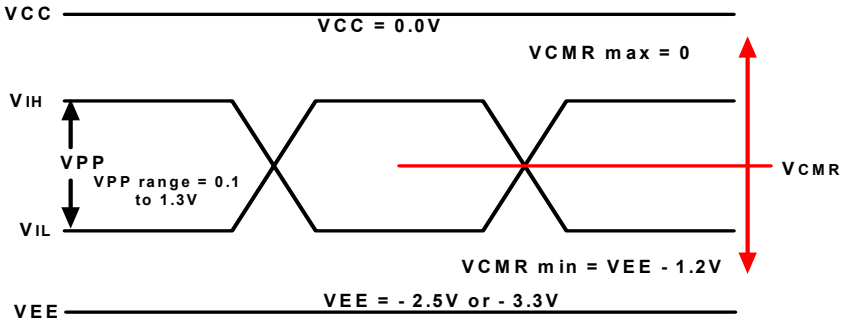


Figure 2. ECL Differential Waveform Definitions

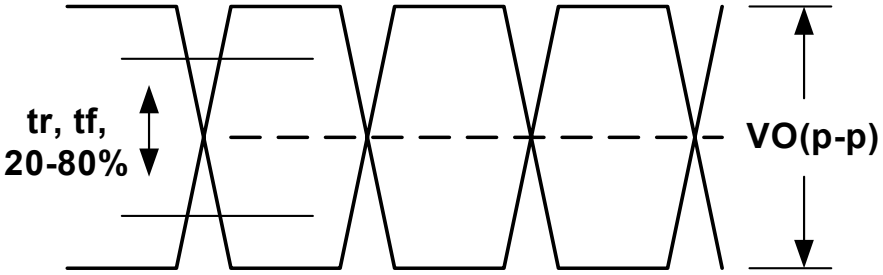


Figure 3. ECL/LVPECL Output

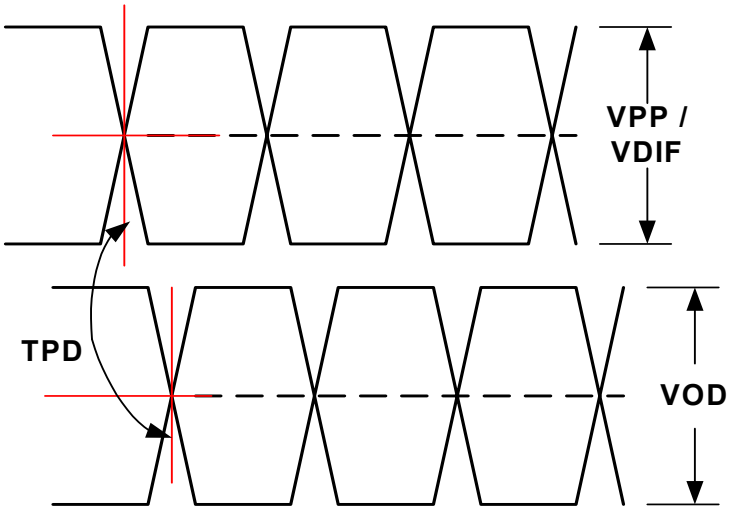
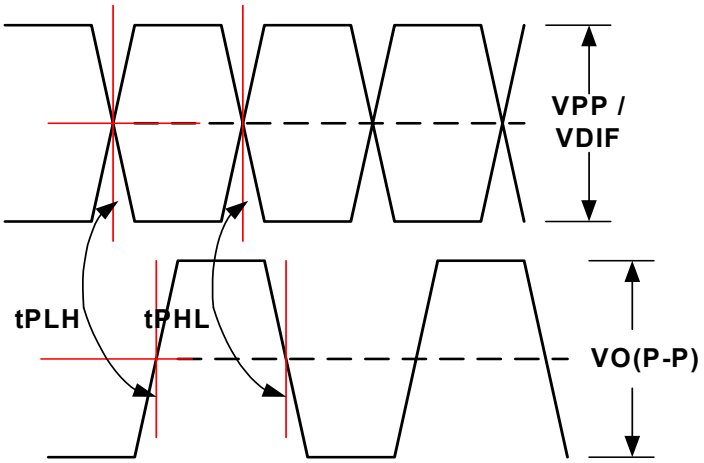


Figure 4. TPD Propagation Delay of Both CLKA or CLKB to Q0–Q9 Pair PECL/ECL to PECL/ECL



tsk(P) Output pulse skew
= | tPLH - tPHL |

Figure 5. Output Pulse Skew

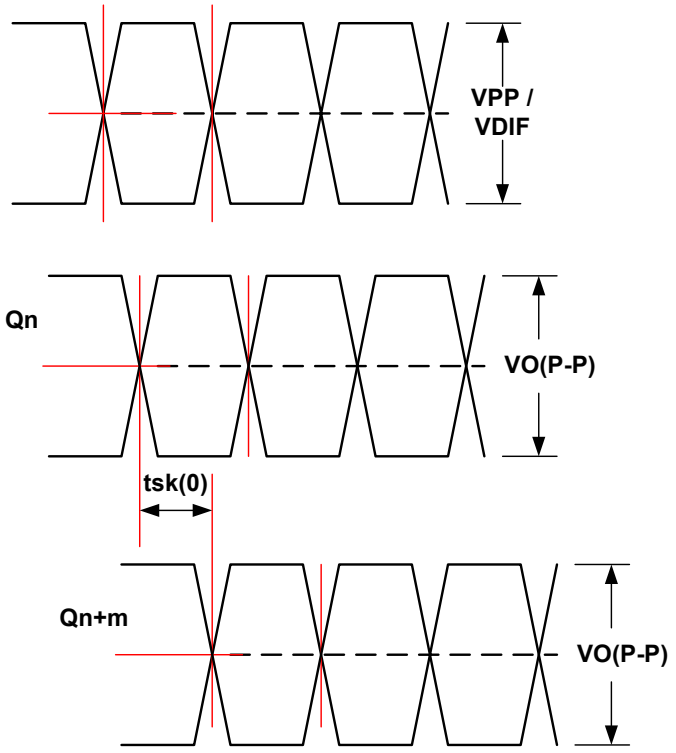


Figure 6. Output-to-output Skew

Test Configurations

Standard test load using a differential pulse generator and differential measurement instrument.

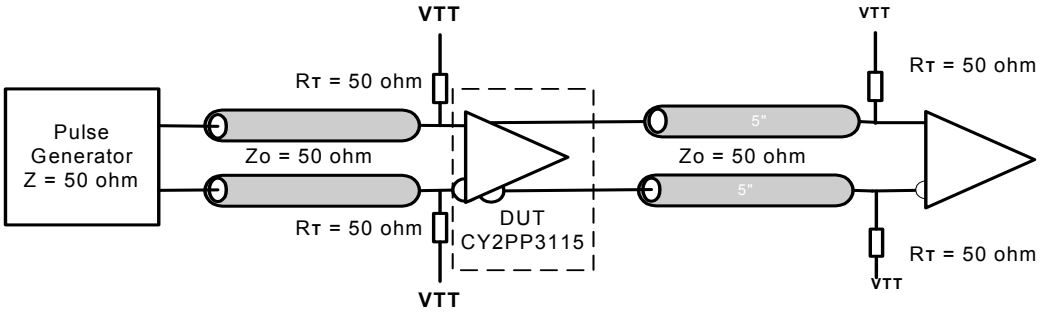


Figure 7. CY2PP3115 AC Test Reference

Applications Information

Termination Examples

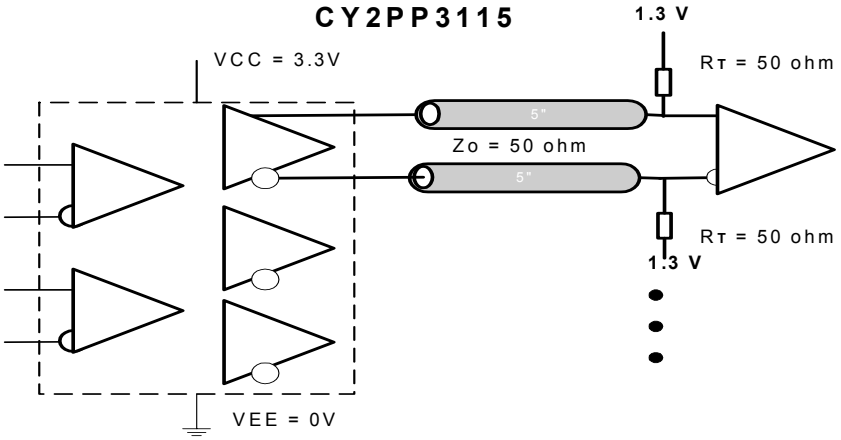


Figure 8. Standard LVPECL – PECL Output Termination

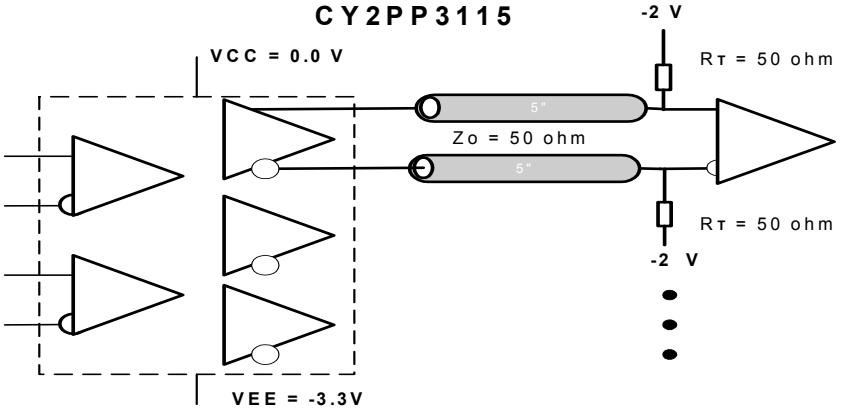


Figure 9. Standard ECL Output Termination

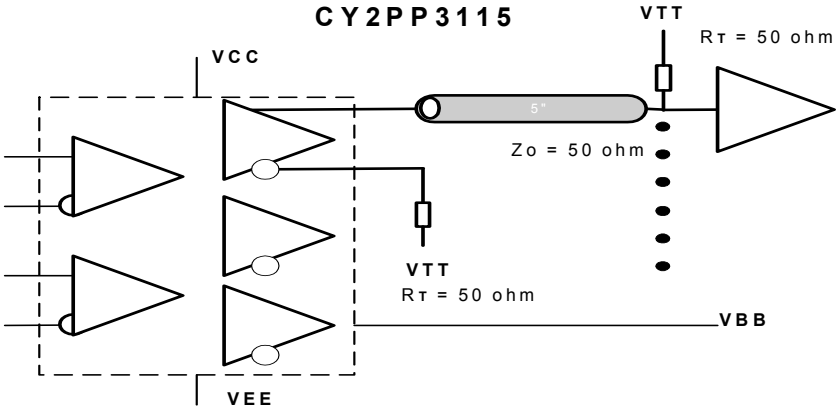


Figure 10. Driving a PECL/ECL Single-ended Input

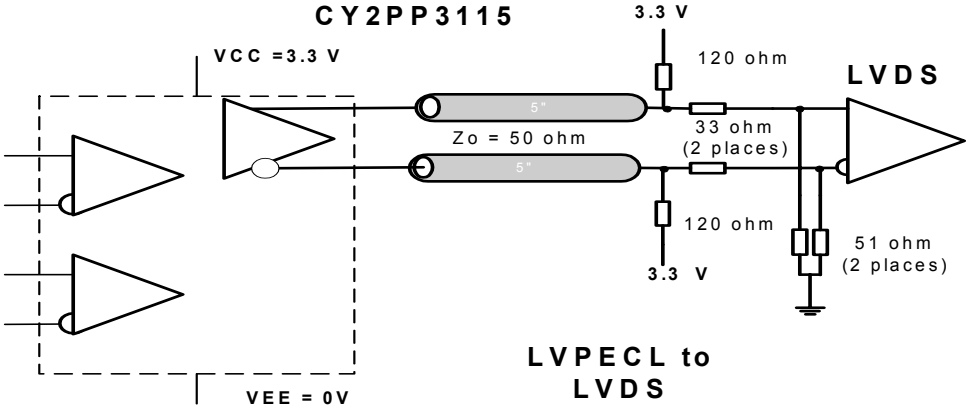


Figure 11. Low-voltage Positive Emitter-Coupled Logic (LVPECL) to a Low-voltage Differential Signaling (LVDS) Interface

Evaluation Material

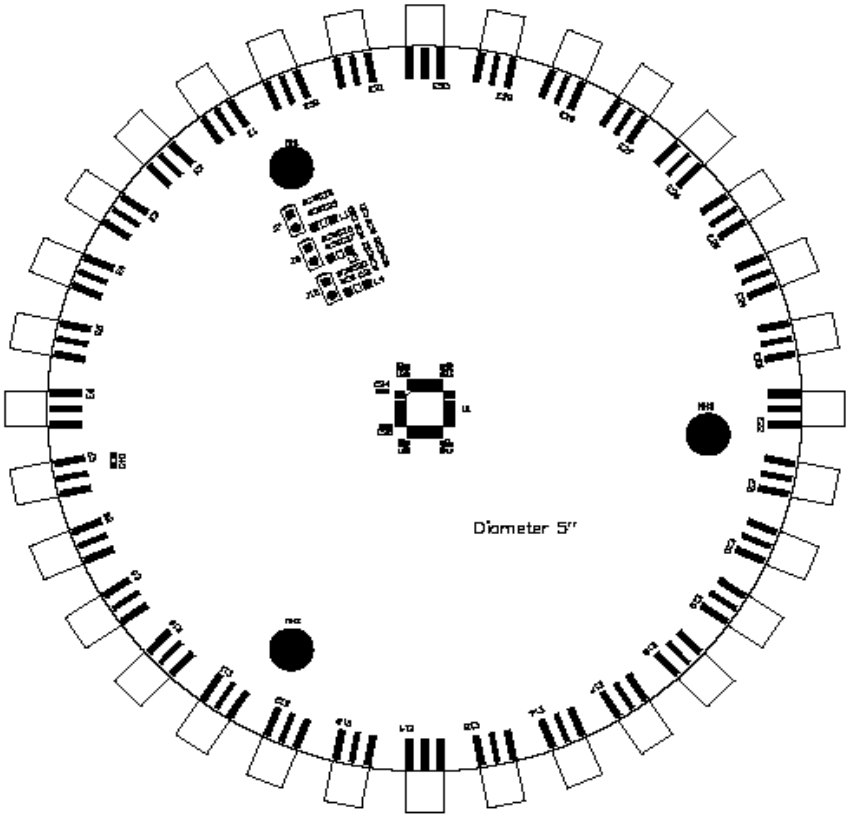
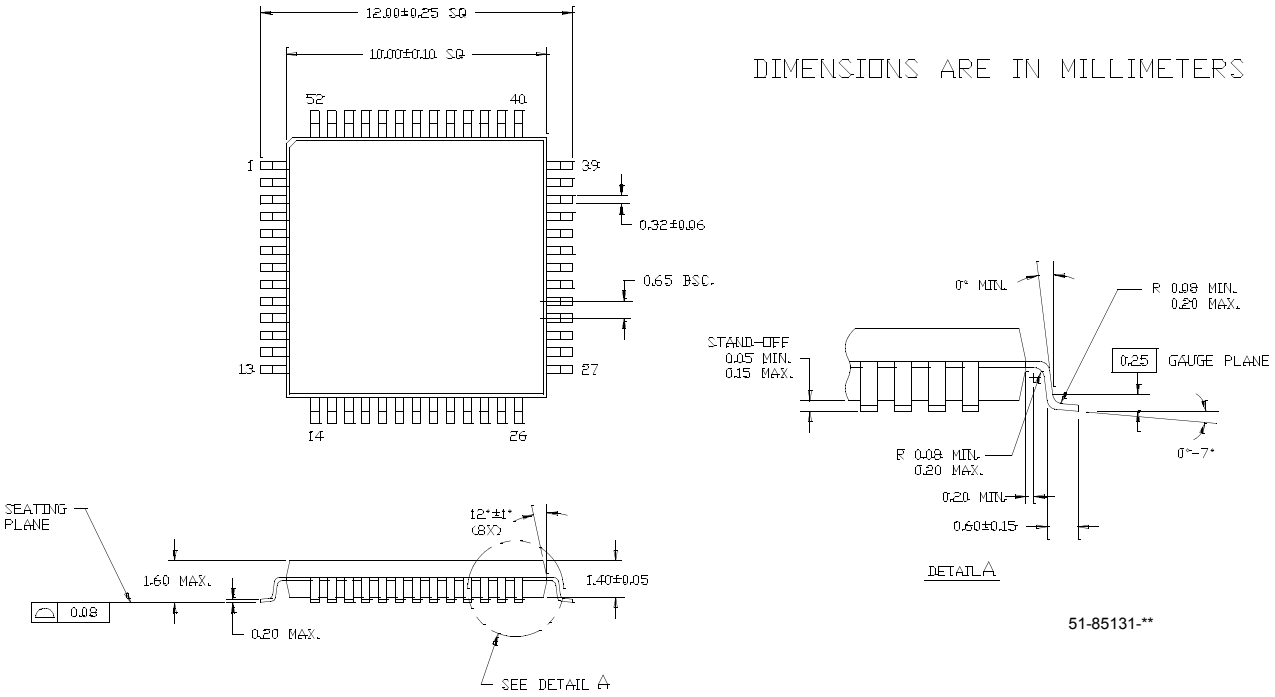


Figure 12. Demonstration PCB

Part Number	Package Type	Product Flow
CY2PP3115AI	52-Pin TQFP	Industrial, –40° to 85°C
CY2PP3115AIT	52-Pin TQFP – Tape and Reel	Industrial, –40° to 85°C

Package Drawing and Dimensions

52-lead Thin Plastic Quad Flat Pack (10 x 10 x 1.4 mm) A52



Document History Page

Document Title: CY2PP3115 FastEdge™ Series 1:15 Differential Fanout Buffer Document Number: 38-07502				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	122042	02/12/03	RGL	New Data Sheet
*A	131090	11/21/03	RGL	Supplied numbers for all specs with TBD after characterization