

Integrated Silicon Pressure Sensor On-Chip Signal Conditioned, Temperature Compensated and Calibrated

The MPXV7002 series piezoresistive transducers are state-of-the-art monolithic silicon pressure sensors designed for a wide range of applications, but particularly those employing a microcontroller or microprocessor with A/D inputs. This transducer combines advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure.

Features

- 2.5% Typical Error over +10°C to +60°C with Auto Zero
- 6.25% Maximum Error over +10°C to +60°C without Auto Zero
- Ideally Suited for Microprocessor or Microcontroller-Based Systems
- Thermoplastic (PPS) Surface Mount Package
- Temperature Compensated over +10° to +60°C
- Patented Silicon Shear Stress Strain Gauge
- Available in Differential and Gauge Configurations

Typical Applications

- Hospital Beds
- HVAC
- Respiratory Systems
- Process Control

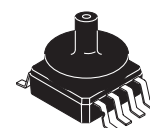
ORDERING INFORMATION

Device Type	Options	Case No.	MPX Series Order No.	Packing Options	Device Marking
SMALL OUTLINE PACKAGE (MPXV7002 SERIES)					
Ported Elements	Gauge, Axial Port, SMT	482A	MPXV7002GC6U	Rails	MPXV7002G
	Gauge, Axial Port, SMT	482A	MPXV7002GC6T1	Tape & Reel	MPXV7002G
	Gauge, Side Port, SMT	1369	MPXV7002GP	Trays	MPXV7002G
	Differential, Dual Port, SMT	1351	MPXV7002DP	Trays	MPXV7002G
	Differential, Dual Port, SMT	1351	MPXV7002DPT1	Tape & Reel	MPXV7002G

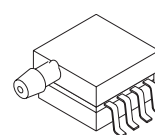
MPXV7002 SERIES

**INTEGRATED
PRESSURE SENSOR**
-2 to 2 kPa (-0.3 to 0.3 psi)
0.5 to 4.5 V OUTPUT

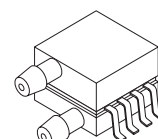
SMALL OUTLINE PACKAGE



**MPXV7002GC6U
CASE 482A-01**



**MPXV7002GP
CASE 1369-01**



**MPXV7002DP
CASE 1351-01**

SMALL OUTLINE PACKAGE PIN NUMBERS⁽¹⁾

1	N/C	5	N/C
2	V _S	6	N/C
3	Gnd	7	N/C
4	V _{out}	8	N/C

1. Pins 1, 5, 6, 7, and 8 are internal device connections. Do not connect to external circuitry or ground. Pin 1 is noted by the notch in the lead.

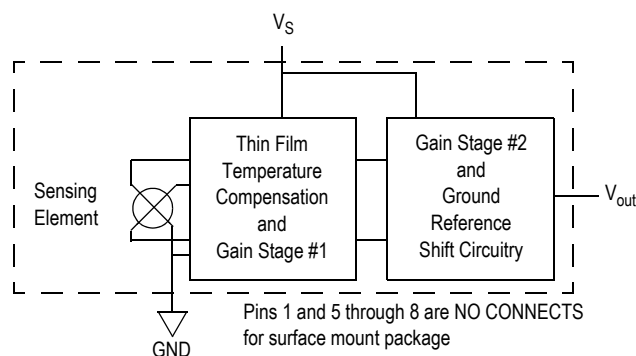


Figure 1. Fully Integrated Pressure Sensor Schematic

Table 1. Maximum Ratings⁽¹⁾

Rating	Symbol	Value	Unit
Maximum Pressure (P1 > P2)	P _{max}	8.0	kPa
Storage Temperature	T _{stg}	-30 to +100	°C
Operating Temperature	T _A	10 to +60	°C

1. Exposure beyond the specified limits may cause permanent damage or degradation to the device.

Table 2. Operating Characteristics (V_S = 5.0 Vdc, T_A = 25°C unless otherwise noted. Decoupling circuit shown in Figure 3 required to meet specification.)

Characteristic	Symbol	Min	Typ	Max	Unit
Pressure Range ⁽¹⁾	P _{OP}	-2.0	—	2.0	kPa
Supply Voltage ⁽²⁾	V _S	4.75	5.0	5.25	Vdc
Supply Current	I _o	—	—	10	mAdc
Pressure Offset ⁽³⁾ @ V _S = 5.0 Volts	V _{off}	2.25	2.5	2.75	Vdc
Full Scale Output ⁽⁴⁾ @ V _S = 5.0 Volts	V _{FSO}	4.25	4.5	4.75	Vdc
Full Scale Span ⁽⁵⁾ @ V _S = 5.0 Volts	V _{FSS}	3.5	4.0	4.5 V	Vdc
Accuracy ⁽⁶⁾	—	—	±2.5 ⁽⁷⁾	±6.25	%V _{FSS}
Sensitivity	V/P	—	1.0	—	V/kPa
Response Time ⁽⁸⁾	t _R	—	1.0	—	ms
Output Source Current at Full Scale Output	I _{O+}	—	0.1	—	mAdc
Warm-Up Time ⁽⁹⁾	—	—	20	—	ms

1. 1.0 kPa (kiloPascal) equals 0.145 psi.
2. Device is ratiometric within this specified excitation range.
3. Offset (V_{off}) is defined as the output voltage at the minimum rated pressure.
4. Full Scale Output (V_{FSO}) is defined as the output voltage at the maximum or full rated pressure.
5. Full Scale Span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.
6. Accuracy (error budget) consists of the following:
 - Linearity: Output deviation from a straight line relationship with pressure over the specified pressure range.
 - Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to and from the minimum or maximum operating temperature points, with zero differential pressure applied.
 - Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from the minimum or maximum rated pressure, at 25°C.
 - TcSpan: Output deviation over the temperature range of 10° to 60°C, relative to 25°C.
 - TcOffset: Output deviation with minimum rated pressure applied, over the temperature range of 10° to 60°C, relative to 25°C.
 - Variation from Nominal: The variation from nominal values, for Offset or Full Scale Span, as a percent of V_{FSS}, at 25°C.
7. Auto Zero at Factory Installation: Due to the sensitivity of the MPXV7002 Series, external mechanical stresses and mounting position can affect the zero pressure output reading. Autozero is defined as storing the zero pressure output reading and subtracting this from the device's output during normal operations. Reference AN1636 for specific information. The specified accuracy assumes a maximum temperature change of ± 5°C between autozero and measurement.
8. Response Time is defined as the time for the incremental change in the output to go from 10% to 90% of its final value when subjected to a specified step change in pressure.
9. Warm-up Time is defined as the time required for the product to meet the specified output voltage after the Pressure has been stabilized.

ON-CHIP TEMPERATURE COMPENSATION, CALIBRATION AND SIGNAL CONDITIONING

The performance over temperature is achieved by integrating the shear-stress strain gauge, temperature compensation, calibration and signal conditioning circuitry onto a single monolithic chip.

Figure 2 illustrates the Differential or Gauge configuration in the basic chip carrier (Case 482). A gel die coat isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the sensor diaphragm.

The MPXV7002 series pressure sensor operating characteristics, and internal reliability and qualification tests are based on use of dry air as the pressure media. Media, other than dry air, may have adverse effects on sensor

performance and long-term reliability. Contact the factory for information regarding media compatibility in your application.

Figure 3 shows the recommended decoupling circuit for interfacing the integrated sensor to the A/D input of a microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

Figure 4 shows the sensor output signal relative to pressure input. Typical, minimum, and maximum output curves are shown for operation over a temperature range of 10° to 60°C using the decoupling circuit shown in Figure 3. The output will saturate outside of the specified pressure range.

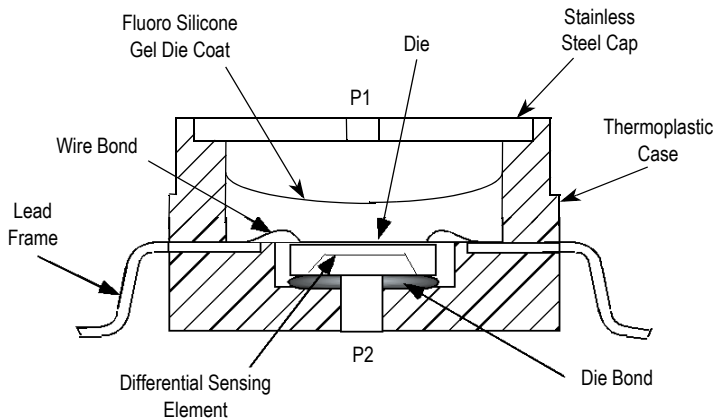


Figure 2. Cross-Sectional Diagram SOP (not to scale)

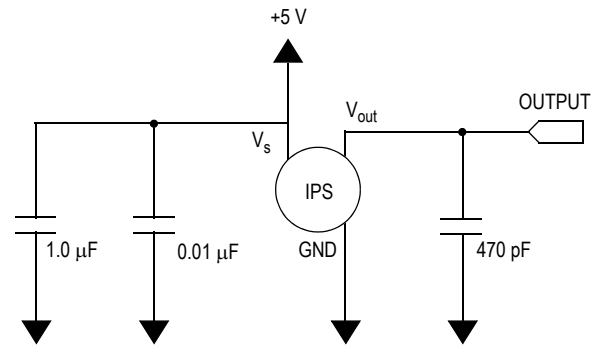


Figure 3. Recommended Power Supply Decoupling and Output Filtering
(For additional output filtering, please refer to Application Note AN1646.)

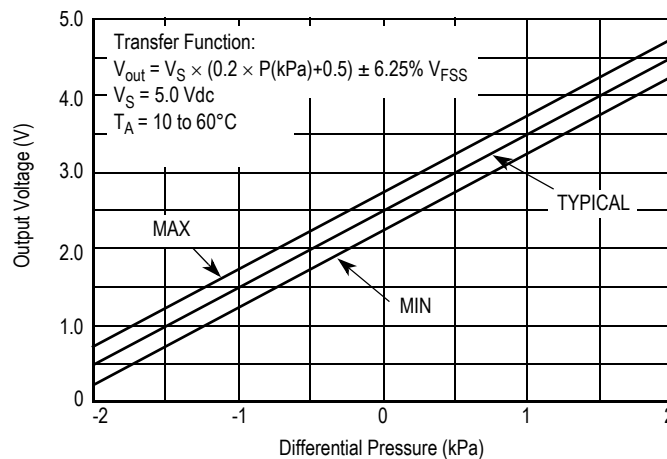


Figure 4. Output versus Pressure Differential

PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE

Freescale designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing a gel die coat which protects the die from harsh media.

The Pressure (P1) side may be identified by using the table below:

Part Number	Case Type	Pressure (P1) Side Identifier
MPXV7002GC6U/GC6T1	482A-01	Vertical Port Attached
MPXV7002GP	1369-01	Side with Port Attached
MPXV7002DP	1351-01	Side with Dual Port Attached

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct

footprint, the packages will self align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

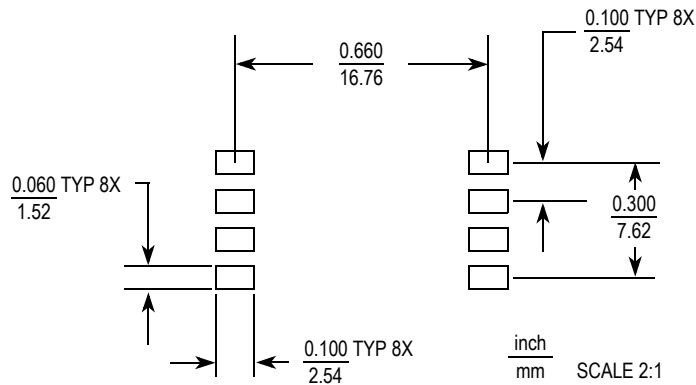
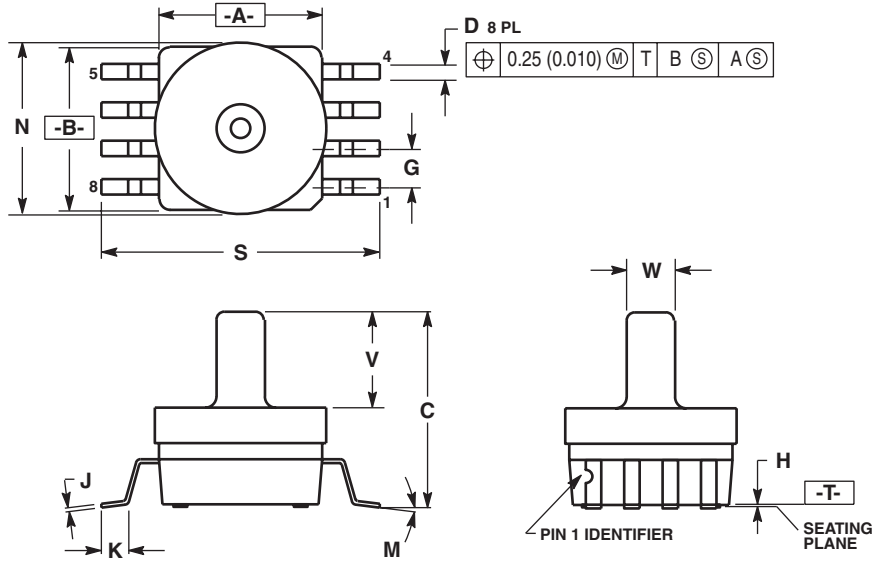


Figure 5. Small Outline Package Footprint

PACKAGE DIMENSIONS

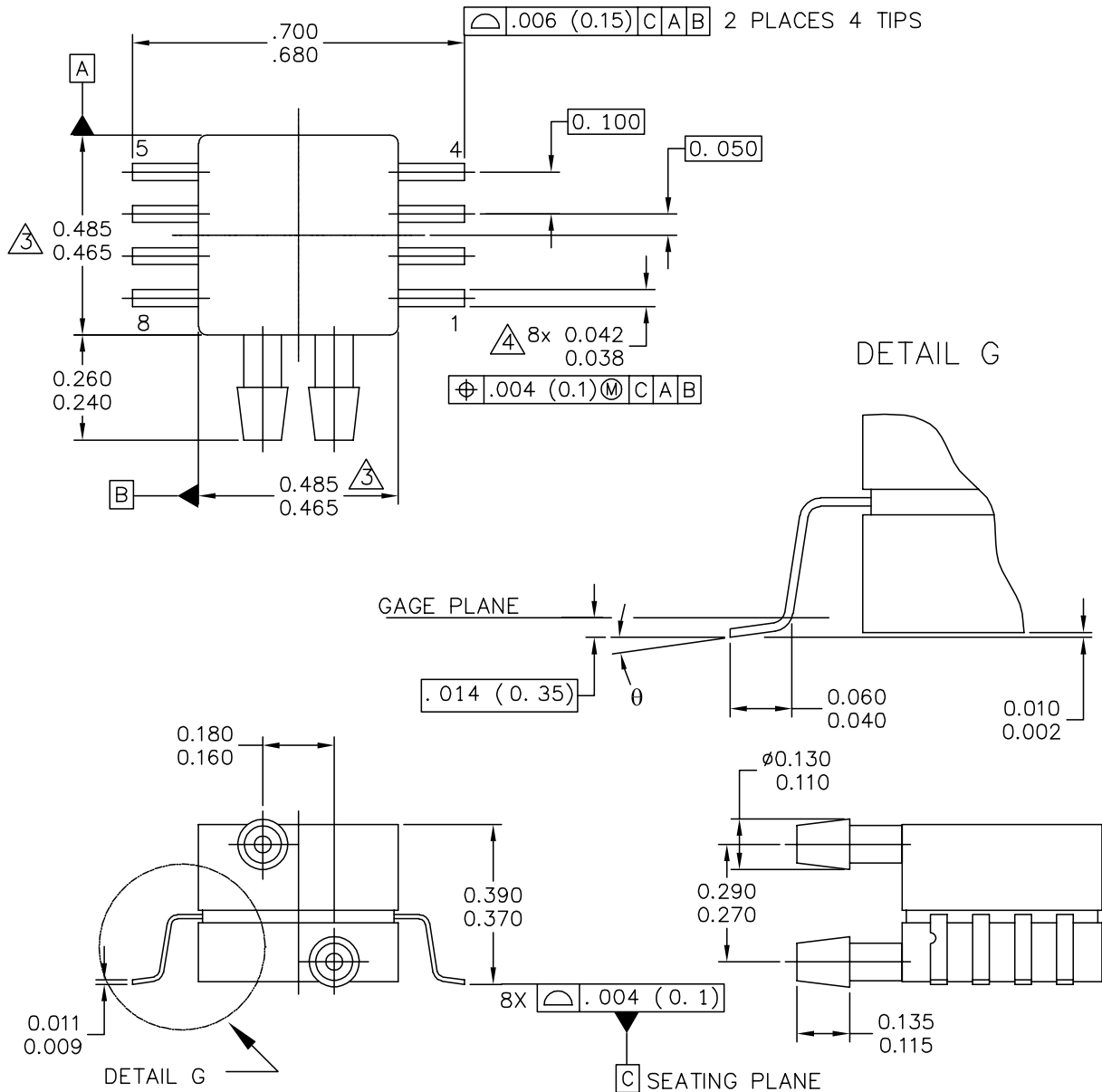


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
 5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.415	0.425	10.54	10.79
B	0.415	0.425	10.54	10.79
C	0.500	0.520	12.70	13.21
D	0.038	0.042	0.96	1.07
G	0.100 BSC		2.54 BSC	
H	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0"	7"	0"	7"
N	0.444	0.448	11.28	11.38
S	0.709	0.725	18.01	18.41
V	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

CASE 482A-01 ISSUE A SMALL OUTLINE PACKAGE

PACKAGE DIMENSIONS



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TITLE: 8 LD SNSR, DUAL PORT	DOCUMENT NO: 98ASA99255D		REV: A
	CASE NUMBER: 1351-01		27 JUL 2005
	STANDARD: NON-JEDEC		

PAGE 1 OF 2

**CASE 1351-01
ISSUE A
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE.

4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL BE .008 MAXIMUM.

STYLE 1:

PIN 1: GND
PIN 2: +V_{out}
PIN 3: V_s
PIN 4: -V_{out}
PIN 5: N/C
PIN 6: N/C
PIN 7: N/C
PIN 8: N/C

STYLE 2:

PIN 1: N/C
PIN 2: V_s
PIN 3: GND
PIN 4: V_{out}
PIN 5: N/C
PIN 6: N/C
PIN 7: N/C
PIN 8: N/C

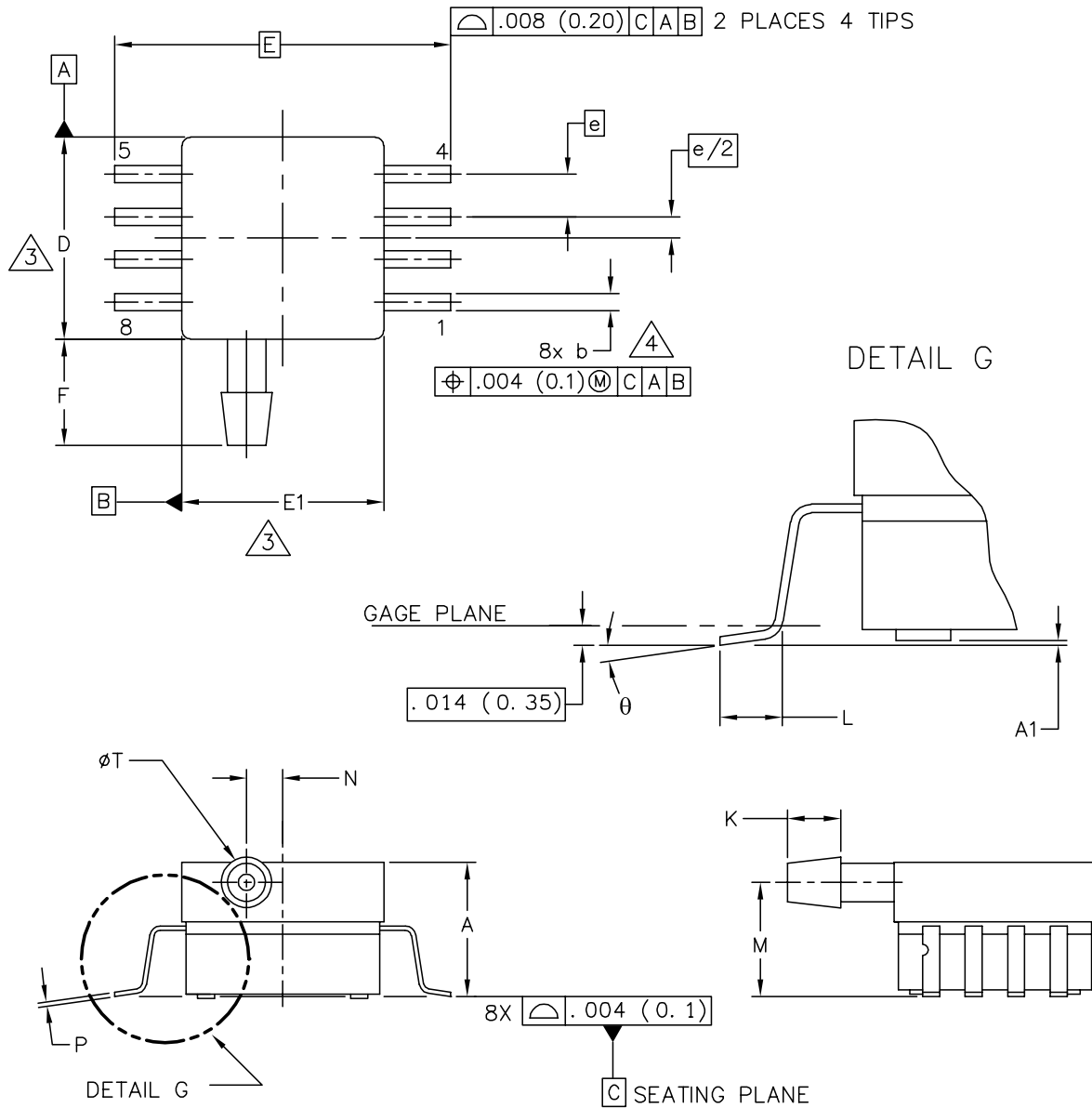
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**CASE 1351-01
ISSUE A
SMALL OUTLINE PACKAGE**

MPXV7002

PACKAGE DIMENSIONS



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TITLE: 8 LD SOP, SIDE PORT	DOCUMENT NO: 98ASA99303D	REV: B
	CASE NUMBER: 1369-01	24 MAY 2005
	STANDARD: NON-JEDEC	

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**CASE 1369-01
ISSUE B
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

③ DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 (0.152) PER SIDE.

④ DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 (0.203) MAXIMUM.

INCHES			MILLIMETERS		DIM	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.300	.330	7.11	7.62	θ	0°	7°	0°	7°
A1	.002	.010	0.05	0.25	—	---	---	---	---
b	.038	.042	0.96	1.07	—	---	---	---	---
D	.465	.485	11.81	12.32	—	---	---	---	---
E	.717 BSC		18.21 BSC		—	---	---	---	---
E1	.465	.485	11.81	12.32	—	---	---	---	---
e	.100 BSC		2.54 BSC		—	---	---	---	---
F	.245	.255	6.22	6.47	—	---	---	---	---
K	.120	.130	3.05	3.30	—	---	---	---	---
L	.061	.071	1.55	1.80	—	---	---	---	---
M	.270	.290	6.86	7.36	—	---	---	---	---
N	.080	.090	2.03	2.28	—	---	---	---	---
P	.009	.011	0.23	0.28	—	---	---	---	---
T	.115	.125	2.92	3.17	—	---	---	---	---
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TITLE: 8 LD SOP, SIDE PORT					DOCUMENT NO: 98ASA99303D			REV: B	
					CASE NUMBER: 1369-01			24 MAY 2005	
					STANDARD: NON-JEDEC				

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**CASE 1369-01
ISSUE B
SMALL OUTLINE PACKAGE**

MPXV7002

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