IXYS

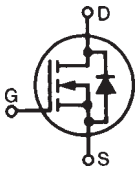
PolarHT™ HiPerFET Power MOSFET ISOPLUS220™

(Electrically Isolated Back Surface)

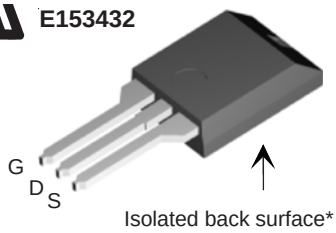
IXFC 96N15P

V_{DSS}	=	150	V
I_{D25}	=	42	A
$R_{DS(on)}$	=	26	mΩ
t_{rr}	<	200	ns

N-Channel Enhancement Mode
Fast Recovery Diode, Avalanche Rated



ISOPLUS 220™
E153432



Isolated back surface*

G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 175°C	150	V
V_{DGR}	T_J = 25°C to 175°C; R_{GS} = 1 MΩ	150	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	42	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	250	A
I_{AR}	T_C = 25°C	60	A
E_{AR}	T_C = 25°C	40	mJ
E_{AS}	T_C = 25°C	1.0	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/μs, $V_{DD} \le V_{DSS}$, $T_J \le 175°C$, R_G = 4 Ω	10	V/ns
P_D	T_C = 25°C	120	W
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
F_C	Mounting force	11...65/2.4...11	N/lb
V_{ISOL}	50/60 Hz, 1 minute	2500	~V
Weight		3	g

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	150			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4 mA	3.0		5.0	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0 V			25	μA
	T_J = 150 °C			300	μA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 48 A, Note 1 Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			26	mΩ

Features

- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Low drain to tab capacitance(<35pF)
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Fast intrinsic Rectifier

Applications

- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control

Advantages

- Easy assembly: no screws, or isolation foils required
- Space savings
- High power density
- Low collector capacitance to ground (low EMI)

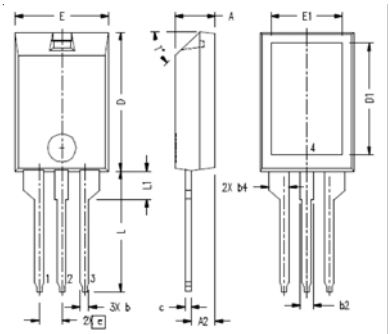
Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) Min.	Typ.	Max.	
g_{fs}	V_{DS}= 10 V; I_D = 48 A, Note 1	35	45		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		3500		pF
C_{oss}			1000		pF
C_{rss}			280		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 48 A R_G = 4 Ω (External)		30		ns
t_r			33		ns
$t_{d(off)}$			66		ns
t_f			18		ns
$Q_{g(on)}$	V_{GS}= 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 48 A		110		nC
Q_{gs}			26		nC
Q_{gd}			59		nC
R_{thJC}				1.25	K/W
R_{thCS}	(TO-247, PLUS220)		0.21		K/W

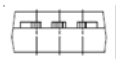
Source-Drain Diode

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) Min.	Typ.	Max.	
I_S	V_{GS} = 0 V			96	A
I_{SM}	Repetitive			250	A
V_{SD}	I_F = I_S, V_{GS} = 0 V,			1.5	V
t_{rr}	I_F = 25 A			200	ns
Q_{RM}	-di/dt = 100 A/µs		600		nC
I_{RM}	V_R = 100 V, V_{GS} = 0 V		6		A

Notes: 1. Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %

ISOPLUS220™ (IXFC) Outline





Note:
Bottom heatsink (Pin 4) is electrically isolated from Pin 1,2, or 3.

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.157	.197	4.00	5.00
A2	.098	.118	2.50	3.00
b	.035	.051	0.90	1.30
b2	.049	.065	1.25	1.65
b4	.093	.100	2.35	2.55
c	.028	.039	0.70	1.00
D	.591	.630	15.00	16.00
D1	.472	.512	12.00	13.00
E	.394	.433	10.00	11.00
E1	.295	.335	7.50	8.50
e	.100 BASIC		2.55 BASIC	
L	.512	.571	13.00	14.50
L1	.118	.138	3.00	3.50
T*			42.5°	47.5°

Ref: IXYS CO 0177 R0

Fig. 1. Output Characteristics @ 25ºC

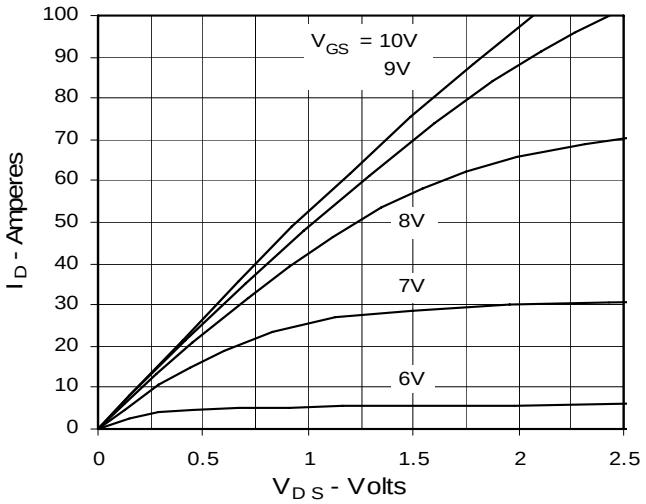


Fig. 2. Extended Output Characteristics @ 25ºC

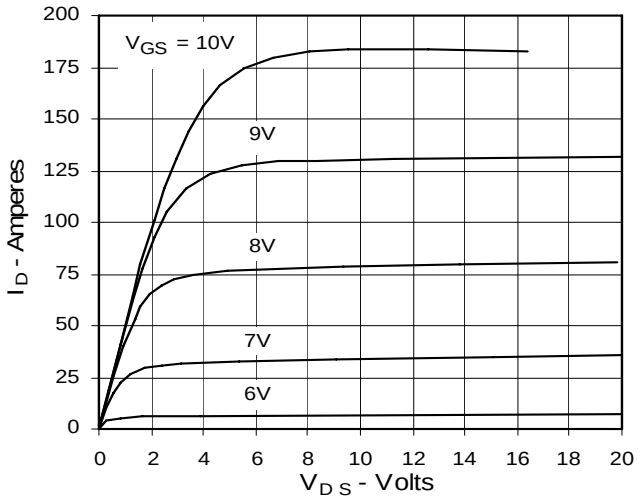


Fig. 3. Output Characteristics @ 150ºC

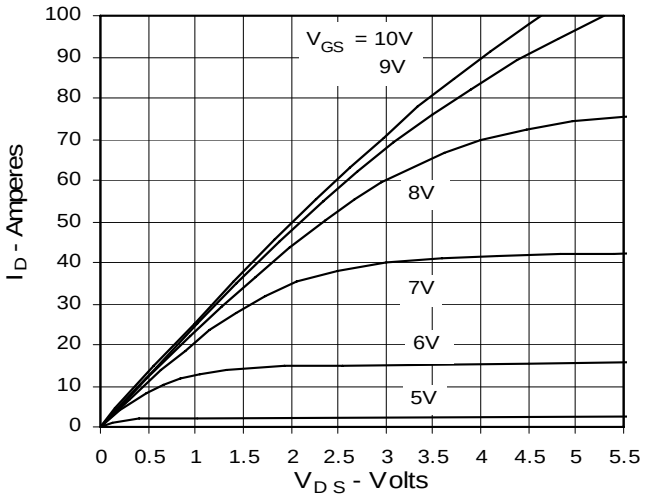


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 48 A Value vs. Junction Temperature

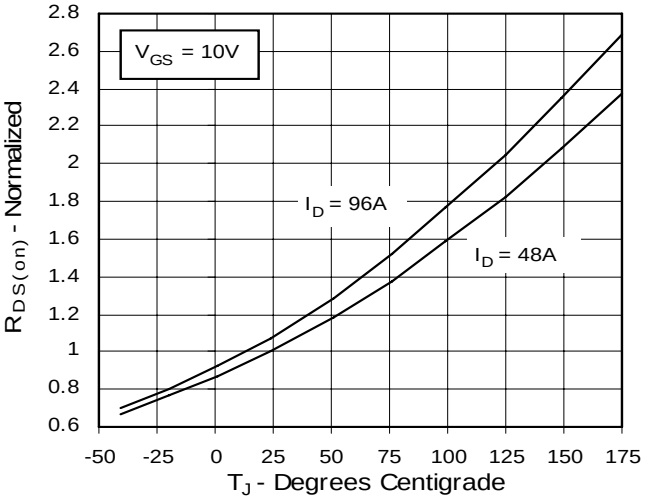


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 48 A Value vs. I_D

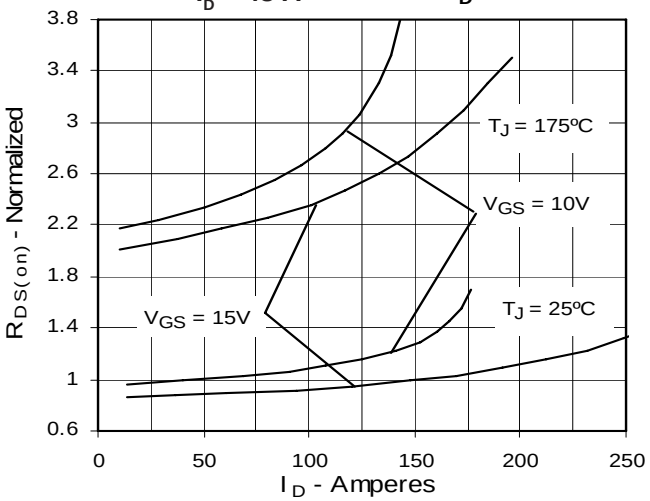


Fig. 6. Drain Current vs. Case Temperature

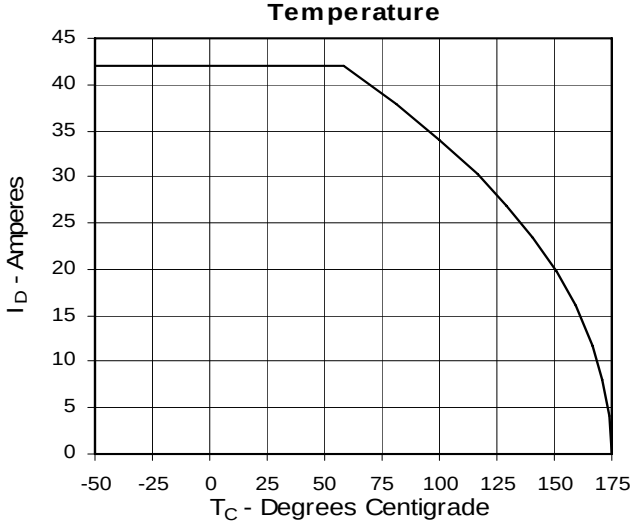


Fig. 7. Input Admittance

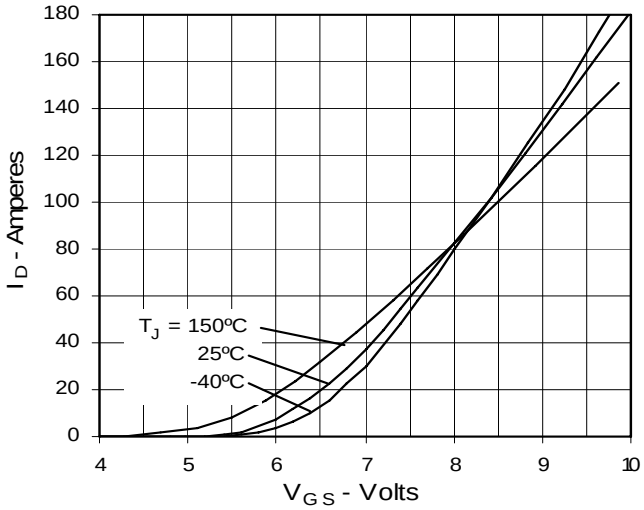


Fig. 8. Transconductance

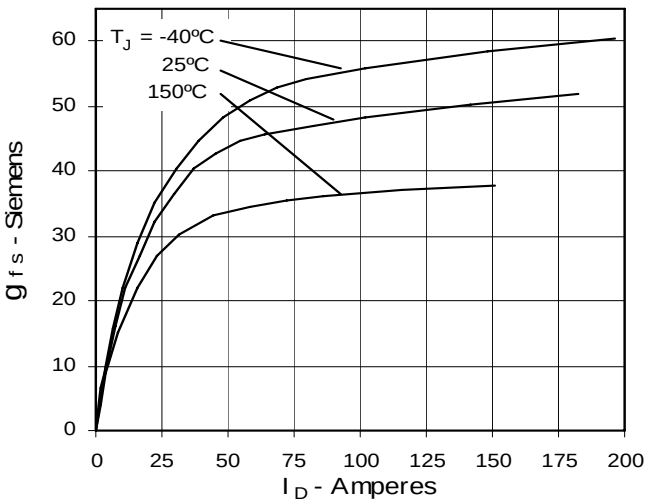


Fig. 9. Source Current vs. Source-To-Drain Voltage

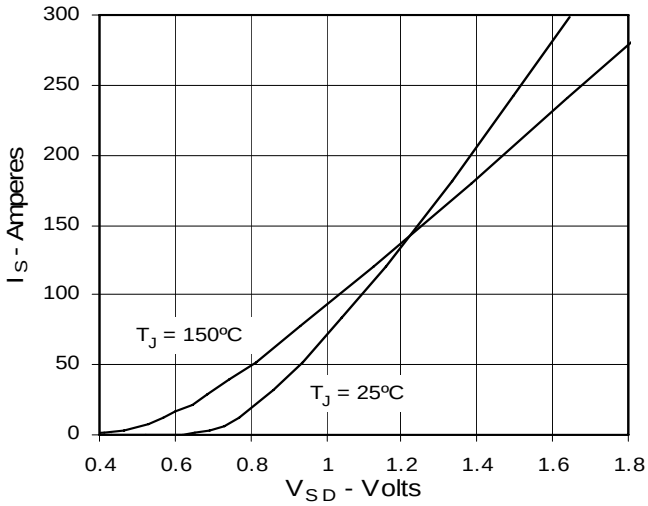


Fig. 10. Gate Charge

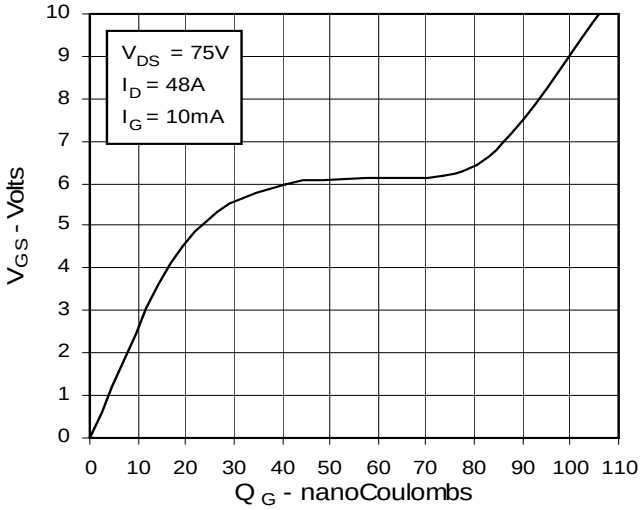


Fig. 11. Capacitance

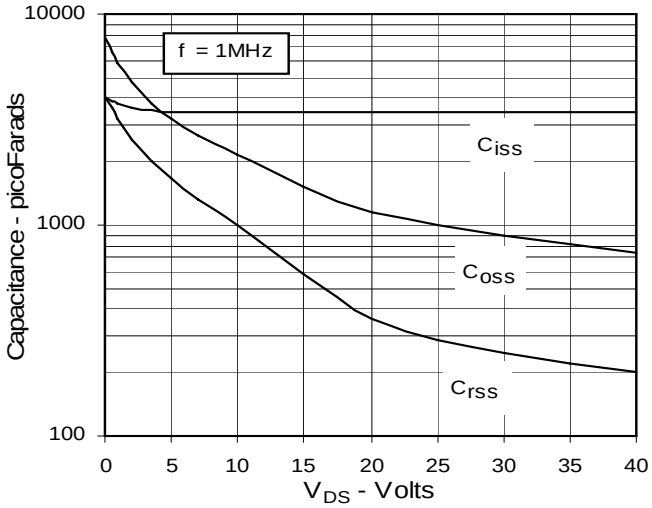


Fig. 12. Forward-Bias Safe Operating Area

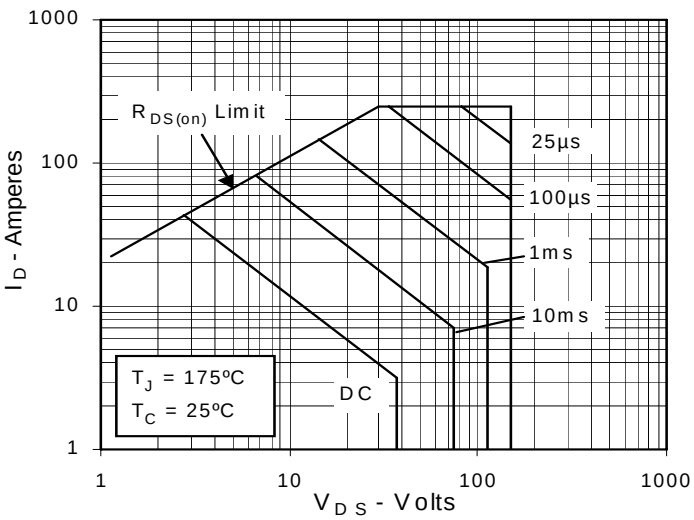


Fig. 13. Maximum Transient Thermal Resistance