HV739 ±100V 3.0A Ultrasound Pulser Demo Board

Introduction

The HV739 is a monolithic single channel, high-speed, high voltage, ultrasound transmitter pulser. This integrated, high performance circuit is in a single, 5x5mm, 32-lead QFN package.

The HV739 can deliver up to a ±3.0A source and sink current to a capacitive transducer. It is designed for the ultrasound material inspection NDT and medical ultrasound imaging applications. It can also be used as a high voltage driver for other piezoelectric or capacitive MEMS transducers, or for ATE systems and pulse signal generators as a signal source.

HV739's circuitry consists of controller logic circuits, level translators, gate driving buffers and a high current and high voltage MOSFET output stage. The output stages of each channel are designed to provide peak output currents over ±3.0A for pulsing, with up to ±100 volt swings. Two floating 12VDC power supplies referenced to V_{PP} and V_{NN} supply the P- and N-type power FET gate drivers. The upper limit frequency of the pulser waveform is 35MHz depending on the load capacitance. The HV739 can also be used as a damping circuit to generate fast return-to-zero waveforms by working with another HV739 as a pulsing circuit. It also has built-in under-voltage and over-temperature protection functions.

Designing a Pulser with the HV739

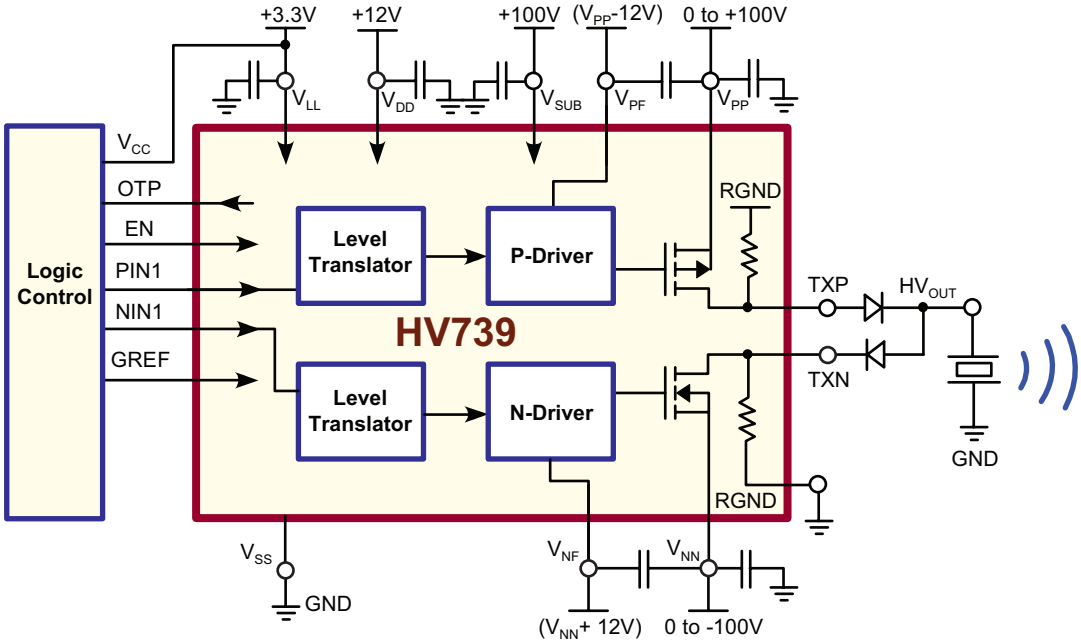
This demo board data sheet describes how to use the HV739DB1 to generate the basic high voltage pulse waveform as an ultrasound transmitting pulser.

The HV739 circuit uses the DC coupling method in all level translators. There are no external coupling capacitors needed. The V_{PP} and V_{NN} rail voltages can be changed rather quickly, compared to a high voltage capacitor gate-coupled driving pulser. This direct coupling topology of the gate drivers not only saves two high voltage capacitors per channel, but also makes the PCB layout easier.

The input stage of the HV739 has high-speed level translators that are able to operate with logic signals of 1.8 to 5.0V volts and are optimized at 3.3 to 5.0V. In this demo board, the control logic signals are connected to a high-speed ribbon cable connector. The control signal logic-high voltage should be the same as the V_{CC} voltage of the demo board, and the logic-low should be reference to GND.

The HV739DB1 output waveforms can be displayed using an oscilloscope directly by connecting the scope probe to the test point HV_{OUT} and GND. The soldering jumper can select whether or not to connect the on-board equivalent-load, a 330pF, 200V capacitor, parallel with a 2.5kΩ, 1W resistor. A coaxial cable can be used to connect the user's transducer to easily drive and evaluate the HV739 transmitter pulser.

Application Circuit



The PCB Layout Techniques

The large thermal pad at the bottom of the HV739 package is connected to the V_{SUB} pins to ensure that it always has the highest potential of the chip, in any condition. V_{SUB} is the connection of the IC's substrate. PCB designers need to pay attention to the connecting traces as the output high-voltage and high-speed traces. In particular, low capacitance to the ground plane and more trace spacing need to be applied in this situation.

High-speed PCB trace design practices that are compatible with about 50 to 100MHz operating speeds are used for the demo board PCB layout. The internal circuitry of the HV739 can operate at quite a high frequency, with the primary speed limitation being load capacitance. Because of this high speed and the high transient currents that result when driving capacitive loads, the supply voltage bypass capacitors and the driver to the FET's gate-coupling capacitors should be as close to the pins as possible. The V_{SS} pin pads should have low inductance feed-through connections that are connected directly to a solid ground plane. The V_{DD}, V_{PP}, V_{PF}, V_{NF} and V_{NN} supplies can draw fast transient currents of up to ±3.0A, so they should be provided with a low-impedance bypass capacitor at the chip's pins. A ceramic capacitor of up to 0.22 to 1.0µF may be used. Minimize the trace length to the ground plane, and insert a ferrite bead in the power supply lead to the capacitor to prevent resonance in the power supply lines. For applications that are sensitive to jitter and noise, and for using multiple HV739 ICs, insert another ferrite bead between V_{DD} and decouple each chip supply separately.

Pay particular attention to minimizing trace lengths and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of HV739's high voltage power stages is very low, in some cases it may be desirable to add a small value resistor in series with the output to obtain better waveform integrity at the load terminals. This will, of course, reduce the output voltage slew rate at the terminals of a capacitive load. Be aware of the parasitic coupling from the outputs to the input signal terminals of HV739. This feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.8V, even small coupling voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Also ensure that the circulating ground return current from a capacitive load cannot react with common inductance to create noise voltages in the input logic circuitry.

Testing the Integrated Pulser

The HV739 pulser demo board should be powered up with multiple lab DC power supplies with current limiting functions. The following power supply voltages and current limits have been used in the testing: V_{PP}= 0 to +100V 10mA, V_{NN}= 0 to -100V 10mA, V_{DD}= +12V 20mA, (V_{PP}-V_{PF}) = +12V 20mA, (V_{NF}-V_{NN}) = +12V 20mA. V_{CC}= +3.3V 5.0mA for HV739 V_{LL}, not including the user's logic circuits.

The power-up or down sequences of the voltage supply ensure that the HV739 chip substrate V_{SUB} is always at the highest potential of all the voltages supplied to the IC.

The (V_{PP}–V_{PF}) and (V_{NF}–V_{NN}) are the two floating power supplies. They are only 12V, but floating with V_{PP} and V_{NN}. The floating voltages can be trimmed within the range of +8.0~+12V to adjust the rising and falling time of the output pulses for the best HD2. Do not exceed the maximum voltage of +12V. The V_{PP} and V_{NN} are the positive and negative high voltages. They can be varied from 0 to +/-100V maximum. Note when the V_{PP}= V_{NN}= 0, the V_{PF} and V_{NF} in respect to the ground voltage is –12V and +12V.

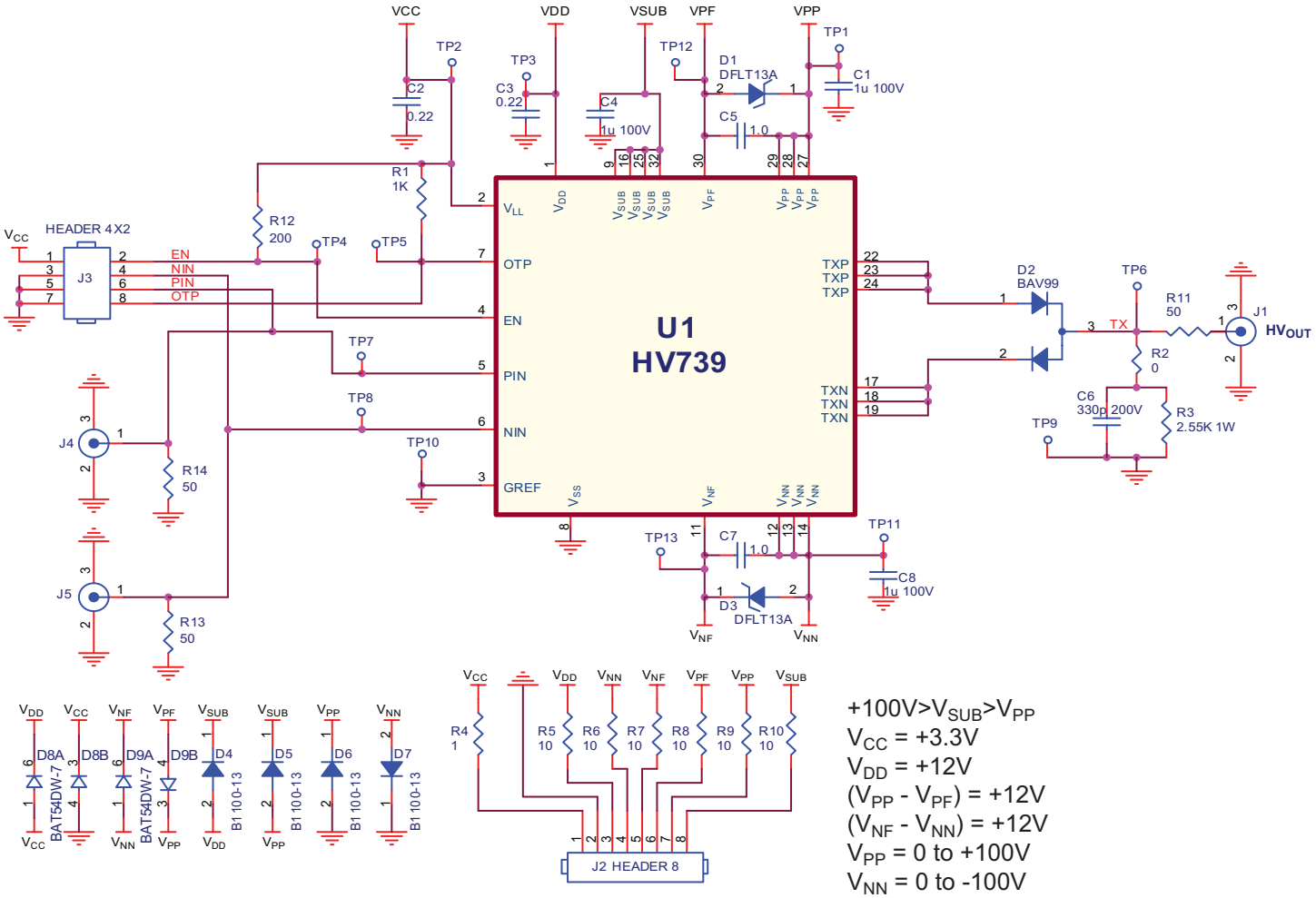
The on-board dummy load 330pF//2.5kΩ should be connected to the high voltage pulser output through the solder jumper when using an oscilloscope's high impedance probe to meet the typical loading condition. To evaluate different loading conditions, one may change the values of RC within the current and power limit of the device.

In order to drive the user's piezo transducers with a cable, one should match the output load impendence properly to avoid cable and transducer reflections. A 50Ω coaxial cable is recommended. The coaxial cable end should be soldered to the HV_{OUT} and GND directly with very short leads. If a user's load is being used, the on-board dummy load should be disconnected by cutting the small shorting copper trace in between the zero ohm resistors R7, R8, R9 or R10 pads. They are shorted by factory default.

All the on-board test points are designed to work with the high impedance probe of the oscilloscope. Some probes may have limited input voltage. When using the probe on these high voltage test-points, make sure that V_{PP}/V_{NN} voltages do not exceed the probe limit. Using the high impendence oscilloscope probe for the on-board test points, it is important to have short ground leads to the circuit board ground plane.

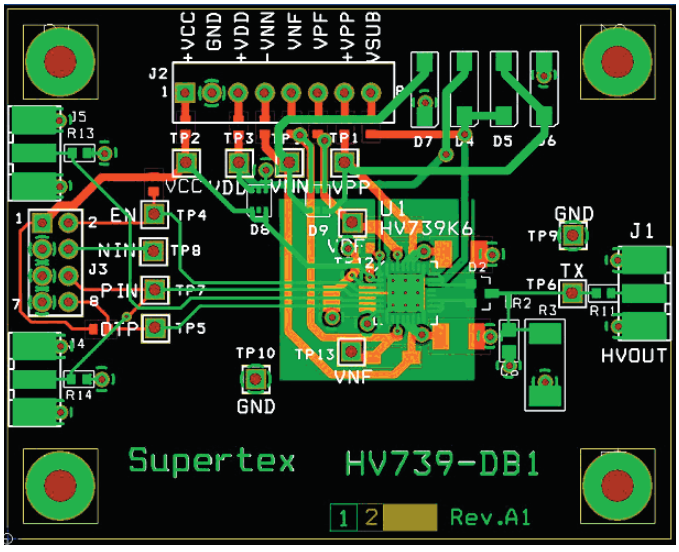
Precautions need to be applied to not overlap the logic-high time periods of the control signals. Otherwise, permanent damage to the device may occur when cross-conduction or shoot-through currents exceed the device's maximum limits.

HV739DB1 Schematic



+100V>V_{SUB}>V_{PP}
V_{CC} = +3.3V
V_{DD} = +12V
(V_{PP} - V_{PF}) = +12V
(V_{NF} - V_{NN}) = +12V
V_{PP} = 0 to +100V
V_{NN} = 0 to -100V

HV739DB1 PCB



Board Voltage Supply Power-Up Sequence

1	V_{CC}	+1.2 to 5.0V positive logic supply voltage for HV739 V_{LL} and user logic circuit.
2	V_{DD}	+12V positive drive supply voltage
3	V_{PF} and V_{NF}	Floating supply voltages, (V_{PP}- V_{PF})= +12V and (V_{NF}- V_{NN}) = +12V
4	V_{SUB}	+100V>V_{SUB}/V_{PP} positive bias voltages
5	V_{PP} / V_{NN}	0 to +/-100V positive and negative high voltages
6	Logic Active	Any logic control active high signals

Note: *The Power-down sequence should be revising as to the power-up sequence above*

Connector and Test Pin Description

Logic Control Signal Input Connector

1	V_{CC}	Logic-high reference voltage input, V_{LL}, +1.2 to 5.0V, normally from control circuit.
2	EN	Pulser output enable logic signal input, active high.
3	GND	Logic signal ground, 0V (2).
4	NIN1	Logic signal input for CH1 negative pulse output, active high. (1)
5	GND	Logic signal ground, 0V.
6	PIN1	Logic signal input for CH1 positive pulse output, active high. (1)
7	GND	Logic signal ground, 0V.
8	OTP	Open drain output of over-temperature protection logic signal, active low.

Power Supply Connector

1	V_{CC}	Logic-high reference voltage supply, +1.2 to 5.0V current limit 5.0mA (for V_{LL} only).
2	GND	Low voltage power supply ground, 0V
3	V_{DD}	+12V positive driver voltage supply with current limit to 10mA.
4	V_{NN}	0 to -100V negative high voltage supply with current limit to 5.0mA
5	V_{NF}	Floating voltage supply (V_{NF}-V_{NN}) = +12V with current limit to 10mA. (3)
6	V_{PF}	Floating voltage supply (V_{PP}-V_{PF}) = +12V with current limit to 10mA. (3)
7	V_{PP}	0 to +100V positive high voltage supply with current limit to 2.0mA
8	V_{SUB}	Chip substrate bias voltage, must be (+100V>V_{SUB}/V_{PP}) with limit to 5.0mA

Note:

(1). Overlap control signals logic-high periods of PIN and NIN may cause the device permanent damage.

(2). Due to the speed of logic control signal, every GND wire in the ribbon cable must connect to signal source ground.

(3). (V_{PP}-V_{PF}) and (V_{NF}-V_{NN}) floating voltage can be trimmed from +8V to +12V for tr/tf time matching. Do not exceed the maximum +12V.

HV739DB1 Waveforms

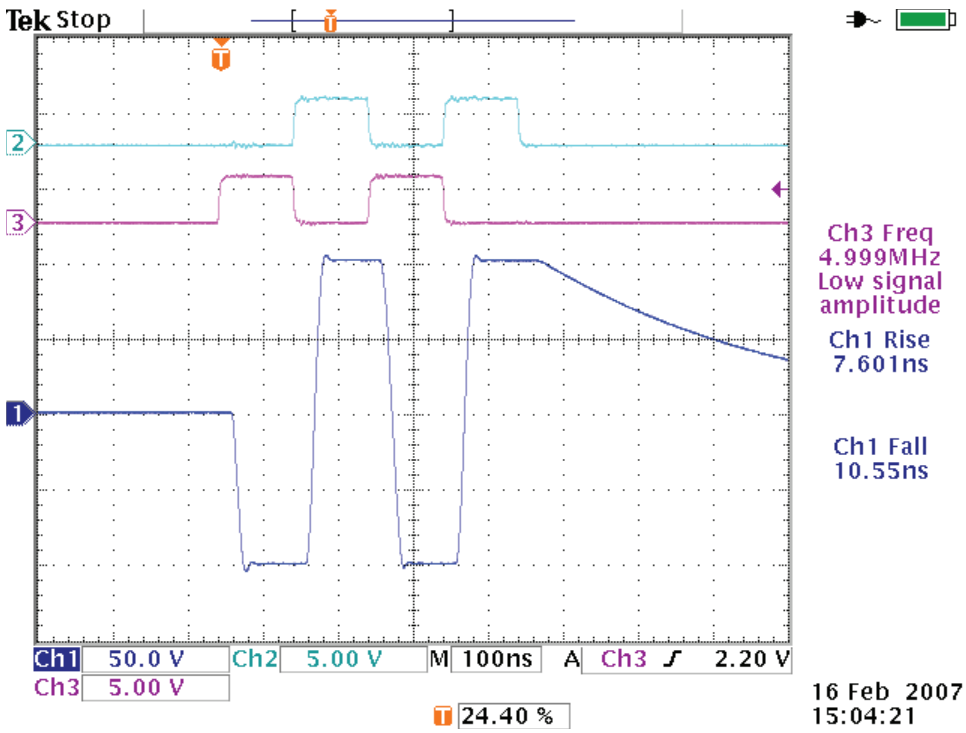


Figure 1: NIN, PIN and output waveform of 5.0MHz, V_{LL}= 3.3V, V_{DD}= +12V, (V_{PP}-V_{PF}) = +12V, (V_{NF}-V_{NN}) = +12V, V_{PP}/V_{NN}= +/-48V, V_{SUB}= +100V with load of 330pF//2.5K.

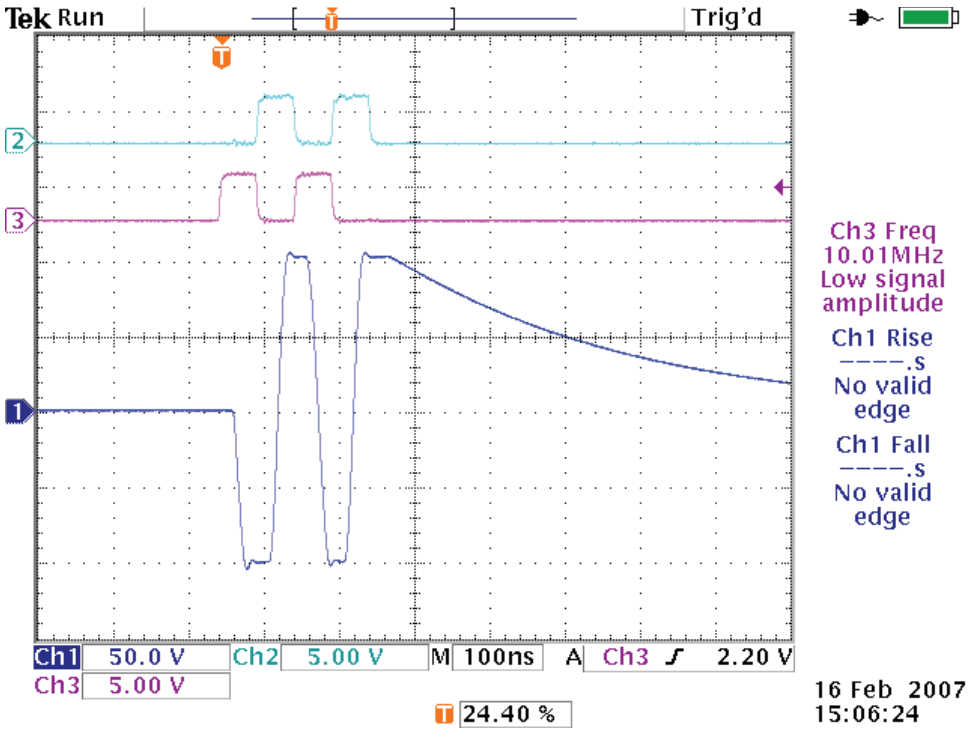


Figure 2: NIN, PIN and output waveform of 10MHz, V_{LL}= 3.3V, V_{DD}= +12V, (V_{PP}-V_{PF}) = +12V, (V_{NF}-V_{NN})= +12V, V_{PP}/V_{NN}= +/-48V, V_{SUB}= +100V with load of 330pF//2.5K.

HV739DB1 Waveforms *(cont.)*

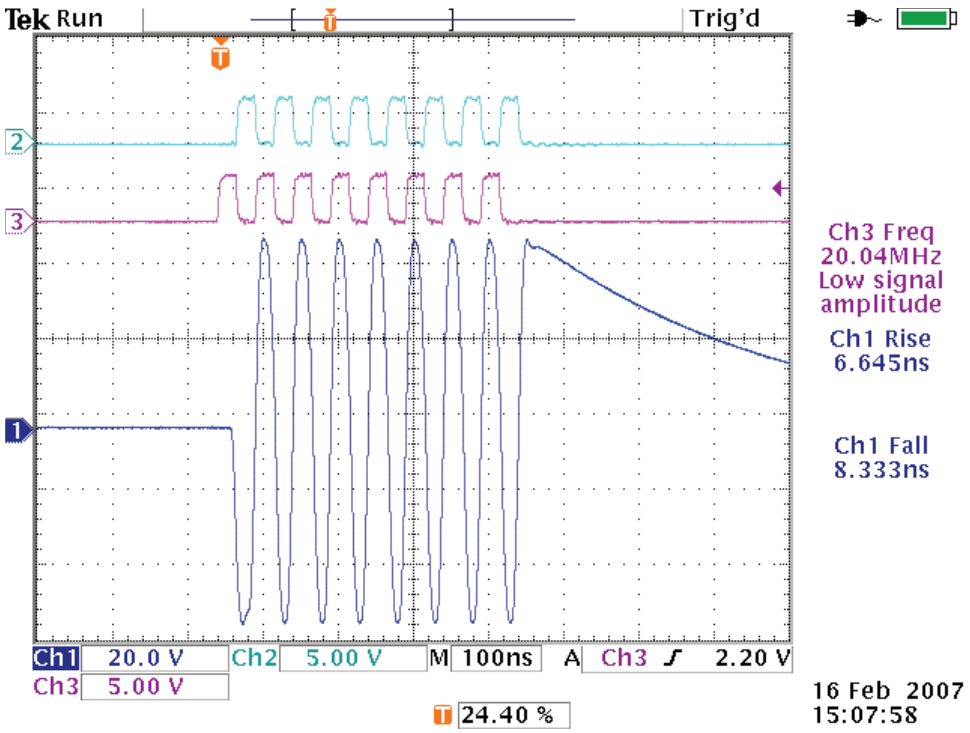


Figure 3: NIN, PIN and output waveform of 20MHz, V_{LL}= 3.3V, V_{DD}= +12V, (V_{PP}-V_{PF})= +12V, (V_{NF}-V_{NN})= +12V, V_{PP}/V_{NN}= +/-48V, V_{SUB}= +100V with load of 330pF//2.5K.

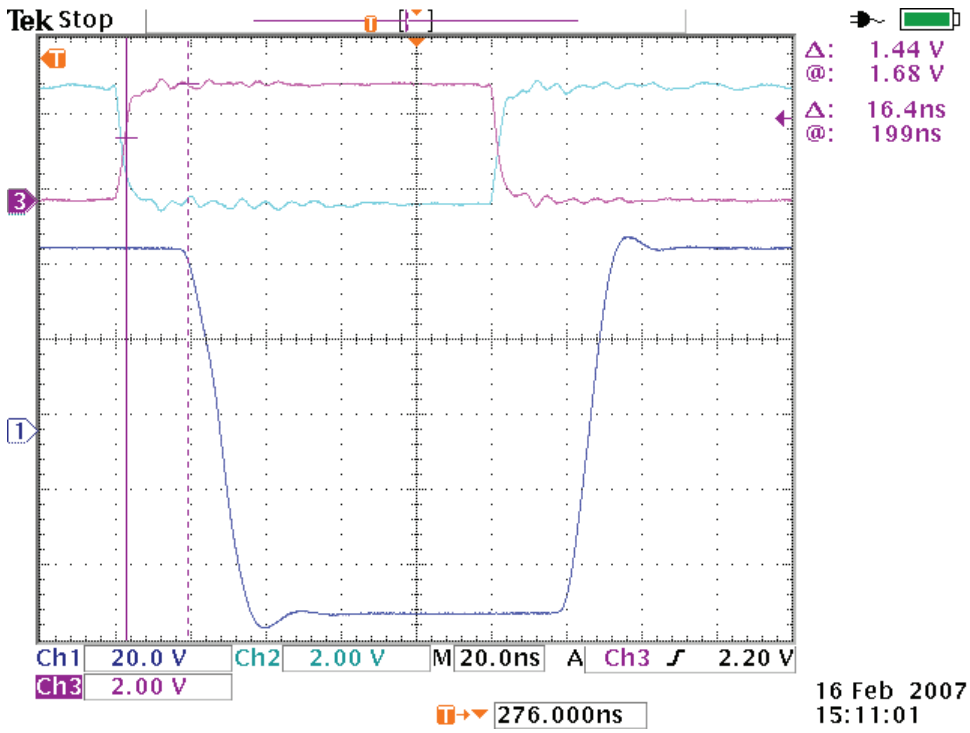


Figure 4: Input to output propagation delay on falling edge is 16.4ns and the tr/tf time are about 10ns/12ns. V_{LL}= 3.3V, V_{DD}= +12V, (V_{PP}-V_{PF})= +12V, (V_{NF}-V_{NN})= +12V, V_{PP}/V_{NN}= +/-48V, V_{SUB}= +100V with load of 330pF//2.5K.

HV739DB1 Waveforms *(cont.)*

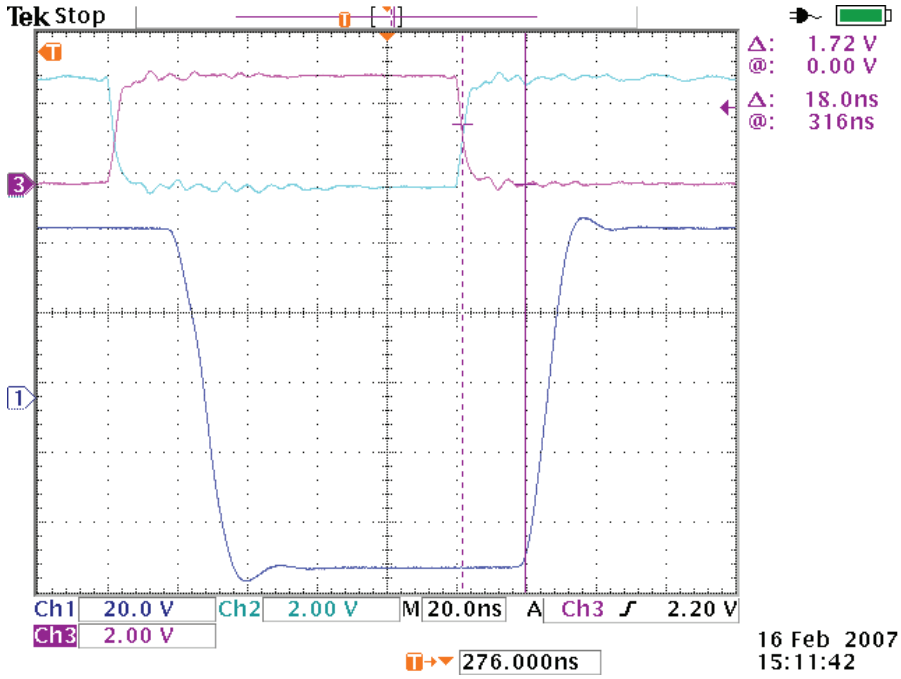


Figure 5: Input to output propagation delay on rising edge is 18ns and the tr/tf time are about 10ns/12ns. V_{LL}= 3.3V, V_{DD}= +12V, (V_{PP}-V_{PF})= +12V, (V_{NF}-V_{NN})= +12V, V_{PP}/V_{NN}= +/-48V, V_{SUB}= +100V with load of 330pF//2.5K.

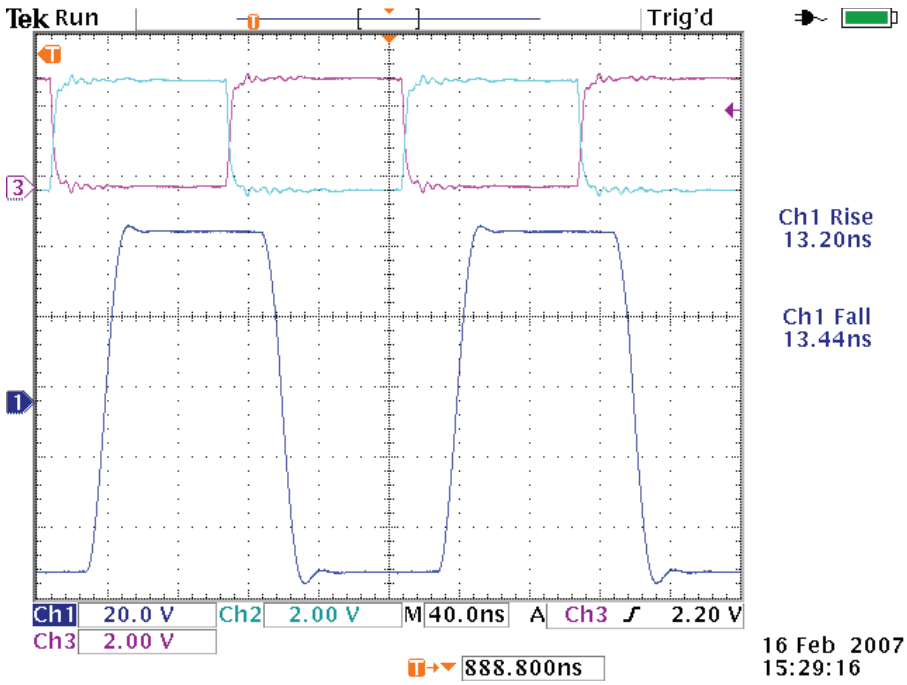


Figure 6: Input to output waveforms of the tr/tf time are about 13ns/13ns at V_{LL}= 3.3V, V_{DD}= +8.5V, (V_{PP}-V_{PF})= +8.5V, (V_{NF}-V_{NN})= +8.5V, V_{PP}/V_{NN}= +/-48V, V_{SUB}= +100V with load of 330pF//2.5K.

HV739DB1 Waveforms *(cont.)*

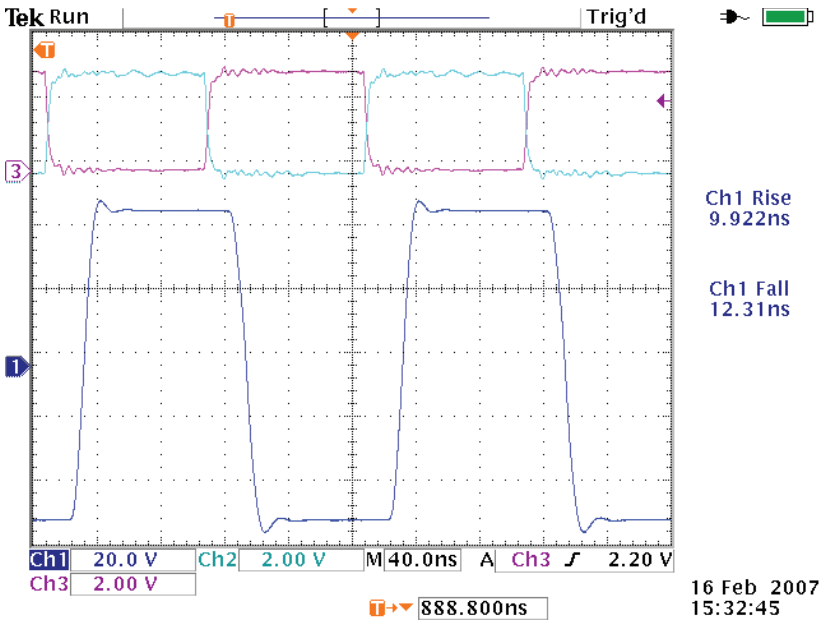


Figure 7: Input to output waveforms of the tr/tf time are about 10ns/12.3ns at V_{LL}= 3.3V, V_{DD}= +12V, (V_{PP}-V_{PF})= +12V, (V_{NF}-V_{NN})= +12V, V_{PP}/V_{NN}= +/-48V, V_{SUB}= +100V with load of 330pF//2.5K.

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