



SANYO Semiconductors

DATA SHEET

LA6574D — Monolithic Linear IC

Five-Channel Driver (four BTL channels plus one H bridge channel) for MD and CD Player

Overview

The LA6574D is a motor driver IC for MD and CD players with four BTL channels and one H bridge channel. The LA6574D features a separate power supply for the H bridge block, an output adjustment pin, and a 3.3V regulator to support a wide range of applications.

Features and Features

- Four power amplifier channels plus one H bridge channel
- I_O max: 700mA (each channel)
- Built-in level shifting circuits for the BLT amplifiers
- Thermal protection circuit (Thermal shutdown circuit)
- Separate loading block power supply
- Built-in 3.3V regulator
- Provides a dedicated pin for adjusting the loading block output

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|--------------|------------------------------|-------------|------------------|
| Supply voltage | V_{CC} max | | 14 | V |
| Allowable power dissipation | P_d max | Independent IC | 1.2 | W |
| | | Mounted on a specified board | 2.0 | W |
| Maximum output current | I_O max | Each channel for CH1 to CH5 | 0.7 | A |
| Maximum input voltage | V_{INB} | | 13 | V |
| MUTE pin voltage | V_{MUTE} | | 13 | V |
| Operating temperature | T_{opr} | | -30 to +85 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +150 | $^\circ\text{C}$ |

* Mounted on a specified board: 76.1mm×114.3mm×1.6mm glass epoxy

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LA6574D

Recommended Operating Conditions at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------|-----------------|------------|-----------|------|
| Supply voltage | V _{CC} | | 5.6 to 13 | V |

Electrical Characteristics at Ta = 25°C, V_{CC1} = V_{CC2} = 8V, VREF = 1.65V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|----------------------|--|---------|-----|----------------------|-------|
| | | | min | typ | max | |
| [Overall Characteristics] | | | | | | |
| No load current drain - I _{CC} on | I _{CC} -ON | All outputs on, FWD = REV = 0V *1 | | 30 | 50 | mA |
| VREF input voltage range | VREF-IN | | 1 | | V _{CC} -1.5 | V |
| [BTL Amplifier Block] | | | | | | |
| Output offset voltage | VOFF | BTL amplifiers, the voltage difference across each channel's output | -50 | | 50 | mV |
| Input voltage range | V _{IN} | Input resistance: 11kΩ | 0 | | V _{CC} | V |
| Output voltage | V _O | The voltage between each of the V _{O+} /V _{O-} pairs when R _L is 8Ω. *2 | 4 | 5 | | V |
| Closed loop voltage gain | VG | Gain from input to output | | 4 | | Times |
| Slew rate | SR | With the amplifier operating independently, twice the value measured between outputs *3 | | 0.5 | | V/μs |
| [H Bridge Block] | | | | | | |
| Output voltage | V _O -LOAD | The voltage between each of the V _{O+} /V _{O-} pairs when R _L is 8Ω. *2 | | 6 | | V |
| Low-level input voltage | V _{IN} -L | | | | 1 | V |
| High-level input voltage | V _{IN} -H | | 2 | | | V |
| Output control voltage | VCONT | VCONT = 3V *2 | | 3.5 | | V |
| [Regulator Block] | | | | | | |
| Output voltage | Vreg | I _L = 100mA | 3.05 | 3.3 | 3.55 | V |
| Load regulation | ΔVRL | I _L = 0 to 200mA | -50 | 0 | 10 | mV |
| Line regulation | ΔVV _{CC} | V _{CC} = 6 to 12V, I _L = 100mA | -15 | 21 | 60 | mV |

Note *1: The total current drain for V_{CC1} and V_{CC2} with no load.

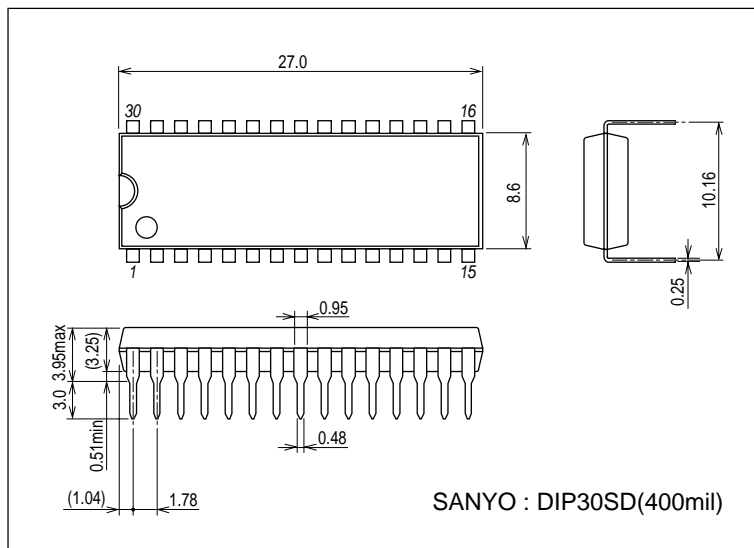
*2: Voltage difference across the load (8Ω). With the outputs in the saturated state.

*3: Design guarantee value

Package Dimensions

unit : mm (typ)

3196A



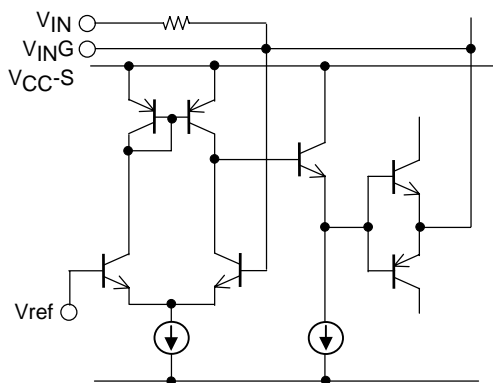
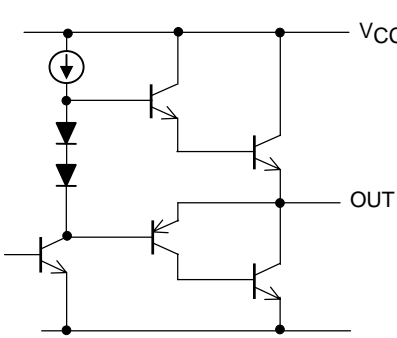
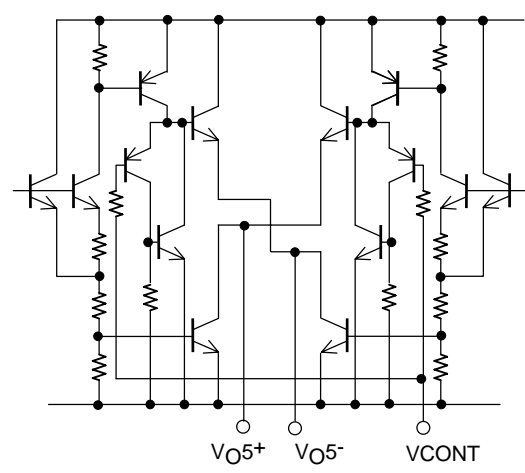
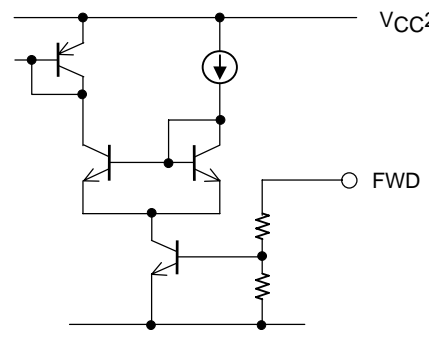
Pin Functions

| Pin No. | Pin Name | Description |
|---------|-------------------------------|--|
| 1 | REV | 5CH (VLO) Output change pin (REV), Logic input for loading block |
| 2 | FWD | 5CH (VLO) Output change pin (FWD), Logic input for loading block |
| 3 | S-GND | Signal system GND |
| 4 | VCONT | Channel 5 (VLO) output voltage control |
| 5 | V _{IN} 4 | Input pin for channel 4 |
| 6 | V _{IN} 4G | Input pin for channel 4 (for gain control) |
| 7 | V _{CC} -S | Signal system power (V _{CC} 1 and V _{CC} 2 short-circuited) |
| 8 | VREF-IN | Reference voltage input pin |
| 9 | REG-OUT | Regulator pin (External PNP collector) |
| 10 | REG-IN | Regulator pin (External PNP base) |
| 11 | V _{IN} 3G | Input pin for channel 3 (for gain control) |
| 12 | V _{IN} 3 | Input pin for channel 3 |
| 13 | V _{IN} 2G | Input pin for channel 2 (for gain control) |
| 14 | V _{IN} 2 | Input pin for channel 2 |
| 15 | V _{IN} 1G | Input pin for channel 1 (for gain control) |
| 16 | V _{IN} 1 | Input pin for channel 1 |
| 17 | V _{CC} 1 | Power for channels 1 and 2 (BTL), (V _{CC} -S and V _{CC} 2 short-circuited) |
| 18 | (NC) | No connect |
| 19 | V _O 1 ⁻ | Output pin (-) for channel 1 |
| 20 | V _O 1 ⁺ | Output pin (+) for channel 1 |
| 21 | V _O 2 ⁻ | Output pin (-) for channel 2 |
| 22 | V _O 2 ⁺ | Output pin (+) for channel 2 |
| 23 | P-GND | Power GND |
| 24 | V _O 3 ⁻ | Output pin (-) for channel 3 |
| 25 | V _O 3 ⁺ | Output pin (+) for channel 3 |
| 26 | V _O 4 ⁻ | Output pin (-) for channel 4 |
| 27 | V _O 4 ⁺ | Output pin (+) for channel 4 |
| 28 | V _O 5 ⁺ | Loading output (+) |
| 29 | V _O 5 ⁻ | Loading output (-) |
| 30 | V _{CC} 2 | Power for channels 3, 4, and 5 (V _{CC} 1 and V _{CC} -S short-circuited) |

*The P-GND functions as power system GND. Set this to the minimum potential together with S-GND.

*Short-circuit three pins of power system, V_{CC}-S, V_{CC}1, and V_{CC}2, externally before use.

Pin Description

| Pin No. | Symbol | Pin Name | Description | Equivalent Circuit |
|--|--|------------|----------------------------|--|
| 5 6 11 12 13 14 15 16 | V_{IN4} V_{IN4G} V_{IN3G} V_{IN3} V_{IN2G} V_{IN2} V_{IN1G} V_{IN1} | Input | Input pin for each channel |  |
| 19 20 21 22 24 25 26 27 | V_{O1-} V_{O1+} V_{O2-} V_{O2+} V_{O3-} V_{O3+} V_{O4-} V_{O4+} | Output | Each output |  |
| 28 29 4 | V_{O5+} V_{O5-} VCONT | V_{O5} | H bridge output |  |
| 2 1 | FWD REV | FWD REV | H bridge input |  |

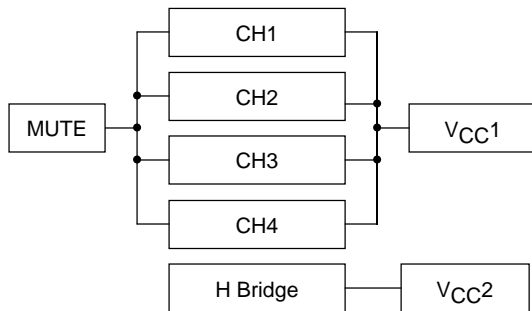
H Bridge Block

| FWD | REV | V _{O5+} | V _{O5-} | Mode |
|-----|-----|------------------|------------------|----------|
| L | L | OFF | OFF | Open *1 |
| L | H | H | L | Forward |
| H | L | L | H | Reverse |
| H | H | L | L | Brake *2 |

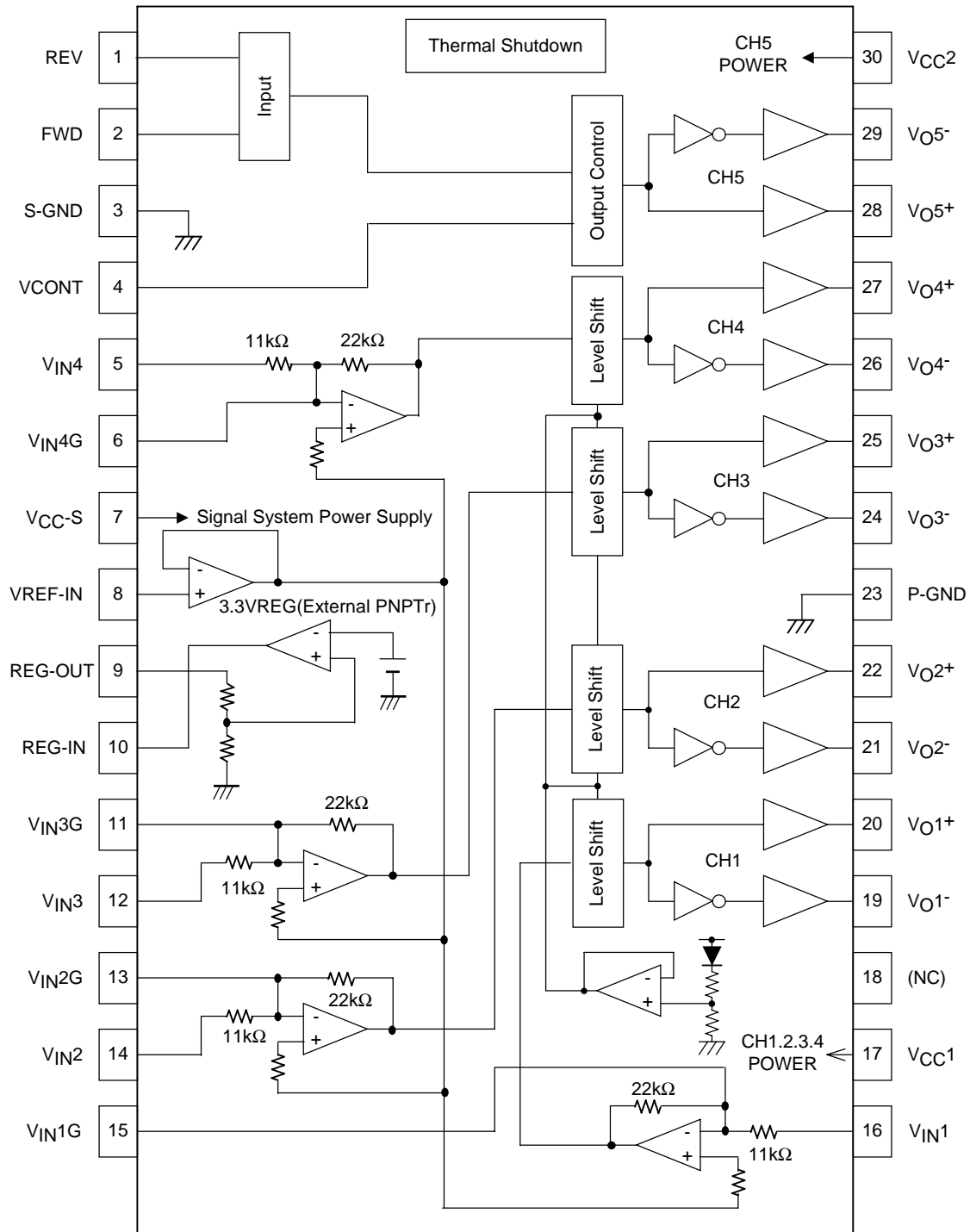
*1: Output: High impedance

*2: In case of braking, the SINK side transistor is turned ON (short brake). V_{LO+} and V_{LO-} are approximately on the GND level.

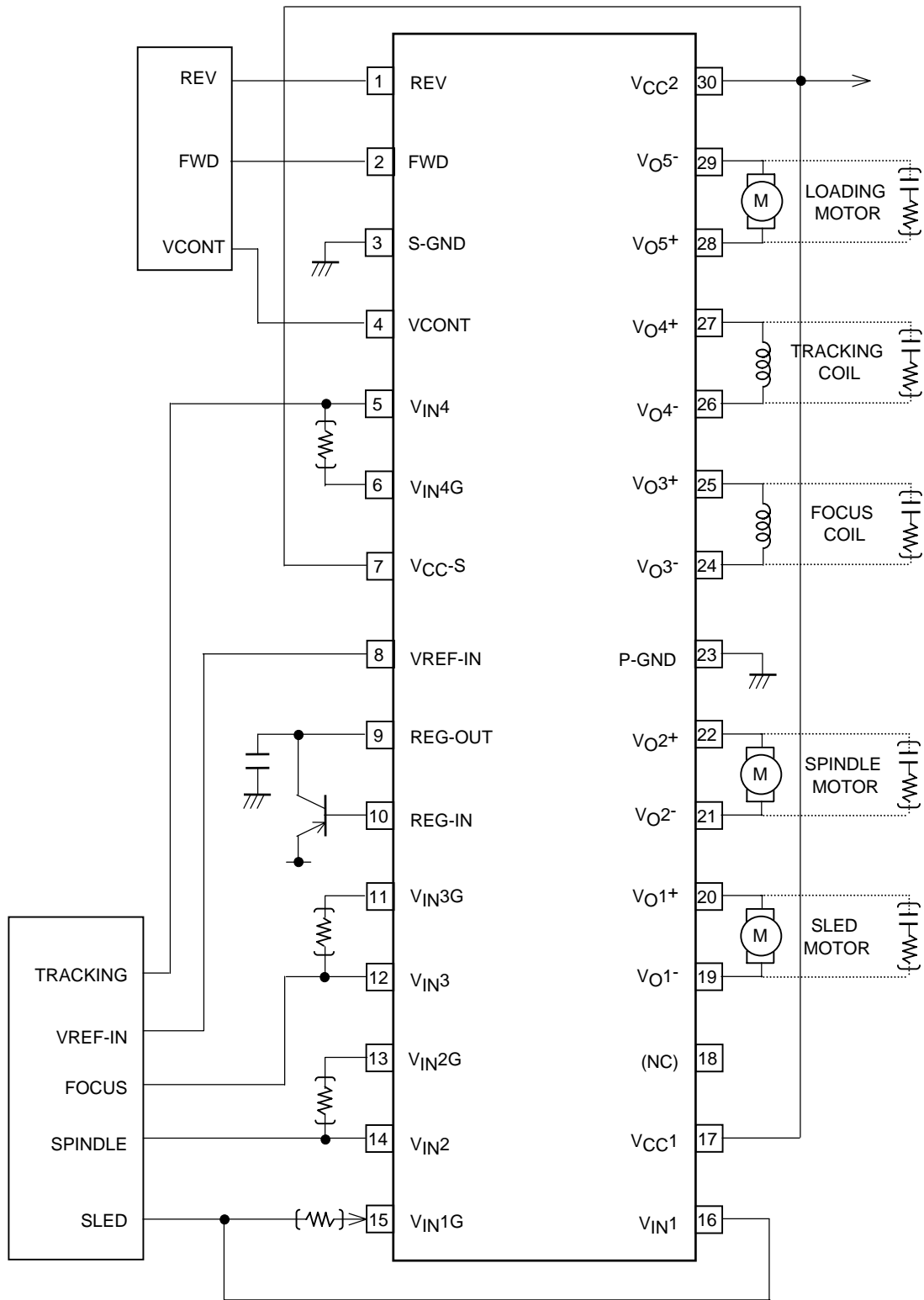
*3: V_{CONT} (output voltage setting pin) and V_{LO} have the following relationship: $V_{LO} = V_{CONT} - 1V$ (typical)

Relationship between the MUTE pin and the power supplies (V_{CC}*)

Block Diagram



Sample Application Circuit



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