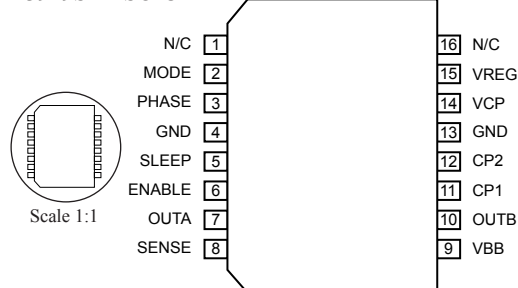


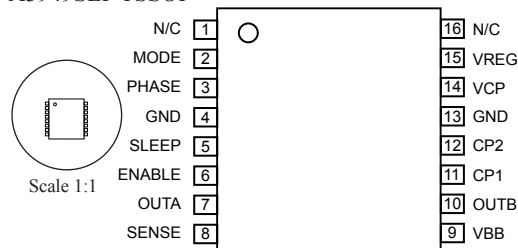
A3949

DMOS Full-Bridge Motor Driver

A3949SLB SOIC



A3949SLP TSSOP



ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage

V_{BB} 36 V

V_{BB} (Peak < 2 μ s) 38 V

Output Current, I_{OUT} (Repetitive)¹ ± 2.8 A

Sense Voltage, V_{SENSE} 0.5 V

Logic Input Voltage, V_{IN} -0.3 V to 7 V

Package Power Dissipation, P_D

A3949SLB² 52°C / W

A3949SLP³ 34°C / W

Operating Temperature Range

Ambient Temperature, T_A -20°C to +85°C

Junction Temperature, T_J +150°C Max.

Storage Temperature, T_S -55°C to +150°C

¹Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, DO NOT exceed the specified I_{OUT} or T_J .

²Measured on a typical two-sided PCB with 2 in.² copper ground plane.

³Measured on a JEDEC-standard "High-K" 4-layer PCB.

Designed for PWM (pulse width modulated) control of dc motors, the A3949 is capable of peak output currents to ± 2.8 A and operating voltages to 36 V.

PHASE and ENABLE input terminals are provided for use in controlling the speed and direction of a dc motor with externally applied PWM control signals. Internal synchronous rectification control circuitry is provided to reduce power dissipation during PWM operation.

Internal circuit protection includes thermal shutdown with hysteresis, undervoltage monitoring of V_{BB} and V_{CP} , and crossover current protection.

The A3949 is supplied in a choice of two power packages, a 16-pin plastic SOIC with a copper batwing tab (part number suffix *LB*), and a low profile (1.1mm) 16-pin TSSOP (suffix *LP*) with exposed power tab. Both packages are available in a lead-free version (100% matte tin leadframe).

FEATURES

- Single supply operation
- Very small outline package
- Low $R_{DS(ON)}$ outputs
- Sleep function
- Internal UVLO
- Crossover current protection
- Thermal shutdown protection

Use the following complete part numbers when ordering:

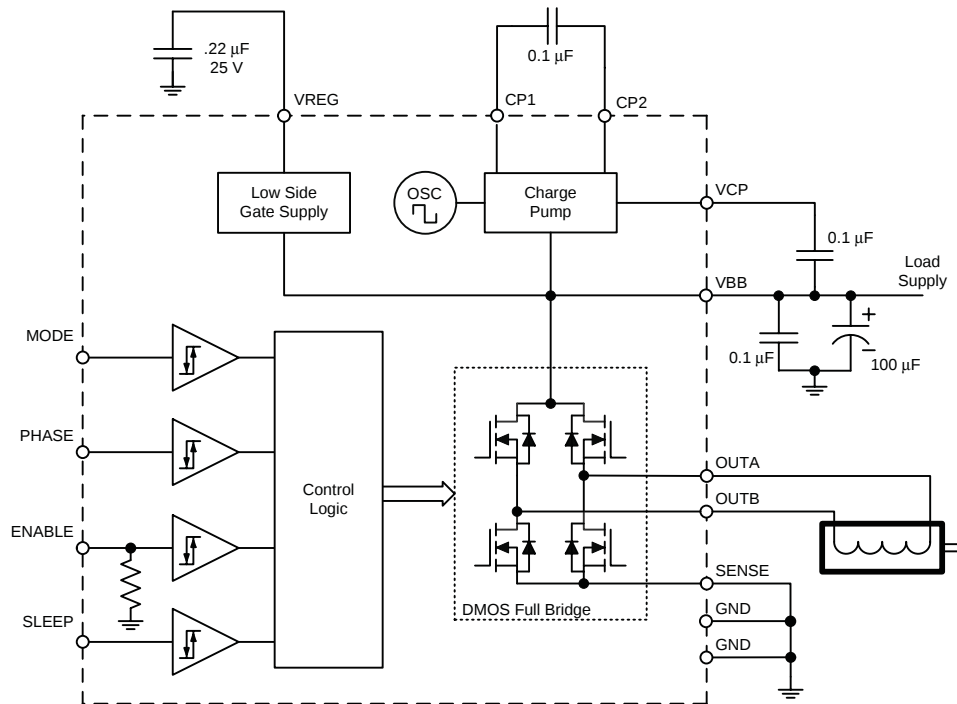
Part Number	Pb-free*	Package	Packing
A3949SLB-T	Yes	16-pin, SOIC	47 per tube
A3949SLBTR-T	Yes	16-pin, SOIC	1000 per reel
A3949SLP-T	Yes	16-pin, TSSOP	96 per tube
A3949SLPTR-T	Yes	16-pin, TSSOP	4000 per reel

*Pb-based variants are being phased out of the product line. The variants cited in this footnote are in production but have been determined to be LAST TIME BUY. This classification indicates that sale of this device is currently restricted to existing customer applications. The variants should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: October 31, 2006. Deadline for receipt of LAST TIME BUY orders: April 27, 2007. These variants include: A3949SLB, A3949SLBTR, A3949SLP, and A3949SLPTR.

A3949

DMOS Full-Bridge Motor Driver

Functional Block Diagram



Control Logic Table

PHASE	ENABLE	MODE	SLEEP	OUTA	OUTB	Function
1	1	X	1	H	L	Forward
0	1	X	1	L	H	Reverse
X	0	1	1	L	L	Brake (slow decay)
1	0	0	1	L	H	Fast decay SR*
0	0	0	1	H	L	Fast decay SR*
X	X	X	0	Hi-Z	Hi-Z	Sleep mode

* To prevent reversal of current during fast decay SR (synchronous rectification), the outputs go to the high impedance state as the current approaches zero.

A3949

DMOS Full-Bridge Motor Driver

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $V_{BB} = 8\text{ V}$ to 36 V (unless otherwise noted)

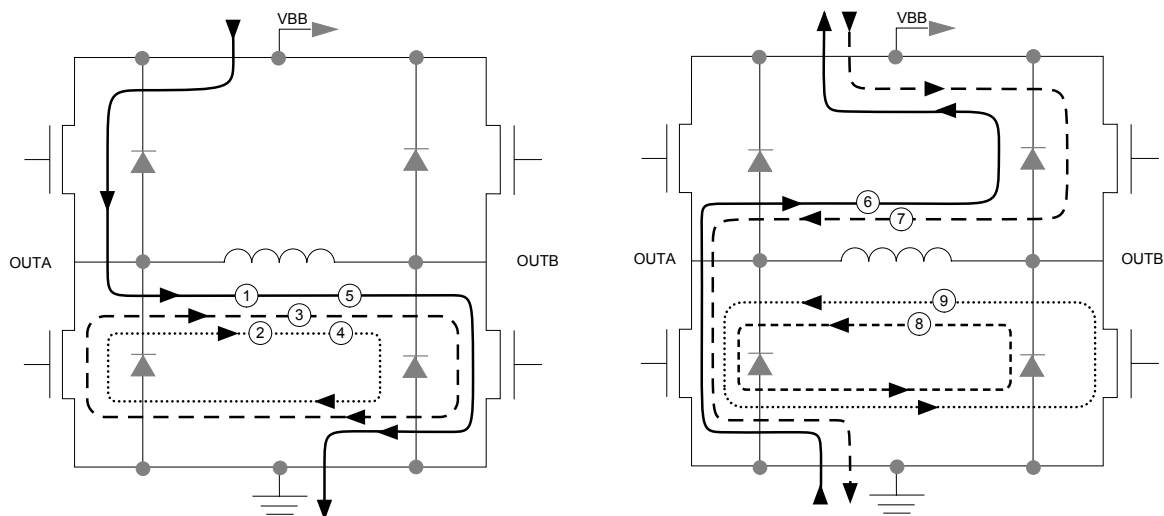
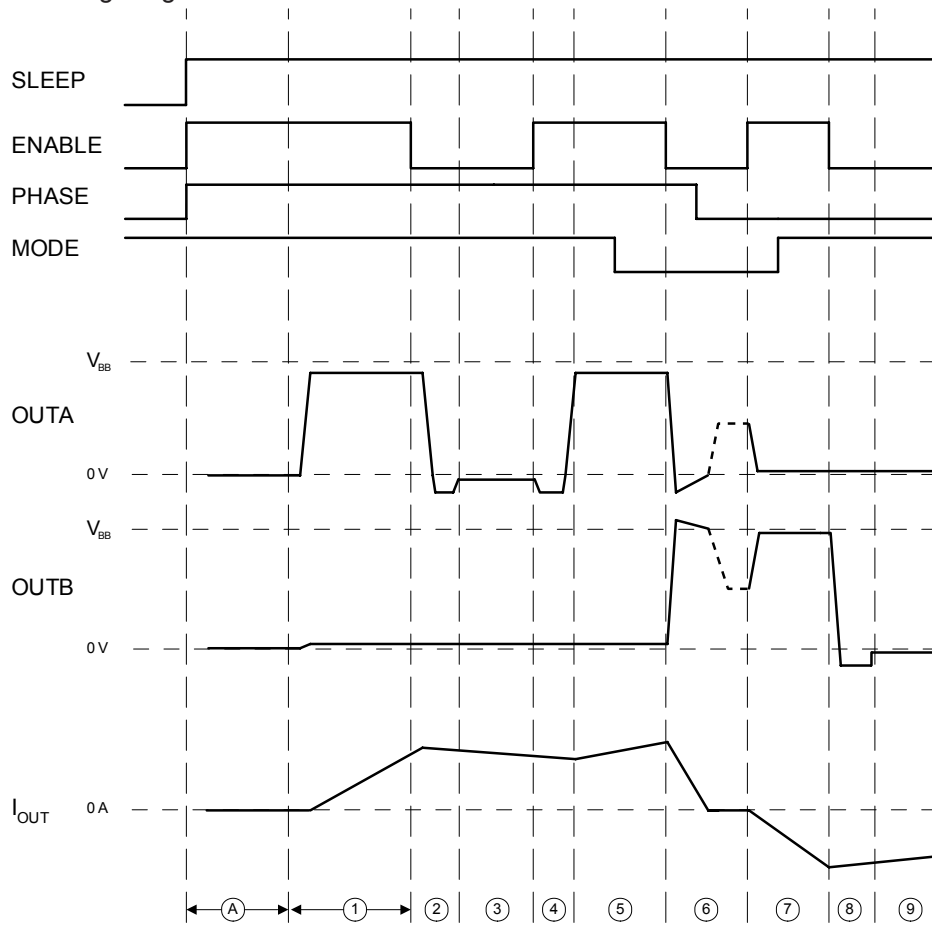
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Output-On Resistance	$R_{\text{DS(on)}}$	Source driver, $I_{\text{OUT}} = -2.8\text{ A}$, $T_J = 25^\circ\text{C}$	–	.4	.48	Ω
		Source driver, $I_{\text{OUT}} = -2.8\text{ A}$, $T_J = 125^\circ\text{C}$	–	.68	–	Ω
		Sink driver, $I_{\text{OUT}} = 2.8\text{ A}$, $T_J = 25^\circ\text{C}$	–	.3	.43	Ω
		Sink driver, $I_{\text{OUT}} = -2.8\text{ A}$, $T_J = 125^\circ\text{C}$	–	.576	–	Ω
Body Diode Forward Voltage	V_F	Source diode, $I_F = -2.8\text{ A}$	–	1.1	1.3	V
		Sink diode, $I_F = 2.8\text{ A}$	–	1	1.3	V
Motor Supply Current	I_{BB}	$f_{\text{PWM}} < 50\text{ kHz}$	–	6	8.5	mA
		Charge pump turned on; outputs disabled	–	3	4.5	mA
		Sleep mode	–	–	10	μA
Logic Input Voltage PHASE, ENABLE, MODE	$V_{\text{IN}(1)}$		2.0	–	–	V
	$V_{\text{IN}(0)}$		–	–	0.8	V
Logic Input Voltage SLEEP	$V_{\text{IN}(1)}$		2.7	–	–	V
	$V_{\text{IN}(0)}$		–	–	0.8	V
Logic Input Current PHASE, MODE pins	$I_{\text{IN}(1)}$	$V_{\text{IN}} = 2.0\text{ V}$	–	< 1.0	20	μA
	$I_{\text{IN}(0)}$	$V_{\text{IN}} = 0.8\text{ V}$	–	< -2.0	–20	μA
Logic Input Current ENABLE pin	$I_{\text{IN}(1)}$	$V_{\text{IN}} = 2.0\text{ V}$	–	40	100	μA
	$I_{\text{IN}(0)}$	$V_{\text{IN}} = 0.8\text{ V}$	–	16	40	μA
Logic Input Current SLEEP pin	$I_{\text{IN}(1)}$	$V_{\text{IN}} = 2.7\text{ V}$	–	27	50	μA
	$I_{\text{IN}(0)}$	$V_{\text{IN}} = 0.8\text{ V}$	–	< 1	10	μA
Propagation Delay Times	t_{pd}	From PWM change to source or sink turn on	–	600	–	ns
		From PWM change to source or sink turn off	–	100	–	ns
Crossover Delay	t_{COD}		–	500	–	ns
Protection Circuitry						
UVLO Enable Threshold		VBB rising	–	6	–	V
UVLO Hysteresis			–	250	–	mV
Thermal Shutdown Temp.	T_J		–	170	–	$^\circ\text{C}$
Thermal Shutdown Hysteresis	ΔT_J		–	15	–	$^\circ\text{C}$

A3949

DMOS Full-Bridge Motor Driver

Data Sheet
29319.47D

PWM Control Timing Diagram



(A) Charge pump and VREG power-up delay (approximately 200 us)

A3949

DMOS Full-Bridge Motor Driver

Functional Description

VREG. This supply voltage is used to operate the sink-side DMOS outputs. VREG is internally monitored and in the case of a fault condition, the outputs of the device are disabled. The VREG pin should be decoupled with a 0.22 μF capacitor to ground.

Charge Pump. The charge pump is used to generate a supply above VBB to drive the source-side DMOS gates. A 0.1 μF ceramic monolithic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1 μF ceramic monolithic capacitor should be connected between VCP and VBB to act as a reservoir to run the high side DMOS devices. The VCP voltage is internally monitored, and in the case of a fault condition, the outputs of the device are disabled.

Shutdown. In the event of a fault due to excessive junction temperature, or low voltage on VCP or VREG, the outputs of the device are disabled until the fault condition is removed. At power-up, the UVLO circuit disables the drivers.

Sleep Mode. Control input SLEEP is used to minimize power consumption when the A3949 is not in use. This disables much of the internal circuitry, including the low-side gate supply and the charge pump. A logic low on this pin puts the device into Sleep mode. A logic high allows normal operation. After coming out of Sleep mode, the user should wait 1 ms before applying PWM signals, to allow the charge pump to stabilize.

Braking. The braking function is implemented by driving the device in slow decay mode via the MODE pin, and applying an enable chop command. Because it is possible to drive current in both directions through the DMOS switches, this configuration effectively shorts out the motor-generated BEMF, as long as the enable chop mode is asserted on the ENABLE pin. The maximum current can be approximated by V_{BEMF} / R_L . Care should be taken to insure that the maximum ratings of the device are not exceeded in worse case braking situations of high speed and high inertial loads.

A3949

DMOS Full-Bridge Motor Driver

Data Sheet
29319.47D

Terminal List Table

Name	Description	Number	
		TSSOP-16	SOIC-16
N/C	Not used	1	1
MODE	Logic input	2	2
PHASE	Logic input for direction control	3	3
GND	Ground	4*	4*
SLEEP	Logic input	5	5
ENABLE	Logic input	6	6
OUTA	Output A for full bridge	7	7
SENSE	Power return	8	8
VBB	Load supply voltage	9	9
OUTB	Output B for full bridge	10	10
CP1	Charge pump capacitor	11	11
CP2	Charge pump capacitor	12	12
GND	Ground	13*	13*
VCP	Reservoir capacitor	14	14
VREG	Low side gate supply decoupler	15	15
N/C	Not used	16	16

*For the TSSOP package, connect pins 4 and 13 to the exposed thermal pad via the PCB layout. In the SOIC package, the pins are internally connected.

[illegible]

A3949

DMOS Full-Bridge Motor Driver

The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro products are not authorized for use as critical components in life-support devices or systems without express written approval.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copyright©2003, 2004 AllegroMicrosystems, Inc.

