

AC'97 Revision 2.1 Audio CODEC with SPDIF Output

DESCRIPTION

WM9707 is a high-quality stereo audio CODEC compliant with the AC'97 Revision 2.1 specification. It performs full duplex 18-bit CODEC functions and supports variable sample rates from 8 to 48k samples/s and offers excellent quality with high SNR. Additional features include 3D sound enhancement, line-level outputs, hardware sample rate conversion, master/slave mode operation and SPDIF output.

WM9707 is interchangeable with AC'97 CODECs from Wolfson and other suppliers. The WM9707 is fully operable on 3.3V or 5V or mixed 3.3/5V supplies, and is packaged in the industry standard 48-lead TQFP package with 7mm body size.

AC'97 FEATURES

- 3.3V or 5V operation
- 18-bit stereo CODEC
- S/N ratio > 95dB
- Multiple stereo input mixer
- Mono and stereo volume control
- 48-lead TQFP package
- Power management features
- Very low standby power
- Variable rate audio (VRA) support
- Analogue 3D stereo enhancement
- Line level outputs
- Supports Rev. 2.1 specified audio sample rates and filtering
- Master/slave ID selection
- PC-beep connection when device held reset
- SPDIF digital output

BLOCK DIAGRAM

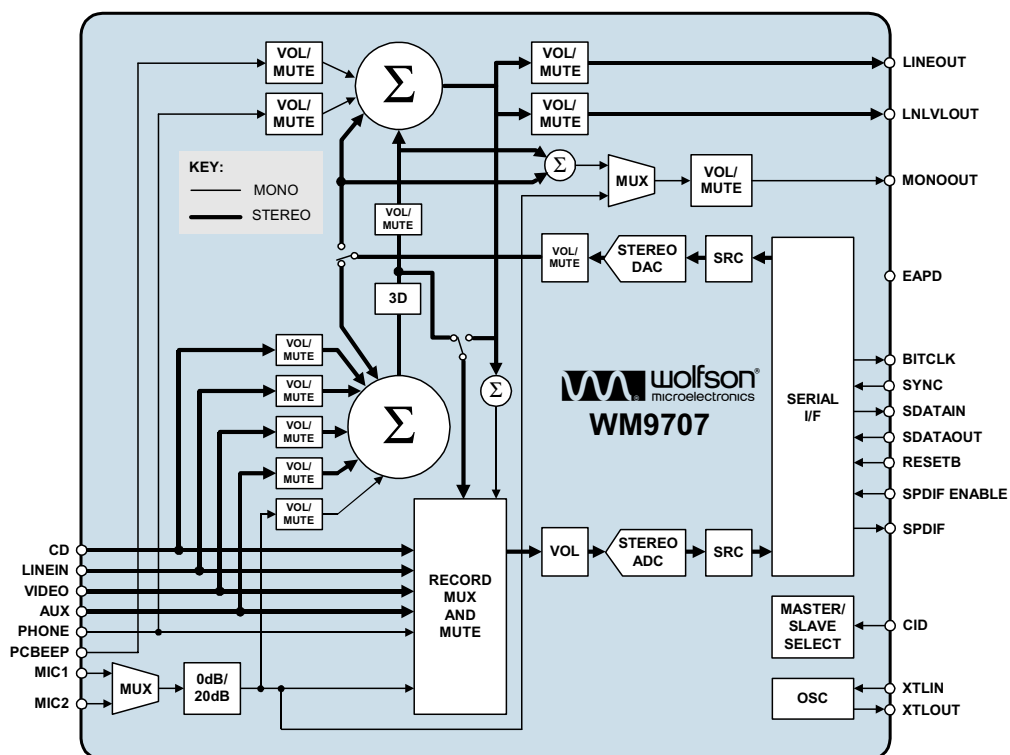
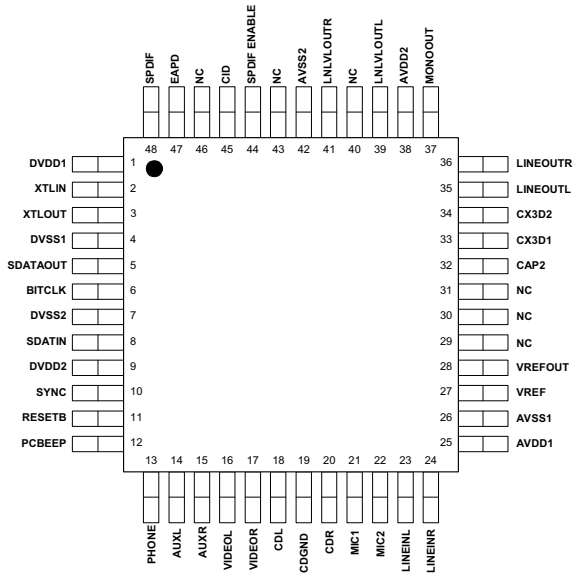


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PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM9707SCFT/V	0 to 70°C	48-lead TQFP (Pb-free)	MSL2	260°C
WM9707SCFT/RV	0 to 70°C	48-lead TQFP (Pb-free, tape and reel)	MSL2	260°C

Note:

Reel quantity = 2,200

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+7V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs	DVSS -0.3V	DVDD +0.3V
Voltage range analogue inputs	AVDD -0.3V	AVDD +0.3V
Operating temperature range, TA	0°C	+70°C
Storage temperature	-65°C	+150°C

Note:

1. The digital supply voltage (DVDD) must always be less than or equal to the analogue supply voltage (AVDD).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD1, DVDD2		-10%	3.3 to 5.0	+10%	V
Analogue supply range	AVDD1, AVDD2		-10%	3.3 to 5.0	+10%	V
Digital ground	DVSS1, DVSS2			0		V
Analogue ground	AVSS1, AVSS2			0		V
Difference DVSS to AVSS			-0.3	0	+0.3	V
Analogue supply current		DVDD, AVDD = 5V		30		mA
Digital supply current		DVDD, AVDD = 5V		16		mA
Standby supply current (all PRs set)		DVDD, AVDD = 5V		10		uA
Analogue supply current		DVDD, AVDD = 3.3V		16		mA
Digital supply current		DVDD, AVDD = 3.3V		11		mA
Standby supply current (all PRs set)		DVDD, AVDD = 3.3V		10		uA

Note:

- Both supplies should be powered on and off at the same time.

ELECTRICAL CHARACTERISTICS

Test Characteristics:

AVDD = 5V, GND = 0V $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, unless otherwise stated

DVDD = 3.3V, GND = 0V $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (DVDD = 3.3 or 5.0V)						
Input LOW level	V_{IL}		AVSS -0.3		0.8	V
Input HIGH level	V_{IH}		2.2		AVDD +0.3	V
Output LOW	V_{OL}	$I_{OL} = 1\text{mA}$			$0.10 \times V_{DD}$	V
Output HIGH	V_{OH}	$I_{OL} = 1\text{mA}$	$0.90 \times V_{DD}$			V
Analogue I/O Levels (Input Signals on any inputs, Outputs on LINEOUT L, R and MONOOUT)						
Input level		Minimum input impedance = 10k	AVSS -100mV		AVDD +100mV	V
Output level		Into 10kΩ load	AVSS +300mV	Near rail to rail	AVDD -300mV	V
Reference Levels						
Reference input/output	CAP2		2/5 AVDD	AVDD/2	3/5 AVDD	V
CAP2 impedance				75		kΩ
Mixer reference	VREF			Buffered CAP2		V
MIC reference	VREFOUT			Buffered CAP2		V
MIDBUFF current sink (pins VREF and VREFOUT)		AVDD = 5V	-5	-15		mA
MIDBUFF current source (pins VREF and VREFOUT)		AVDD = 5V	5	15		mA
MIDBUFF current source (pins VREF and VREFOUT)		AVDD = 3.3V		10		mA
MIDBUFF current sink (pins VREF and VREFOUT)		AVDD = 3.3V		-10		mA

Test Characteristics:AVDD = 5V, GND = 0VT_A = 0°C to +70°C, unless otherwise statedDVDD = 3.3V, GND = 0VT_A = 0°C to +70°C, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Circuit Specifications (AVDD = 5V) 48kHz sampling						
SNR A-weighted (Note 1)			85	95		dBv
Full scale output voltage		VREF = 2.5V		1.0		V _{rms}
THD		-3dBfs input	74 (0.02%)	-90		dBv
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Out of band rejection				-40		dB
Spurious tone reduction				-100		dB
PSRR		20 to 20kHz		40		dB
ADC Circuit Specifications (AVDD = 5V) 48kHz sampling						
SNR A-weighted (Note 1)			75	90		dB
ADC input for full scale output		VREF = 2.5V		1.0		V _{rms}
THD		-6dBv input	74	-85		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Stop band rejection			-74			dB
PSRR		20 to 20kHz		40		dB
Mixer Circuit Specifications (AVDD = 5V) 48kHz sampling						
SNR CD path A-weighted (Note 1)			90	100		dB
SNR Other paths A-weighted (Note 1)			85	95		dB
Maximum input voltage			AVSS	1.0	AVDD	V _{rms}
Maximum output voltage on LINEOUT			1.0	1.8		V _{rms}
THD		0dBv input	74	-90		dB
Frequency response (+/-1dB)			20		20,000	Hz
Input impedance (CD inputs)		At any gain		15		kΩ
Input impedance (other mixer inputs)		At max gain	10	20		kΩ
		At 0db gain	50	100		kΩ
Input impedance MIC inputs		At max gain	10	30		kΩ
		At 0db gain	55	110		kΩ
PSRR		20 to 20kHz		50		dB
DAC Circuit Specifications (AVDD = 3.3V) 48kHz sampling						
SNR A-weighted (Note 1)				92		dB
Full scale output voltage		VREF = 1.65V		0.7		V _{rms}
THD		-3dBFS input		-85		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Out of band rejection				-40		dB
Spurious tone reduction				-100		dB
PSRR		20 to 20kHz		40		dB

Test Characteristics:AVDD = 5V, GND = 0VT_A = 0°C to +70°C, unless otherwise statedDVDD = 3.3V, GND = 0VT_A = 0°C to +70°C, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Circuit Specifications (AVDD = 3.3V) 48kHz sampling						
SNR A-weighted (Note 1)				85		dB
ADC input for full scale output		VREF = 1.65V		0.7		V _{rms}
THD		-6dBv input		80		dB
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Stop band rejection			-74			dB
PSRR		20 to 20kHz		40		dB
Mixer Circuit Specifications (AVDD = 3.3V) 48kHz sampling						
SNR CD path A-weighted (Note 1)				95		dB
SNR Other paths A-weighted (Note 1)				90		dB
Maximum input voltage				0.6		V _{rms}
Maximum output voltage on LINEOUT				1.2		V _{rms}
THD (Note 2)		-3.6dBv input		85		dBv
Frequency response (+/-1dB)			20		20,000	Hz
Input impedance (CD inputs)		At any gain		15		kΩ
Input impedance (other Mixer inputs)		At max gain		20		kΩ
		At 0db gain		100		kΩ
Input impedance MIC inputs		At max gain		30		kΩ
		At 0db gain		110		kΩ
PSRR		20 to 20kHz		50		dB
Clock Frequency Range						
Crystal clock				24.576		MHz
BITCLK frequency				12.288		MHz
SYNC frequency				48.0		kHz

Notes:

1. SNR is the ratio of 0dB signal output to the output level with no signal, measured A-weighted over a 20Hz to 20kHz bandwidth.
2. Inputs are scaled for AVDD eg; 0dBv at 5.0V is equivalent to -3.6dBv at 3.3V.

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DVDD1	Supply	Digital positive supply
2	XTLIN	Digital input	Clock crystal connection or clock input (XTAL not used)
3	XTLOUT	Digital output	Clock crystal connection
4	DVSS1	Supply	Digital ground supply
5	SDATAOUT	Digital input	Serial data input
6	BITCLK	Digital output (master) Digital input (slave)	Serial interface clock output to AC'97 controller or input from AC'97 master CODEC
7	DVSS2	Supply	Digital ground supply
8	SDATAIN	Digital output	Serial data output to AC'97 controller
9	DVDD2	Supply	Digital positive supply
10	SYNC	Digital input	Serial interface sync pulse from AC'97 controller
11	RESETB	Digital input	NOT reset input (active low, resets registers)
12	PCBEEP	Analogue input	Mixer input, typically for PCBEEP signal
13	PHONE	Analogue input	Mixer input, typically for PHONE signal
14	AUXL	Analogue input	Mixer input, typically for AUX signal
15	AUXR	Analogue input	Mixer input, typically for AUX signal
16	VIDEOL	Analogue input	Mixer input, typically for VIDEO signal
17	VIDEOR	Analogue input	Mixer input, typically for VIDEO signal
18	CDL	Analogue input	Mixer input, typically for CD signal
19	CDGND	Analogue input	CD input common mode reference (ground)
20	CDR	Analogue input	Mixer input, typically for CD signal
21	MIC1	Analogue input	Mixer input with extra gain if required
22	MIC2	Analogue input	Mixer input with extra gain if required
23	LINEINL	Analogue input	Mixer input, typically for LINE signal
24	LINEINR	Analogue input	Mixer input, typically for LINE signal
25	AVDD1	Supply	Analogue positive supply
26	AVSS1	Supply	Analogue ground supply, chip substrate
27	VREF	Analogue output	Buffered CAP2
28	VREFOUT	Analogue output	Reference for microphones; buffered CAP2
29	NC		No internal connection
30	NC		No internal connection
31	NC		No internal connection
32	CAP2	Analogue input	Reference input/output; pulls to midrail if not driven
33	CX3D1	Analogue output	Output pin for 3D difference signal
34	CX3D2	Analogue input	Input pin for 3D difference signal
35	LINEOUTL	Analogue output	Main analogue output for left channel
36	LINEOUTR	Analogue output	Main analogue output for right channel
37	MONOOUT	Analogue output	Main mono output
38	AVDD2	Supply	Analogue positive supply
39	LNLVLOUTL	Analogue output	Left channel line level output
40	NC		No internal connection
41	LNLVLOUTR	Analogue output	Right channel line level output
42	AVSS2	Supply	Analogue ground supply, chip substrate
43	NC		No internal connection
44	SPDIF ENABLE	Digital input	SPDIF ENABLE (internal pull-down)
45	CID	Digital input	Master/slave ID select (internal pull-up), Hi = master
46	NC		No internal connection
47	EAPD	Digital output	External amplifier powerdown/GPO
48	SPDIF	Digital output	SPDIF digital audio data output

DETAILED TIMING DIAGRAMS

Test Characteristics:

AVDD = 5V, GND = 0V $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, unless otherwise stated.

DVDD = 3.3V, GND = 0V $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, unless otherwise stated.

All measurements are taken at 10% to 90% VDD, unless otherwise stated. All the following timing information is guaranteed, not tested.

AC-LINK LOW POWER MODE

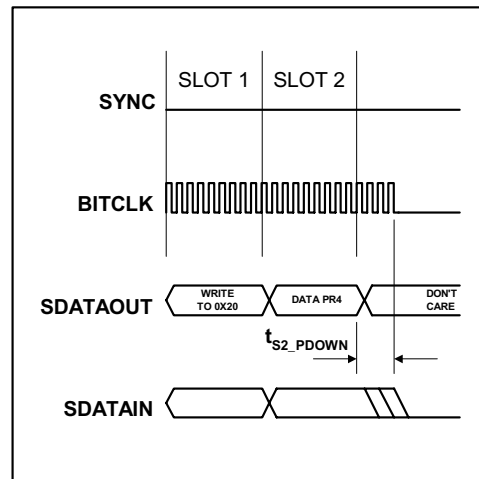


Figure 1 AC-Link Powerdown Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
End of slot 2 to BITCLK SDATIN low	t_{S2_PDOWN}			1.0	μs

COLD RESET

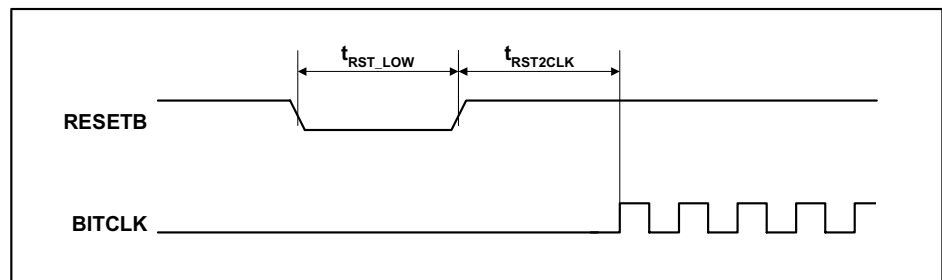


Figure 2 Cold Reset Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
RESETB active low pulse width	t_{RST_LOW}	1.0			μs
RESETB inactive to BITCLK startup delay	t_{RST2_CLK}	162.8			ns

WARM RESET

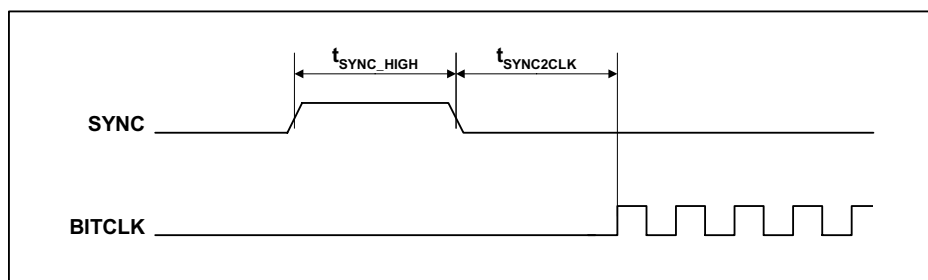


Figure 3 Warm Reset Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SYNC active high pulse width	$t_{\text{SYNC_HIGH}}$		1.3		μs
SYNC inactive to BITCLK startup delay	$t_{\text{SYNC2_CLK}}$	162.4			ns

CLOCK SPECIFICATIONS

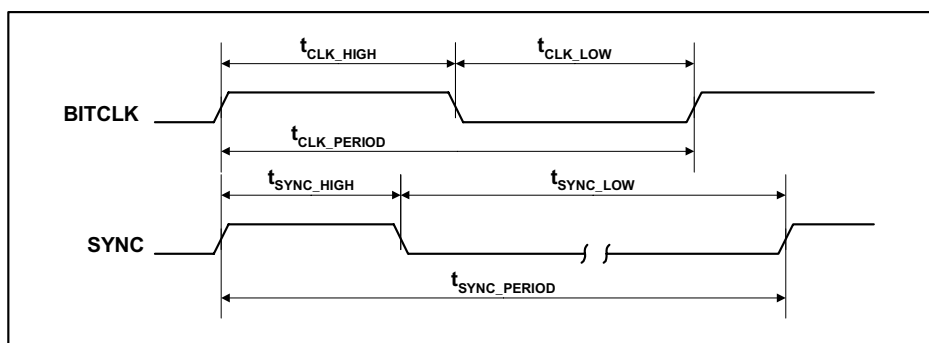


Figure 4 Clock Specifications (50pF External Load)

Note: Worst case duty cycle restricted to 40/60.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BITCLK frequency			12.288		MHz
BITCLK period	$t_{\text{CLK_PERIOD}}$		81.4		ns
BITCLK output jitter (See Note)				750	ps
BITCLK high pulse width (See Note)	$t_{\text{CLK_HIGH}}$	32.56	40.7	48.84	ns
BITCLK low pulse width (See Note)	$t_{\text{CLK_LOW}}$	32.56	40.7	48.84	ns
SYNC frequency			48.0		kHz
SYNC period	$t_{\text{SYNC_PERIOD}}$		20.8		μs
SYNC high pulse width	$t_{\text{SYNC_HIGH}}$		1.3		μs
SYNC low pulse width	$t_{\text{SYNC_LOW}}$		19.5		μs

DATA SETUP AND HOLD (50pF EXTERNAL LOAD)

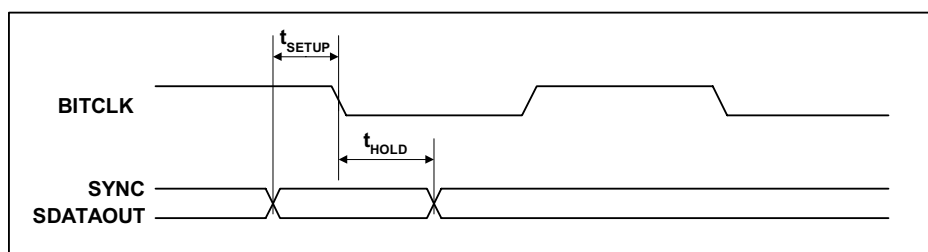


Figure 5 Data Setup and Hold (50pF External Load)

Note: Setup and hold time parameters for SDATAIN are with respect to AC'97 Controller.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Setup to falling edge of BITCLK	t_{SETUP}	15.0			ns
Hold from falling edge of BITCLK	t_{HOLD}	5.0			ns

SIGNAL RISE AND FALL TIMES

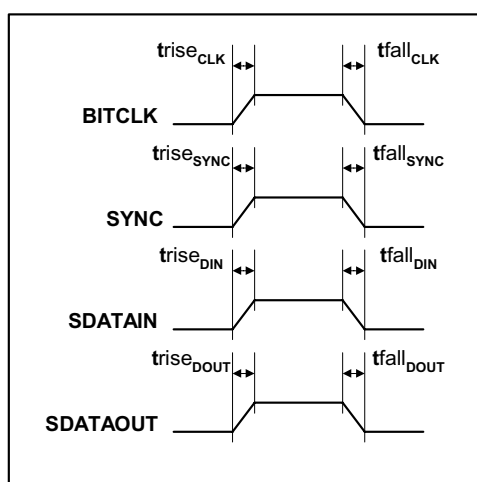


Figure 6 Signal Rise and Fall Times (50pF External Load)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BITCLK rise time	$trise_{\text{CLK}}$	2		6	ns
BITCLK fall time	$tfall_{\text{CLK}}$	2		6	ns
SYNC rise time	$trise_{\text{SYNC}}$	2		6	ns
SYNC fall time	$tfall_{\text{SYNC}}$	2		6	ns
SDATAIN rise time	$trise_{\text{DIN}}$	2		6	ns
SDATAIN fall time	$trise_{\text{DIN}}$	2		6	ns
SDATAOUT rise time	$trise_{\text{DOUT}}$	2		6	ns
SDATAOUT fall time	$tfall_{\text{DOUT}}$	2		6	ns

The diagram illustrates the internal architecture of the WM9707 AC97 rev2.1 Codec. Key components and their connections include:

- Serial Interface:** Manages data flow between the DAC Audio Data and the DAC Decimation filters. It includes a DAC and an ADC, with programmable I/O supports for surround channels.
- DAC Decimation filters:** Process the DAC Audio Data into SRC control reg 32h, which then feeds into the ADC Decimation filters.
- Variable Rate Audio Support:** Provides SRC control reg 20h to the DAC Interpolation Filters.
- Digital Sigma Delta Modulators:** Convert digital data into analog signals, outputting to the DAC Interpolation Filters.
- DAC Interpolation Filters:** Filter the analog signals from the Digital Sigma Delta Modulators and the DAC Decimation filters.
- PGA (Programmable Gain Amplifier) blocks:** Multiple PGA blocks (e.g., PGA Reg 10h, PGA Reg 12h, PGA Reg 14h, PGA Reg 16h, PGA Reg 18h, PGA Reg 19h, PGA Reg 20h, PGA Reg 21h, PGA Reg 22h, PGA Reg 23h, PGA Reg 24h, PGA Reg 25h, PGA Reg 26h, PGA Reg 27h, PGA Reg 28h, PGA Reg 29h, PGA Reg 30h, PGA Reg 31h, PGA Reg 32h, PGA Reg 33h, PGA Reg 34h, PGA Reg 35h, PGA Reg 36h, PGA Reg 37h, PGA Reg 38h, PGA Reg 39h, PGA Reg 40h, PGA Reg 41h, PGA Reg 42h, PGA Reg 43h, PGA Reg 44h, PGA Reg 45h, PGA Reg 46h, PGA Reg 47h, PGA Reg 48h, PGA Reg 49h, PGA Reg 50h, PGA Reg 51h, PGA Reg 52h, PGA Reg 53h, PGA Reg 54h, PGA Reg 55h, PGA Reg 56h, PGA Reg 57h, PGA Reg 58h, PGA Reg 59h, PGA Reg 60h, PGA Reg 61h, PGA Reg 62h, PGA Reg 63h, PGA Reg 64h, PGA Reg 65h, PGA Reg 66h, PGA Reg 67h, PGA Reg 68h, PGA Reg 69h, PGA Reg 70h, PGA Reg 71h, PGA Reg 72h, PGA Reg 73h, PGA Reg 74h, PGA Reg 75h, PGA Reg 76h, PGA Reg 77h, PGA Reg 78h, PGA Reg 79h, PGA Reg 80h, PGA Reg 81h, PGA Reg 82h, PGA Reg 83h, PGA Reg 84h, PGA Reg 85h, PGA Reg 86h, PGA Reg 87h, PGA Reg 88h, PGA Reg 89h, PGA Reg 90h, PGA Reg 91h, PGA Reg 92h, PGA Reg 93h, PGA Reg 94h, PGA Reg 95h, PGA Reg 96h, PGA Reg 97h, PGA Reg 98h, PGA Reg 99h, PGA Reg 100h, PGA Reg 101h, PGA Reg 102h, PGA Reg 103h, PGA Reg 104h, PGA Reg 105h, PGA Reg 106h, PGA Reg 107h, PGA Reg 108h, PGA Reg 109h, PGA Reg 110h, PGA Reg 111h, PGA Reg 112h, PGA Reg 113h, PGA Reg 114h, PGA Reg 115h, PGA Reg 116h, PGA Reg 117h, PGA Reg 118h, PGA Reg 119h, PGA Reg 120h, PGA Reg 121h, PGA Reg 122h, PGA Reg 123h, PGA Reg 124h, PGA Reg 125h, PGA Reg 126h, PGA Reg 127h, PGA Reg 128h, PGA Reg 129h, PGA Reg 130h, PGA Reg 131h, PGA Reg 132h, PGA Reg 133h, PGA Reg 134h, PGA Reg 135h, PGA Reg 136h, PGA Reg 137h, PGA Reg 138h, PGA Reg 139h, PGA Reg 140h, PGA Reg 141h, PGA Reg 142h, PGA Reg 143h, PGA Reg 144h, PGA Reg 145h, PGA Reg 146h, PGA Reg 147h, PGA Reg 148h, PGA Reg 149h, PGA Reg 150h, PGA Reg 151h, PGA Reg 152h, PGA Reg 153h, PGA Reg 154h, PGA Reg 155h, PGA Reg 156h, PGA Reg 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Figure 7 Functional Block Diagram

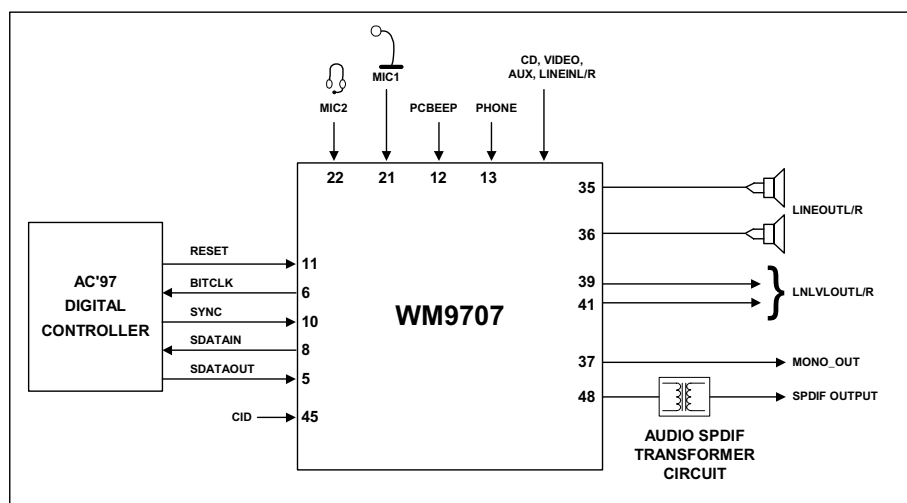


Figure 8 Revision 2.1 Compliant 2-Channel CODEC

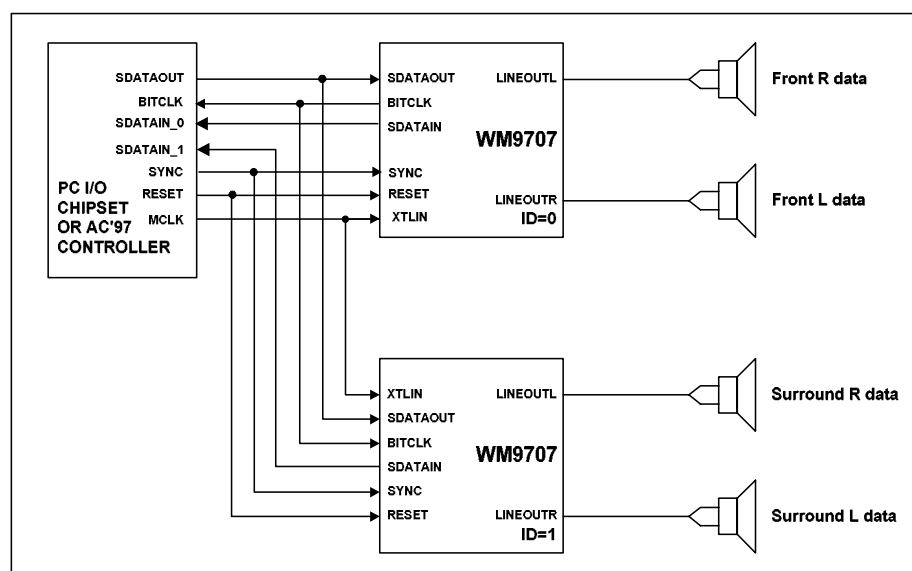


Figure 9 WM9707 in a 4 Channel System

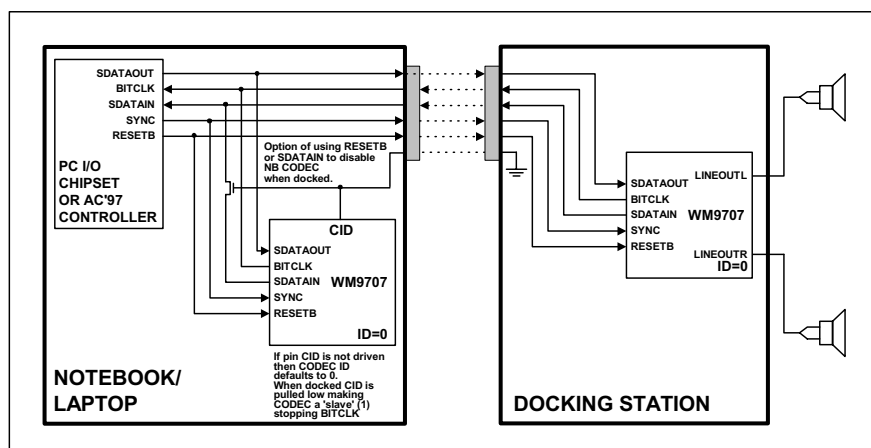


Figure 10 WM9707 in a Docking Station System

DEVICE DESCRIPTION

INTRODUCTION

The WM9707 is fully compliant with Revision 2.1 of the AC'97 specification.

The WM9707 comprises a stereo 18-bit CODEC, (that is, 2 ADCs and 2 DACs) a comprehensive analogue mixer with 4 sets of stereo inputs, phone, 2 microphone, and PC-beep inputs. Additionally, on-chip reference generation circuits generate the necessary bias voltages for the device, and a bidirectional serial interface allows transfer of control data and DAC and ADC words to and from the AC'97 controller. The WM9707 supports 18-bit resolution within the DAC and ADC functions, but the AC'97 serial interface specification allows any word length up to 20-bits to be written to, or read from, the AC'97 CODEC. These words are MSB justified, and any LSBs not used will simply default to 0. Normally it is anticipated that 16-bit words will be used in most PC type systems. Therefore, for the DAC, 16-bit words will be downloaded into the CODEC from the controller, along with padding of 0s to make the 16-bit word up to 20-bit length. In this case, the WM9707 will process the 16-bit word along with 0 padding bits in the 2 LSB locations (to make 18-bit). At the ADC output, WM9707 will provide an 18-bit word, again with 0s in the two LSB locations (20-bit). The AC'97 controller will then ignore the 4 LSBs of the 20-bit word. When the WM9707 is interrogated at Register 00h, it responds indicating it is an 18-bit device.

The WM9707 has the ADC and DAC functions implemented using oversampled, or sigma-delta converters, and uses on-chip digital filters to convert these 1-bit signals to and from the 48ks/s 16/18-bit PCM words that the AC'97 controller requires. The digital parts of the device are powered separately from the analogue to optimise performance, and 3.3V digital and 5V analogue supplies may be used on the same device to further optimise performance. Digital IOs are 5V tolerant when the analogue supplies are 5V, so the WM9707 may be connected to a controller running on 5V supplies, but use 3.3V for the digital section of WM9707. WM9707 is also capable of operating with a 3.3V supply only (digital and analogue).

An internally generated midrail reference is provided at pin CAP2 which is used as the chip reference. This pin should be heavily decoupled. Refer to Figure 18 for more details.

The WM9707 is not limited to PC-only applications. The ability to power down sections of the device selectively, and the option to choose alternative master clock, and hence sample rates, means that many alternative applications in areas such as telecomms, may be anticipated.

Additional features added to the Intel AC'97 specification, such as the EAPD (External Amplifier Powerdown) bit, internal connection of PC-beep to the outputs in the case where the device is reset, are supported, along with optional features such as variable sample rate support and SPDIF output.

3D STEREO ENHANCEMENT

This device contains a stereo enhancement circuit, designed to optimise the listening experience when the device is used in a typical PC operating environment. That is, with a pair of speakers placed either side of the monitor with little spatial separation. This circuit creates a difference signal by differencing left and right channel playback data, then filters this difference signal using lowpass and highpass filters whose time constants are set using external capacitors connected to the CX3D pins 33 and 34. Typically the values of 100nF and 47nF set highpass and lowpass poles at about 100Hz and 1kHz respectively. This frequency band corresponds to the range over which the ear is most sensitive to directional effects.

The filtered difference signal is gain adjusted by an amount set using the 4-bit value written to Register 22h bits 3 to 0. Value 0h is disable, value Fh is maximum effect. Typically a value of 8h is optimum. The user interface would most typically use a slider type of control to allow the user to adjust the level of enhancement to suit the program material. Bit D13 3D in Register 20h is the overall 3D enable bit. The capability Register 00h reads back the value 11000 in bits D14 to D10. This corresponds to decimal 24, which is registered with Intel as Wolfson Stereo Enhancement.

Note that the external capacitors setting the filtering poles applied to the difference signal may be adjusted in value, or even replaced with a direct connection between the pins. If such adjustments are made, then the amount of difference signal fed back into the main signal paths may be significant, and can cause large signals which may limit, distort, or overdrive signal paths or speakers. Adjust these values with care, to select the preferred acoustic effect.

There is no provision for pseudo-stereo effects. Mono signals will have no enhancement applied (if the signals are in phase and of the same amplitude).

Signals from the PCM DAC channels can have stereo enhancement applied. It can also be bypassed if desired. This control is enabled by setting the POP bit in Register 20h.

VARIABLE SAMPLE RATE SUPPORT

The DACs and ADCs on this device support all the recommended sample rates specified in the Intel Revision 2.1 specification for audio rates. The default rate is 48ks/s. If alternative rates are selected and variable rate audio is enabled (Register 2Ah, bit 0), the AC'97 interface continues to run at 48k words per second, but data is transferred across the link in bursts such that the net sample rate selected is achieved. It is up to the AC'97 Revision 2.1 compliant controller to ensure that data is supplied to the AC link, and received from the AC link, at the appropriate rate.

The device supports on demand sampling. That is, when the DAC signal processing circuits need another sample, a sample request is sent to the controller which must respond with a data sample in the next frame it sends. For example, if a rate of 22.05ks/s is selected, on average the device will request a sample from the controller every other frame, for each of the stereo DACs. Note that if an unsupported rate is written to one of the rate registers, the rate will default to the nearest rate supported. The Register will then respond when interrogated with the supported rate the device has defaulted to.

The left and right channels of the ADCs and DACs always sample at the same rate.

AUDIO SAMPLE RATE (HZ)	CONTROL VALUE D15-D0 (HEX)
8000	1F40
11025	2B11
16000	3E80
22050	5622
32000	7D00
44100	AC44
48000	BB80

Table 1 Variable Sample Rates Supported

SPDIF DIGITAL AUDIO DATA OUTPUT

Pin 48 may be used to output the PCM DAC playback data in SPDIF (IEC958) digital data format. In order to enable this output, bit SPDF in Register 5Ch should be set or pin 44 pulled high. Additionally, a bit SCMS in Register 5Ch may also be set, which removes the copyright flag in the IEC958 data, allowing serial copy protect mechanisms to be implemented. Note that this data output will only operate at the SYNCH rate and so only supports 48ks/s operation. The PCM DACs continue to function normally when SPDIF output is enabled.

GAIN CONTROL REGISTER LOCATION

PGA	CONTROL REGISTER	MUTE DEFAULT
DAC	18h	Muted (bit-15)
Mixer	72h	Not-muted (bit-15)
Volume	02h	Muted (15)

Table 2 Gain Control Register Location

MASTER/SLAVE ID SUPPORT

WM9707 supports operation as either a master or a slave CODEC. Configuration of the device as either a master or as a slave, is selected by tying the CID pin 45 on the package.

Fundamentally, a device identified as a master (ID = 0) produces BITCLK as an output, whereas a slave (any other ID) must be provided with BITCLK as an input. This has the obvious implication that if the master device on an AC link is disabled, the slave devices cannot function.

The AC'97 Revision 2.1 specification defines that the CID pin has inverting sense, and are provided with internal weak pull ups. Therefore, if no connections are made to the CID pin, then the pin pulls hi and an ID = 0 is selected, i.e. master. External connects to ground will select other IDs.

PIN 45 CID	ID SELECTED	MASTER OR SLAVE	BITCLK
NC	0	Master	Output
Ground	1	Slave	Input

Table 3 ID Selection

CONTROL INTERFACE

A digital interface has been provided to control the WM9707 and transfer data to and from it. This serial interface is compatible with the Intel AC'97.

The main control interface functions are:

- Control of analogue gain and signal paths through the mixer
- Bi-directional transfer of ADC and DAC words to and from AC'97 controller
- Selection of Powerdown down modes.

AC-LINK DIGITAL SERIAL INTERFACE PROTOCOL

The WM9707 incorporates a 5-pin digital serial interface that links it to the AC'97 controller. AC-link is a bi-directional, fixed rate, serial PCM digital stream. It handles multiple input and output audio streams, as well as control Register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. With a minimum required DAC and ADC resolution of 16-bits, AC'97 may also be implemented with 18 or 20-bit DAC/ADC resolution, given the headroom that the AC-link architecture provides. The WM9707 provides support for 18-bit operation.

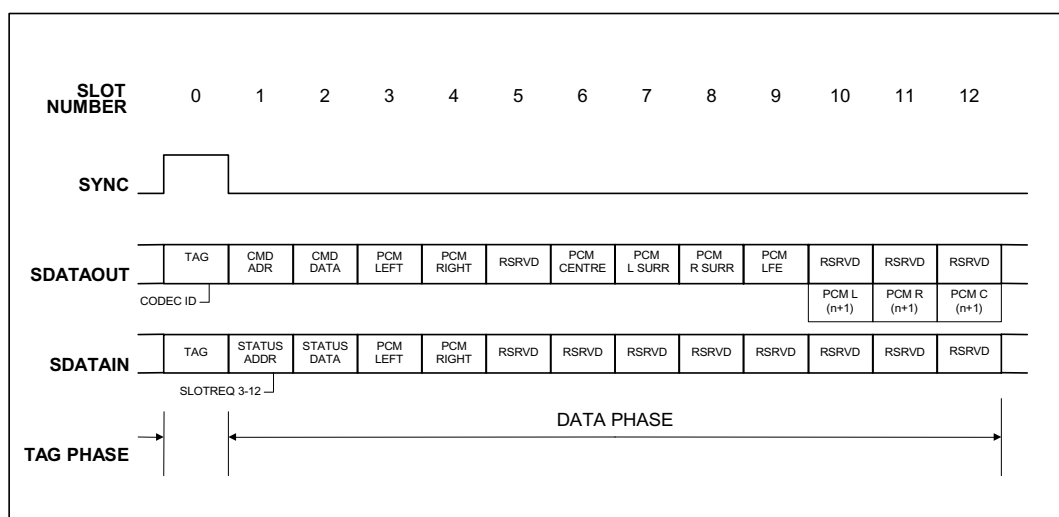


Figure 11 AC'97 Standard Bi-Directional Audio Frame

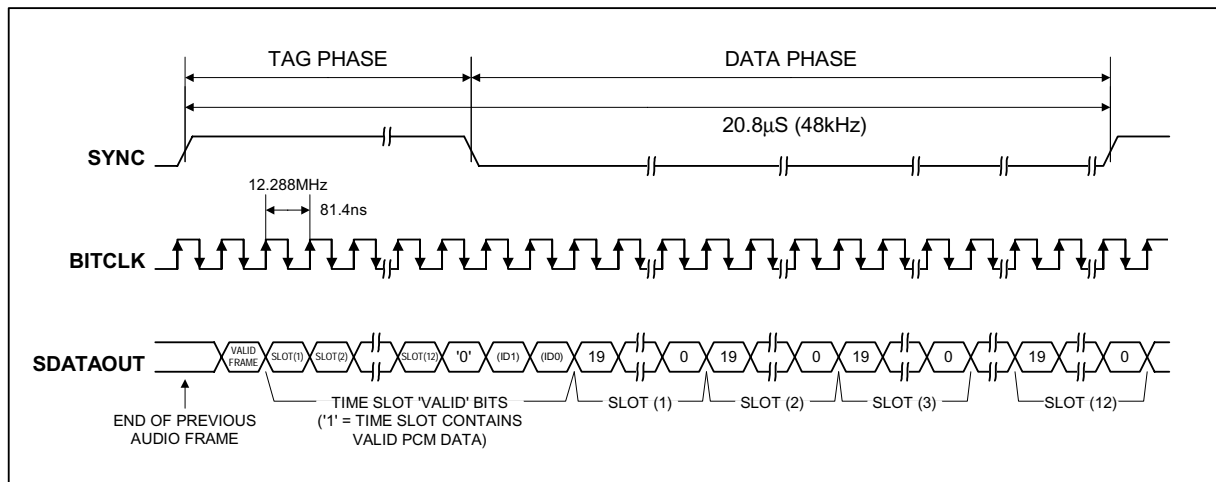


Figure 12 AC-link Audio Output Frame

The datastreams currently defined by the AC'97 specification include:

PCM playback - 2 output slots	2-channel composite PCM output stream
PCM record data - 2 input slots	2-channel composite PCM input stream
Control - 2 output slots	Control Register write port
Status - 2 input slots	Control Register read port
Optional modem line CODEC output - 1 output slot	Modem line CODEC DAC input stream
Optional modem line CODEC input - 1 input slot	Modem line CODEC ADC output stream
Optional dedicated microphone input - 1 input slot	Dedicated microphone input stream in support of stereo AEC and/or other voice applications.

Synchronisation of all AC-link data transactions is signalled by the WM9707 controller. The WM9707 drives the serial bit clock onto AC-link, which the AC'97 controller then qualifies with a synchronisation signal to construct audio frames.

SYNC, fixed at 48kHz, is derived by dividing down the serial clock (BITCLK). BITCLK, fixed at 12.288MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BITCLK. The receiver of AC-link data, (WM9707 for outgoing data and AC'97 controller for incoming data), samples each serial bit on the falling edges of BITCLK.

The AC-link protocol provides for a special 16-bit time slot (slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is tagged invalid, it is the responsibility of the source of the data, (the WM9707 for the input stream, AC'97 controller for the output stream), to stuff all bit positions with 0s during that slot's active time.

SYNC remains high for a total duration of 16 BITCLKs at the beginning of each audio frame.

The portion of the audio frame where SYNC is high is defined as the Tag Phase. The remainder of the audio frame where SYNC is low is defined as the Data Phase. Additionally, for power savings, all clock, sync, and data signals can be halted. This requires that the WM9707 be implemented as a static design to allow its register contents to remain intact when entering a power savings mode.

AC-LINK AUDIO OUTPUT FRAME (SDATAOUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the WM9707's DAC inputs, and control registers. As briefly mentioned earlier, each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16-bits, which are used for AC-link protocol infrastructure.

OUTPUT TAG SLOT (16-BITS)

Bit (15)	Frame Valid	
Bit (14)	Slot 1 Valid Command Address bit	(Primary CODEC only)
Bit (13)	Slot 2 Valid Command Data bit	(Primary CODEC only)
Bit (12:3)	Slot 3-12 Valid bits as defined by AC'97	
Bit 2	Reserved	(Set to 0)
Bit (1:0)	2-bit Message ID field	(00 reserved for Primary; 01 indicates Secondary)

Within slot 0 the first bit is a global bit (SDATAOUT slot 0, bit 15) which flags the validity for the entire audio frame. If the Valid Frame bit is a 1, this indicates that the current audio frame contains at least one time slot of valid data. The next 12-bit positions sampled by the WM9707 indicate which of the corresponding 12 time slots contain valid data.

In this way data streams of differing sample rates can be transmitted across AC-link at its fixed 48kHz audio frame rate. Figure 12 illustrates the time slot based AC-link protocol.

When the CODEC is a slave device, bits 14 and 13 are not used to validate data in slots 1 and 2. Instead, if the message ID bits (1:0) match the CODEC ID then the address is valid and bit 19 from slot 1 then indicates if slot 2 is valid.

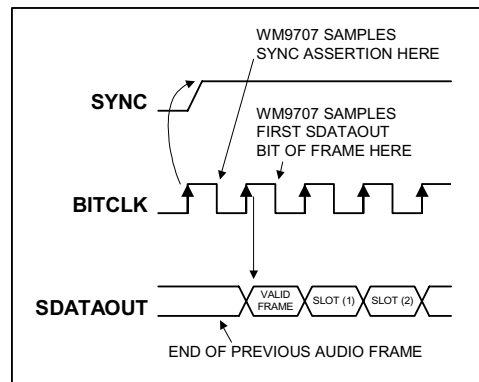


Figure 13 Start of an Audio Output Frame

A new audio output frame begins with a low to high transition of SYNC as shown in Figure 13. SYNC is synchronous to the rising edge of BITCLK. On the immediately following falling edge of BITCLK, the WM9707 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising edge of BITCLK, AC'97 transitions SDATAOUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BITCLK, and subsequently sampled by the WM9707 on the following falling edge of BITCLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

Baseline AC'97 specified audio functionality MUST ALWAYS sample rate convert to and from a fixed 48ks/s on the AC'97 controller. This requirement is necessary to ensure that interoperability between the AC'97 controller and the WM9707, among other things, can be guaranteed by definition for baseline specified AC'97 features.

SDATAOUT's composite stream is MSB justified (MSB first) with all non-valid slot bit positions stuffed with 0s by the AC'97 controller.

In the event that there are less than 20 valid bits within an assigned and valid time slot, the AC'97 controller always stuffs all trailing non-valid bit positions of the 20-bit slot with 0s.

As an example, consider an 8-bit sample stream that is being played out to one of the WM9707's DACs. The first 8 bit positions are presented to the DAC (MSB justified) followed by the next 12 bit positions, which are stuffed with 0s by the AC'97 controller. This ensures that regardless of the resolution of the implemented DAC (16, 18 or 20-bit), no DC biasing will be introduced by the least significant bits.

When mono audio sample streams are output from the AC'97 controller, it is necessary that BOTH left and right sample stream time slots be filled with the same data.

SLOT 1: COMMAND ADDRESS PORT

The command port is used to control features, and monitor status for the WM9707 functions including, but not limited to, mixer settings, and power management (refer to the Serial Interface Register Map). The control interface architecture supports up to 64, 16-bit read/write registers, addressable on even byte boundaries. Only the even Registers (00h, 02h, etc.) are valid. Odd register read/write will have no effect on the WM9707.

Audio output frame slot 1 communicates control register address, and read/write command information to the WM9707.

COMMAND ADDRESS PORT BIT ASSIGNMENTS

Bit (19)	Read/write command (1 = read, 0 = write)
Bit (18:12)	Control register index (64 16-bit locations, addressed on even byte boundaries)
Bit (11:0)	Reserved (stuffed with 0s)

The first bit (MSB) sampled by the WM9707 indicates whether the current control transaction is a read or write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0s by the AC'97 controller.

SLOT 2: COMMAND DATA PORT

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle. (As indicated by slot 1, bit 19).

Bit (19:4)	Control register write data (stuffed with 0s if current operation is a read)
Bit (3:0)	Reserved (stuffed with 0s)

If the current command port operation is a read then the entire time slot must be stuffed with 0s by the AC'97 controller.

SLOT 3: PCM PLAYBACK LEFT CHANNEL

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical Games Compatible PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0s.

SLOT 4: PCM PLAYBACK RIGHT CHANNEL

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical Games Compatible PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples.

If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0s.

SLOT 5: OPTIONAL MODEM LINE CODEC

Audio output frame slot 5 contains the MSB justified modem DAC input data. This optional AC'97 feature is not supported in the WM9707, and if data is written to this location it is ignored. This may be determined by the AC'97 controller interrogating the WM9707 Vendor ID registers.

SLOTS 6 TO 9: SURROUND SOUND DATA

Audio output frame slots 6 to 9 are used to send surround sound data.

SLOTS 10 AND 11: LINE2 AND HANDSET DAC

These data slots are not supported.

SLOT 12: GPIO CONTROL

These data slots are not supported.

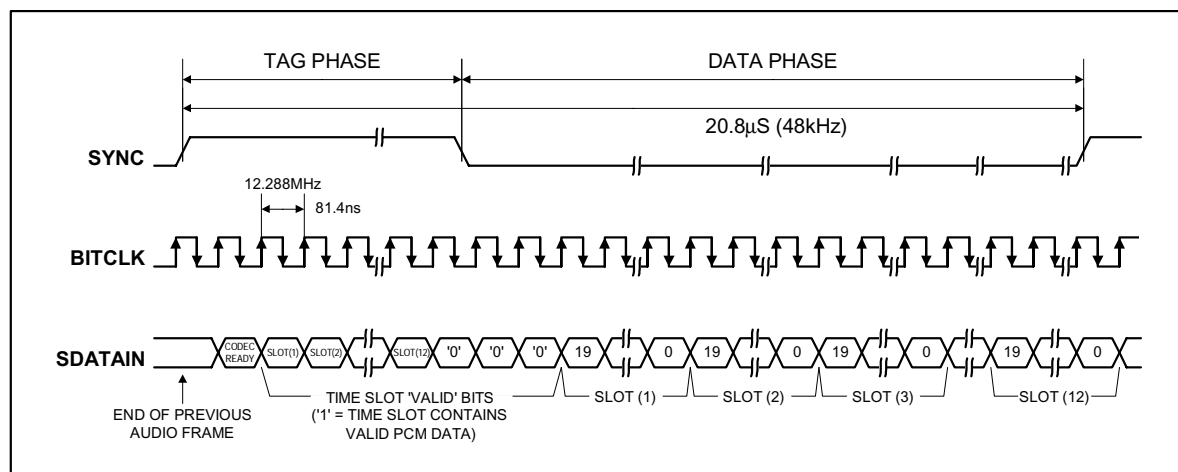
AC-LINK AUDIO INPUT FRAME (SDATAIN)

Figure 14 AC-link Audio Input Frame

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC'97 controller. As is the case for audio output frame, each AC-link audio input frame consists of 12, 20-bit time slots.

Slot 0 is a special reserved time slot containing 16-bits, which are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATAIN slot 0, bit 15) which flags whether the WM9707 is in the CODEC Ready state or not. If the CODEC Ready bit is a 0, this indicates that the WM9707 is not ready for normal operation. This condition is normal following the desertion of power on reset for example, while the WM9707's voltage references settle. When the AC-link CODEC Ready indicator bit is a 1, it indicates that the AC-link and the WM9707 control and status registers are in a fully operational state. The AC'97 controller must further probe the Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting the WM9707 into operation the AC'97 controller should poll the first bit in the audio input frame (SDATAIN slot 0, bit 15) for an indication that the WM9707 has gone CODEC Ready.

Once the WM9707 is sampled CODEC Ready then the next 12 bit positions sampled by the AC'97 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. Figure 14 illustrates the time slot based AC-link protocol.

There are several subsections within the WM9707 that can independently go busy/ready. It is the responsibility of the WM9707 controller to probe more deeply into the WM9707 register file to determine which the WM9707 subsections are actually ready.

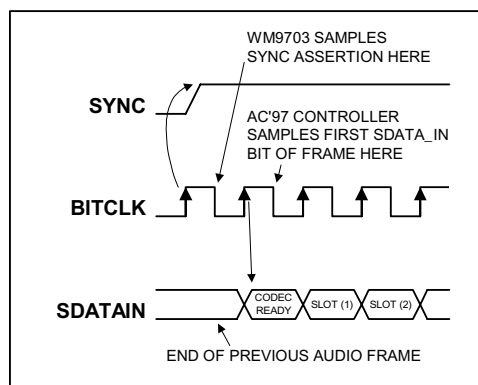


Figure 15 Start of an Audio Input Frame

A new audio input frame begins with a low to high transition of SYNC as shown in Figure 15. SYNC is synchronous to the rising edge of BITCLK. On the immediately following falling edge of BITCLK, AC'97 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BITCLK, AC'97 transitions SDATAIN into the first bit position of slot 0 ("CODEC Ready" bit). Each new bit position is presented to AC-link on a rising edge of BITCLK, and subsequently sampled by the AC'97 Controller on the following falling edge of BITCLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

SDATAIN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0s by the WM9707. SDATAIN should be sampled on the falling edges of BITCLK.

SLOT 1: STATUS ADDRESS PORT

The status port is used to monitor status for the WM9707 functions including, but not limited to, mixer settings, and power management.

Audio input frame slot 1 echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged valid by the WM9707 during slot 0).

STATUS ADDRESS PORT BIT ASSIGNMENTS:

Bit (19)	RESERVED (stuffed with 0s)
Bit (18:12)	Control register index (echo of register index for which data is being returned)
Bit (11:2)	Variable sample rate SLOTREQ bits.
Bit (1:0)	RESERVED (stuffed with 0s)

The first bit (MSB) generated by the WM9707 is always stuffed with a 0. The following 7 bit positions communicate the associated control register address. The next 10 bits support the AC'97 Rev 2.1 variable sample rate signalling protocol, and the trailing 2 bit positions are stuffed with 0s by AC'97.

SLOT 2: STATUS DATA PORT

The status data port delivers 16-bit control register read data.

Bit (19:4)	Control register read data (stuffed with 0s if tagged invalid by WM9701)
Bit (3:0)	RESERVED (stuffed with 0s)

If slot 2 is tagged invalid by the WM9707, then the entire slot will be stuffed with 0s by the WM9707.

SLOT 3: PCM RECORD LEFT CHANNEL

Audio input frame slot 3 is the left channel output of the WM9707's input Mux, post-ADC.

The WM9707 sends out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0s to fill out its 20-bit time slot.

SLOT 4: PCM RECORD RIGHT CHANNEL

Audio input frame slot 4 is the right channel output of the WM9707's input Mux, post-ADC.

The WM9707's ADCs can be implemented to support 16, 18, or 20-bit resolution.

The WM9707 ships out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0s to fill out its 20-bit time slot.

SLOT 5: OPTIONAL MODEM LINE CODEC

Not supported by WM9707.

SLOT 6: OPTIONAL DEDICATED MICROPHONE RECORD DATA

Not supported by WM9707.

SLOTS 7 TO 12: RESERVED

Audio input frame slots 7 to 12 are reserved for future use and are always stuffed with 0s by the WM9707.

AC-LINK LOW POWER MODE

The AC-link signals can be placed in a low power mode. When the WM9707's Powerdown Register 26h, is programmed to the appropriate value, both BITCLK and SDATAIN will be brought to, and held at a logic low voltage level.

BITCLK and SDATAIN are transitioned low immediately following the decode of the write to the Powerdown Register 26h with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-link into its low power mode, slots 1 and 2 are assumed to be the only valid stream in the audio output frame. At this point in time it is assumed that all sources of audio input have also been neutralised.

The AC'97 controller should also drive SYNC and SDATAOUT low after programming the WM9707 to this low power, halted mode.

Once the WM9707 has been instructed to halt BITCLK, a special wake up protocol must be used to bring the AC-link to the active mode since normal audio output and input frames can not be communicated in the absence of BITCLK.

WAKING UP THE AC-LINK

There are 2 methods for bringing the AC-link out of a low power, halted mode. Regardless of the method, it is the AC'97 controller that performs the wake up task.

AC-link protocol provides for a Cold WM9707 Reset, and a Warm WM9707 Reset.

The current Powerdown state would ultimately dictate which form of WM9707 reset is appropriate. Unless a cold or register reset (a write to the Reset Register 00h) is performed, wherein the WM9707 registers are initialised to their default values, registers are required to keep state during all Powerdown modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the Powerdown was triggered. When AC-link powers up it indicates readiness via the CODEC Ready bit (input slot 0, bit 15).

COLD WM9707 RESET

A cold reset is achieved by asserting RESETB for the minimum specified time (1 μ s). By driving RESETB low, BITCLK, and SDATAOUT will be activated, or re-activated as the case may be, and all the WM9707 control registers will be initialised to their default power on reset values.

RESETB is an asynchronous WM9707 input.

WARM WM9707 RESET

A warm WM9707 reset will re-activate the AC-link without altering the current WM9707 register values. A warm reset is signalled by driving SYNC high for a minimum of 1µs in the absence of BITCLK.

Within normal audio frames SYNC is a synchronous input. In the absence of BITCLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the WM9707. The WM9707 will not respond with the activation of BITCLK until SYNC has been sampled low again by the WM9707. This will preclude the false detection of a new audio frame.

SERIAL INTERFACE REGISTER MAP DESCRIPTION

(See Table 17)

The serial interface bits perform control functions described as follows: The register map is fully specified by the AC'97 specification, and this description is simply repeated below, with optional unsupported features omitted.

RESET REGISTER (INDEX 00h)

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code of the part, indication of modem support (not supported by the WM9707) and a code for the type of 3D stereo enhancement.

The ID decodes the capabilities of the WM9707 based on the following:

BIT	FUNCTION	VALUE ON WM9707 (BINARY)
ID0	Dedicated Mic PCM in channel	0
ID1	Modem line CODEC support	0
ID2	Bass and treble control	0
ID3	Simulated stereo (mono to stereo)	0
ID4	Headphone out support	1
ID5	Loudness (bass boost) support	0
ID6	18-bit DAC resolution	1
ID7	20-bit DAC resolution	0
ID8	18-bit ADC resolution	1
ID9	20-bit ADC resolution	0
SE4...SE0	Wolfson Microelectronics 3D enhancement	11000

Table 4 Reset Register Function

Note that the WM9707 defaults to indicate 18-bit compatibility.

PLAY MASTER VOLUME REGISTERS (INDEX 02h, 04h AND 06h)

These registers manage the output signal volumes. Register 02h controls the stereo master volume (both right and left channels), Register 04h controls the optional stereo headphone out, and Register 06h controls the mono volume output. Each step corresponds to 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞dB.

ML5 to ML0 is for left channel level, MR5 to MR0 is for the right channel and MM5 to MM0 is for the mono out channel.

Support for the MSB of the volume level is not provided by the WM9707. If the MSB is written to, then the WM9707 detects when that bit is set and sets all 4 LSBs to 1s. Example: If the driver writes a 1xxxx the WM9707 interprets that as x11111. It will also respond when read with x11111 rather than 1xxxx, the value written to it. The driver can use this feature to detect if support for the 6th bit is there or not.

The default value of both the mono and the stereo registers is 8000h (1000 0000 0000 0000), which corresponds to 0dB gain with mute on.

MUTE	MX4...MX0 (BINARY)	FUNCTION
0	0 0000	0dB attenuation
0	0 0001	1.5dB attenuation
0	1 1111	46.5dB attenuation
1	x xxxx	∞ dB attenuation

Table 5 Volume Register Function**MASTER TONE CONTROL REGISTERS (INDEX 08h)**

Optional register for support of tone controls (bass and treble). The WM9707 does not support bass and treble and writing to this register will have no effect, reading will result in all zeros.

PC BEEP REGISTER (INDEX 0Ah)

This controls the level for the PC-beep input. Each step corresponds to approximately 3dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at $-\infty$ dB.

WM9707 defaults to the PC-beep path being muted, except during reset when the path is open, so an external speaker should be provided within the PC to alert the user to power on self-test problems.

MUTE	PV3...PV0 (BINARY)	FUNCTION
0	0000	0dB attenuation
0	1111	45dB attenuation
1	xxxx	∞ dB attenuation

Table 6 PC-beep Register Function**ANALOGUE MIXER INPUT GAIN REGISTERS (INDEX 0Ch - 18h AND 72h)**

This controls the gain/attenuation for each of the analogue inputs and mixer PGA. Each step corresponds to approximately 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at $-\infty$ dB.

REGISTER 0Eh (MIC VOLUME REGISTER)

This has an extra bit that is for a 20dB boost. When bit 6 is set to 1 the 20dB boost is on. The default value is 8008h, which corresponds to 0dB gain with mute on.

The default value for the mono registers is 8008h, which corresponds to 0dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0dB gain with mute on.

MUTE	GX4...GX0 (BINARY)	FUNCTION
0	00000	+12dB gain
0	01000	0dB gain
0	11111	-34.5dB gain
1	xxxxx	$-\infty$ dB gain

Table 7 Mixer Gain Control Register Function**RECORD SELECT CONTROL REGISTER (INDEX 1Ah)**

Used to select the record source independently for right and left (see Table 8). The default value is 0000h, which corresponds to Mic in.

SR2 TO SR0	RIGHT RECORD SOURCE	SL2 TO SL0	LEFT RECORD SOURCE
0	Mic	0	Mic
1	CD in (R)	1	CD in (L)
2	Video in (R)	2	Video in (L)
3	Aux in (R)	3	Aux in (L)
4	Line in (R)	4	Line in (L)
5	Stereo mix (R)	5	Stereo mix (L)
6	Mono mix	6	Mono mix
7	Phone	7	Phone

Table 8 Record Select Register Function

RECORD GAIN REGISTERS (INDEX 1Ch)

1Ch is for the stereo input and 1Eh is for the optional special purpose correlated audio Mic channel. Each step corresponds to 1.5dB. 22.5dB corresponds to 0F0Fh. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel(s) is set at $-\infty$ dB.

The default value is 8000h, which corresponds to 0dB gain with mute on.

MUTE	GX3...GX0 (BINARY)	FUNCTION
0	1111	+22.5dB gain
0	0000	0dB gain
1	xxxxx	$-\infty$ dB gain

Table 9 Record Gain Register Function

GENERAL PURPOSE REGISTER (INDEX 20h)

This register is used to control several miscellaneous functions of the WM9707.

Below is a summary of each bit and its function. Only the 3D, MIX, MS and LPBK bits are supported by the WM9707. The MS bit controls the Mic selector. The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements. The function default value is 0000h which is all off.

BIT	FUNCTION	WM9707 SUPPORT
POP	PCM out path and mute, 0 = pre-3D, 1 = post-3D	Yes
ST	Simulated stereo enhancement, on/off 1 = on	No
3D	3D stereo enhancement on/off, 1 = on	Yes
LD	Loudness (bass boost) on/off, 1 = on	No
LLBK	Local loop back - for modem, line CODEC	No
RLBK	Remote loop back - for modem, line CODEC	No
MIX	Mono output select 0 = Mix, 1 = Mic	Yes
MS	Mic select 0 = Mic1, 1 = Mic2	Yes
LPBK	ADC/DAC loopback mode	Yes

Table 10 General Purpose Register Function

3D CONTROL REGISTER (INDEX 22h)

This register is used to control the centre and/or depth of the 3D stereo enhancement function built into of the AC'97 component. Only the depth bits DP0 to 3 have effect in the WM9707.

DP3...DP0 (DECIMAL)	DEPTH
0	0%
1	
-	
8	Typical value
-	
15	100%

POWERDOWN CONTROL/STATUS REGISTER (INDEX 26h)

This read/write register is used to program Powerdown states and monitor subsystem readiness. The lower half of this register is read only status, a 1 indicating that the subsection is *ready*. *Ready* is defined as the subsection able to perform in its nominal state. When this register is written the bit values that come in on AC-link will have no effect on read only bits 0 to 7.

When the AC-link CODEC Ready indicator bit (SDATAIN slot 0, bit 15) is a 1 it indicates that the AC-link and the WM9707 control and status registers are in a fully operational state. The AC'97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

READ BIT	FUNCTION
REF	VREFs up to nominal level
ANL	Analogue mixers, etc ready
DAC	DAC section ready to accept data
ADC	ADC section ready to transmit data

Table 11 Powerdown Status Register Function

The powerdown modes are as follows. The first three bits are to be used individually rather than in combination with each other. The last bit PR3 can be used in combination with PR2 or by itself. PR0 and PR1 control the PCM ADCs and DACs only. PR6 is not supported by the WM9707.

WRITE BIT	FUNCTION
PR0	PCM in ADCs and input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analogue mixer Powerdown (VREF still on)
PR3	Analogue mixer Powerdown (VREF off)
PR4	Digital interface (AC-link) Powerdown (external clock off)
PR5	Internal clock disable
PR6	HP amp Powerdown – not supported
EAPD	External amplifier Powerdown

Table 12 Powerdown Control Register Function

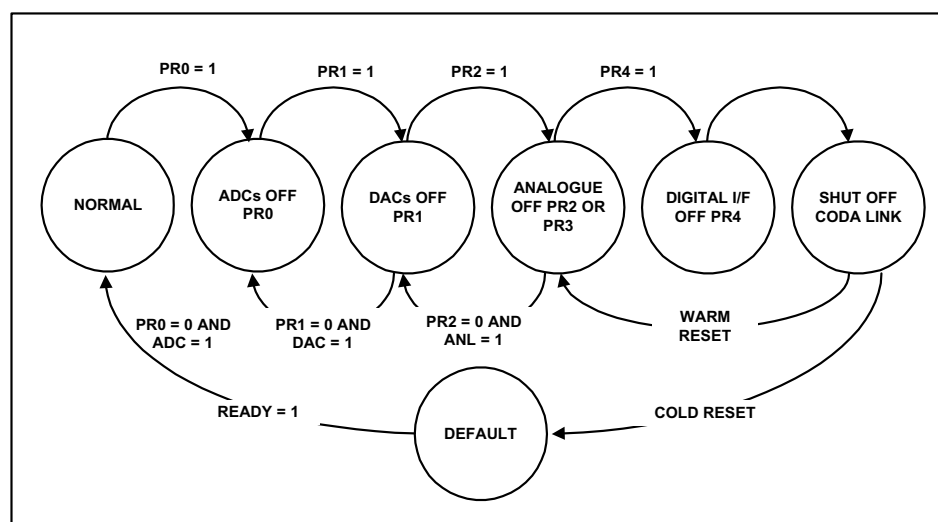


Figure 16 An Example of the WM9707 Powerdown/Powerup Flow

Figure 16 illustrates one example procedure to do a complete Powerdown of the WM9707. From normal operation sequential writes to the Powerdown Register are performed to Powerdown the WM9707 a piece at a time. After everything has been shut off (PR0 to PR3 set), a final write (of PR4) can be executed to shut down the WM9707's digital interface (AC-link).

The part will remain in sleep mode with all its registers holding their static values. To wake up the WM9707, the AC'97 controller will send a pulse on the sync line issuing a warm reset. This will restart the WM9707's digital interface (resetting PR4 to 0). The WM9707 can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers, as a cold reset will set them to their default states. When a section is powered back on, the Powerdown Control/Status Register (index 26h) should be read to verify that the section is ready (i.e. stable) before attempting any operation that requires it.

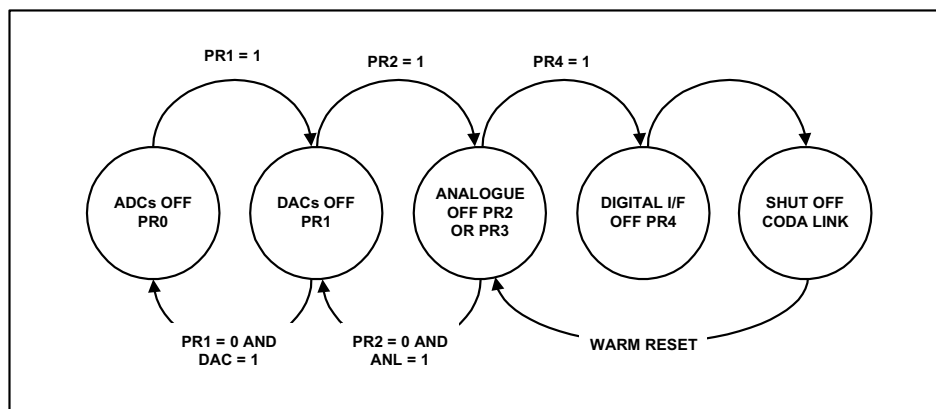


Figure 17 The WM9707 Powerdown/Flow with Analogue Still Alive

Figure 17 illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This is used when the user could be playing a CD (or external LINE_IN source) through WM9707 to the speakers but have most of the system in low power mode. The procedure for this follows the previous except that the analogue mixer is never shut down.

POWERDOWN CONTROL/STATUS REGISTER (INDEX 26h)

Note that in order to go into ultimate low power mode, PR4 and PR5 are required to be set which turns off the oscillator circuit. Asserting SYNC resets the PR4 and PR5 bit and re-starts the oscillator in the same way as the AC link is restarted. Note that PR4 is redundant in slave mode.

REVISION 2.1 REGISTERS (INDEX 28h TO 58h)

These registers are specified as to use in Revision 2.1 of the AC'97 specification and have the following functions on the WM9707:

REGISTER 28h – EXTENDED AUDIO ID

The Extended Audio ID register is a read only register that identifies which extended audio features are supported (in addition to the original AC'97 features identified by reading the reset register at index 00h). A non zero value indicates the feature is supported.

DATA BIT	FUNCTION	ANY MODE
VRA	Variable rate audio support	1
DRA	Double rate audio support	0
VRM	Variable rate Mic ADC support	0
CDAC	Centre DAC support	0
SDAC	Surround DAC support	0
LDAC	LFE DAC support	0
AMAP	Slot to front DAC mapping support	0
ID1	CODEC configuration – fixed in 9707	0
ID0	CODEC configuration – pin 45 value	1 (Inverse of level at pin 45)

Table 13 Extended Audio ID Register

REGISTER 2Ah – EXTENDED AUDIO STATUS AND CONTROL REGISTER

The Extended Audio Status and Control Register is a read/write register that provides status and control of the extended audio features.

DATA BIT	FUNCTION	READ/WRITE	WM9707 SUPPORT
VRA	Enables variable rate audio mode	Read/write	Yes
DRA	Enable double rate audio mode	Read/write	No
VRM	Enables variable rate Mic ADC	Read/write	No
CDAC	Indicates centre DAC ready	Read	No
SDAC	Indicates surround DAC ready	Read	No
LDAC	Indicates LFE DAC ready	Read	No
MADC	Indicates Mic ADC ready	Read	No
PRI	Set to turn off centre DAC	Read/write	No
PRJ	Set to turn off surround DACs	Read/write	No
PRK	Set to turn off LFE DACs	Read/write	No
PRL	Set to turn off Mic ADC	Read/write	No

Table 14 Extended Audio Status and Control Register

REGISTER 2Ch TO 32h – AUDIO SAMPLE RATE CONTROL REGISTERS

These registers are read/write registers that are written to, to select alternative sample rates for the audio PCM converters. Default is the 48ks/s rate. Note that only Revision 2.1 recommended rates are supported by the WM9707, selection of any other unsupported rates will cause the rate to default to the nearest supported rate, and the supported rate value to be latched and so read back.

Note that the SPDIF mode only supports 48ks/s rate.

REGISTERS 36h AND 38h – 6 CHANNEL VOLUME CONTROL

These read/write registers control the output volume of the optional four PCM channels. (not supported by the WM9707)

VENDOR RESERVED REGISTERS (INDEX 5Ah - 7Ah)

These registers are vendor specific. Do not write to these registers unless the Vendor ID register has been checked first to ensure that the driver knows the source of the AC '97 component.

SPDIF DIGITAL AUDIO DATA OUTPUT – (INDEX 5Ch)

The WM9707 provides an SPDIF output. In order to enable this output, bit SPDF in Register 5Ch should be set. Additionally, a bit SCMS in Register 5Ch may also be set, which sets the copyright flag in the IEC958 data, allowing serial copy protect mechanisms to be removed.

The WM9707 can be programmed to automute the DACs. By setting the mute bit, the WM9707 will mute the DACs when it detects a continuous sequence of 1024 zeros. Register 5Ch contains four vendor specific control bits.

DATA BIT	FUNCTION
AME	Setting this bit enables the automute function which causes the DAC PGAs (Reg 18) to mute when the data input is zero for 1024 bits.
SPDE	Setting this enables the SPDIF output. It can also be enabled by raising the SPDEN pin (Pin 47) to DVDD.
SPDC	This enables the copyright protect bit in the SPDIF data stream.
HPFD	Setting this bit disables the HPF on the ADC path.

Table 15 SPDIF Digital Audio Data Output and Automute Control

VENDOR SPECIFIC GAIN CONTROL REGISTERS – (INDEX 72h)

This register controls the gain and mute functions applied to the mixer path. This PGA is not accommodated in the Intel specification, but is required in order to allow the option of simultaneous recording of the mixer output and playback of DAC signals. The function is as per the other mixer PGA's. However, the default value of the register is not-muted. If it is not used it will be transparent to the user.

VENDOR ID REGISTERS (INDEX 7Ch TO 7Eh)

This register is for specific vendor identification if so desired. The ID method is Microsoft's Plug and Play Vendor ID code. The first character of that ID is F7 to F0, the second character S7 to S0, and the third T7 to T0. These three characters are ASCII encoded. The REV7 to REV0 field is for the Vendor Revision number. In the WM9707 the vendor ID is set to WML3.

Wolfson is a registered Microsoft Plug and Play vendor.

VENDOR SURROUND SOUND REGISTERS (INDEX 74h)

This register describes how data is mapped to the AC'97 DACs. Register 74h can be used to change the incoming DAC data slots that are used by the on-board DACs. This allows software control of multiple CODECs.

SURROUND SOUND DSS1, DSS0	PCM OUT LEFT	PCM OUT RIGHT
00	3	4
01	7	8
1X	6	9

Table 16 Vendor Surround Sound Register - Reg 74 [1:0]

The volume control register is still 02h and the rate register is 2Ch. The ID pins have no effect on this mapping.

SERIAL INTERFACE REGISTER MAP

The following table shows the function and address of the various control bits that are loaded through the serial interface during write operations.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	6150h
02h	Master volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
04h	LNLVL volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master volume mono	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PCBEEP volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV2	PV0	X	8000h
0Ch	Phone volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line in volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM out volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Rec select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Rec gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
20h	General purpose	POP	X	3D	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
22h	3D control	X	X	X	X	X	X	X	X	X	X	X	X	DP3	DP2	DP1	DP0	0000h
24h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
26h	Power/down control status	APD	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Ext'd audio ID	ID1	ID0	X	X	X	X	Amap	Ldac	Sdac	Cdac	X	X	VRM	X	DRA	VRA	1001h
2Ah	Ext'd audio stat/ctrl	X	PRL	PRK	PRJ	PRI	X	Madc	Ldac	Sdac	Cdac	X	X	VRM	X	DRA	VRA	0000h
2Ch	Front DAC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	Audio ADC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
5Ch	Vendor specific	REVISION				X	X	X	X	X	X	X	X	HPF D	SPD C	SPD E	AME	1000h
72h	Front mixer volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	0808h
74h	Surround sound	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DSS1	DSS0	0000h
7Ah	Vendor reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	574Dh
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev0	4C03h

Table 17 Serial Interface Register Map Description

RECOMMENDED EXTERNAL COMPONENTS

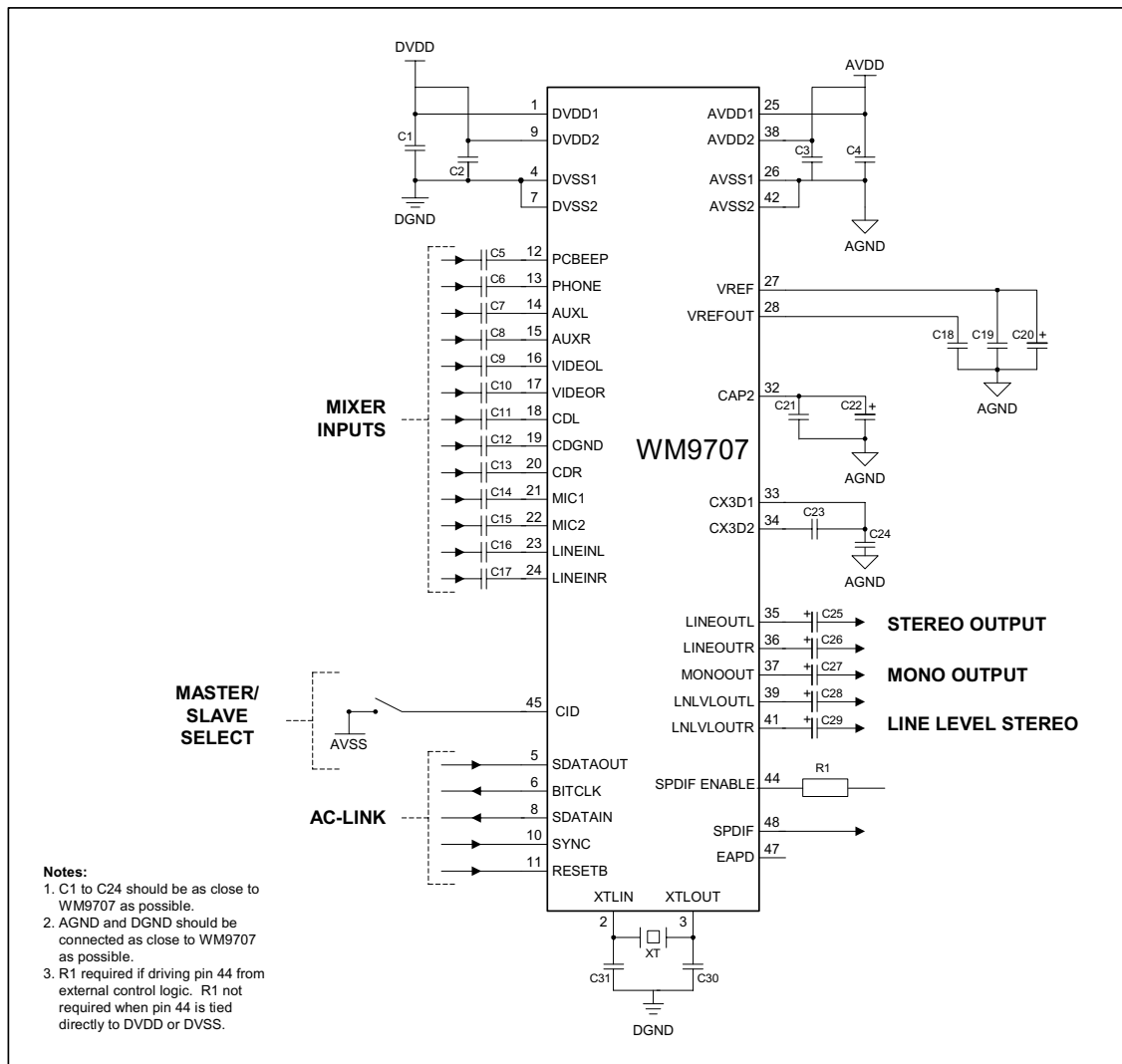


Figure 18 External Components Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1 to C4	100nF	De-coupling for DVDD and AVDD
C5 to C17	470nF	AC coupling capacitors for setting DC level of analogue inputs to VCAP1. Value chosen to give corner frequency below 20Hz for min 10K input impedance.
C18	1μF	Reference de-coupling capacitors for ADC, DAC, Mixer and CAP2 references. Ceramic type or similar.
C19	0.1μF	
C20	10μF	
C21	0.1μF	
C22	10μF	
C23	100nF	3D low pass filter. This value sets nominal 100Hz.
C24	47nF	3D high pass filter. This value sets nominal 1kHz.
C25 to C29	10μF	Output AC coupling caps to remove VREF DC level from outputs.
C30 and C31	22pF	Optional capacitors for better crystal frequency stability.
R1	1kΩ	See note 3 above
XT	24.576 MHz	AC'97 master clock frequency. A bias resistor is not required, but if connected will not affect operation if value is large (above 1MΩ).

Table 18 External Component Values

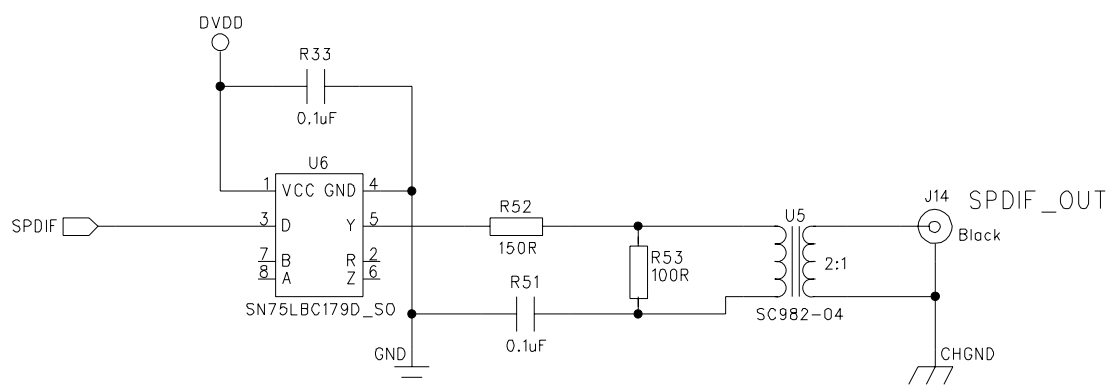


Figure 19 Suggested SPDIF Output Circuit (DVDD = 5V)

RECOMMENDATIONS FOR 3.3V OPERATION

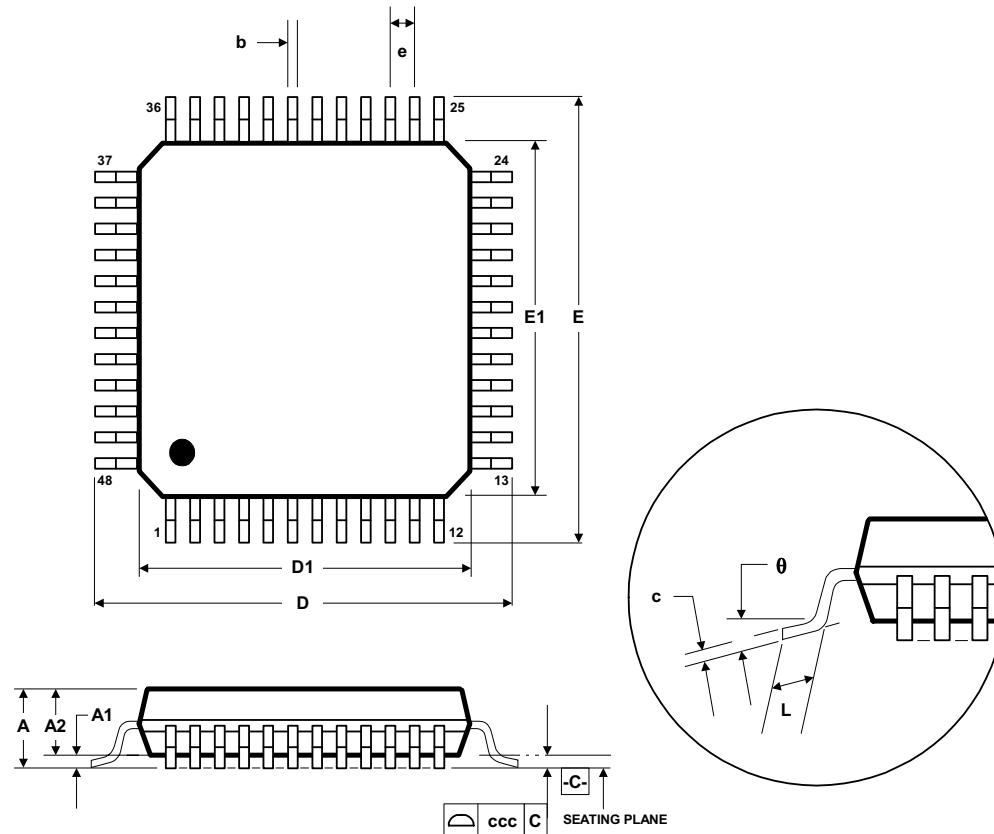
The device's performance with AVDD = 3.3V is shown in Electrical Characteristics.

In 3.3V analogue operation, mid-rail reference scales to 1.65V. All ADC and DAC references are 2/3rds of their nominal 5V value. Input and output signals that are 1Vrms in 5V applications, scale to 660mVrms in 3.3V applications. It is not possible to produce an undistorted 1Vrms output by using the mixer PGA gain whilst running from a 3.3V analogue supply.

PACKAGE DIMENSIONS

FT: 48 PIN TQFP (7 x 7 x 1.4 mm)

DM003.B



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.60
A ₁	0.05	-----	0.15
A ₂	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	9.00 BSC		
D ₁	7.00 BSC		
E	9.00 BSC		
E ₁	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
θ	0°	3.5°	7°
Tolerances of Form and Position			
ccc	0.08		
REF:	JEDEC.95, MS-026		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MS-026, VARIATION = BBC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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