622 Mbps Clock and Data Recovery IC with Integrated Limiting Amplifier

ADN2804

FEATURES

- Exceeds SONET requirements for jitter transfer/ generation/tolerance
- Quantizer sensitivity: 3.3 mV typical
- Adjustable slice level: ±95 mV
- Patented clock recovery architecture
- Loss-of-signal (LOS) detect range: 2.6 mV to 18.4 mV
- Independent slice level adjust and LOS detector
- No reference clock required
- Loss-of-lock indicator
- I²C® interface to access optional features
- Single-supply operation: 3.3 V
- Low power: 423 mW typical
- 5 mm × 5 mm, 32-lead LFCSP, Pb free

APPLICATIONS

- BPON ONT
- SONET OC-12
- WDM transponders
- Regenerators/repeaters
- Test equipment
- Broadband cross-connects and routers

GENERAL DESCRIPTION

The ADN2804 provides the receiver functions of quantization, signal level detect, clock and data recovery, and data retiming for 622 Mbps NRZ data. The ADN2804 automatically locks to 622 Mbps data without the need for an external reference clock or programming. In the absence of input data, the output clock drifts no more than ±5%. All SONET jitter requirements are met, including jitter transfer, jitter generation, and jitter tolerance. All specifications are quoted for −40°C to +85°C ambient temperature, unless otherwise noted.

This device, together with a PIN diode and a TIA preamplifier, can implement a highly integrated, low cost, low power fiber optic receiver.

The receiver's front-end loss-of-signal (LOS) detector circuit indicates when the input signal level falls below a user-adjustable threshold. The LOS detect circuit has hysteresis to prevent chatter at the output.

The ADN2804 is available in a compact 5 mm × 5 mm, 32-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM

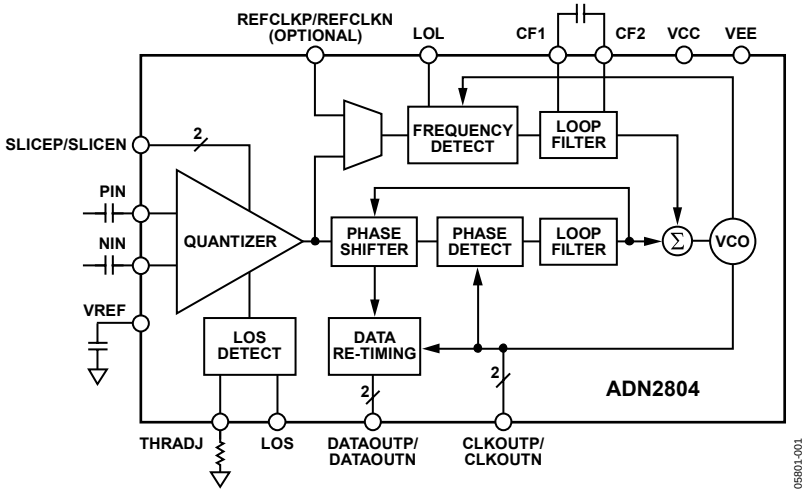

Figure 1.

Rev. 0

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REVISION HISTORY

2/06—Revision 0: Initial Version

SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, VEE = 0 V, C_F = 0.47 µF, SLICEP = SLICEN = VEE, input data pattern: PRBS $2^{23} - 1$, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
QUANTIZER—DC CHARACTERISTICS					
Input Voltage Range	@ PIN or NIN, dc-coupled	1.8		2.8	V
Peak-to-Peak Differential Input	PIN − NIN			2.0	V
Input Common-Mode Level	DC-coupled (see Figure 27, Figure 28, and Figure 29)	2.3	2.5	2.8	V
Differential Input Sensitivity	$2^{23} - 1$ PRBS, ac-coupled,[1] BER = 1×10^{-10}	6	3.3		mV p-p
Input Offset			500		µV
Input RMS Noise	BER = 1×10^{-10}		290		µV rms
QUANTIZER—AC CHARACTERISTICS					
Data Rate			622		Mbps
Output Clock Range	Absence of input data		622 ± 5%		MHz
S11	@ 622 MHz		−15		dB
Input Resistance	Differential		100		Ω
Input Capacitance			0.65		pF
QUANTIZER—SLICE ADJUSTMENT					
Gain	SLICEP − SLICEN = ±0.5 V	0.10	0.11	0.13	V/V
Differential Control Voltage Input	SLICEP − SLICEN	−0.95		+0.95	V
Control Voltage Range	DC level @ SLICEP or SLICEN	VEE		0.95	V
Slice Threshold Offset			1		mV
LOSS-OF-SIGNAL (LOS) DETECT					
Loss-of-Signal Detect Range (see Figure 6)	R_{THRESH} = 0 Ω	14.9	16.7	18.4	mV
	R_{THRESH} = 100 kΩ	2.6	3.5	4.4	mV
Hysteresis (Electrical)	OC-12				
	R_{THRESH} = 0 Ω	6.2	6.9	7.7	dB
	R_{THRESH} = 100 kΩ	4.1	6.1	8.1	dB
LOS Assert Time	DC-coupled[2]		500		ns
LOS Deassert Time	DC-coupled[2]		400		ns
LOSS-OF-LOCK (LOL) DETECT					
VCO Frequency Error for LOL Assert	With respect to nominal		1000		ppm
VCO Frequency Error for LOL Deassert	With respect to nominal		250		ppm
LOL Response Time	OC-12		200		µs
ACQUISITION TIME					
Lock to Data Mode	OC-12		2.0		ms
Optional Lock to REFCLK Mode			20.0		ms
DATA RATE READBACK ACCURACY					
Fine Readback	In addition to REFCLK accuracy				
	OC-12		100		ppm
POWER SUPPLY VOLTAGE		3.0	3.3	3.6	V
POWER SUPPLY CURRENT	Locked to 622.08 Mbps		128		mA
OPERATING TEMPERATURE RANGE		−40		+85	°C

[1] PIN and NIN should be differentially driven and ac-coupled for optimum sensitivity.
[2] When ac-coupled, the LOS assert and deassert times are dominated by the RC time constant of the ac coupling capacitor and the 50 Ω input termination of the ADN2804 input stage.

JITTER SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, VEE = 0 V, C_F = 0.47 µF, SLICEP = SLICEN = VEE, input data pattern: PRBS $2^{23} - 1$, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
PHASE-LOCKED LOOP CHARACTERISTICS					
Jitter Transfer Bandwidth	OC-12		75	130	kHz
Jitter Peaking	OC-12		0	0.03	dB
Jitter Generation	OC-12, 12 kHz to 5 MHz		0.001	0.003	UI rms
			0.011	0.026	UI p-p
Jitter Tolerance	OC-12, $2^{23} - 1$ PRBS				
	30 Hz[1]	100			UI p-p
	300 Hz[1]	44			UI p-p
	25 kHz	2.5			UI p-p
	250 kHz[1]	1.0			UI p-p

[1] Jitter tolerance of the ADN2804 at these jitter frequencies is better than what the test equipment is able to measure.

OUTPUT AND TIMING SPECIFICATIONS

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
LVDS OUTPUT CHARACTERISTICS					
(CLKOUTP/CLKOUTN, DATAOUTP/DATAOUTN)					
Output Voltage High	V_{OH} (see Figure 3)			1475	mV
Output Voltage Low	V_{OL} (see Figure 3)	925			mV
Differential Output Swing	V_{OD} (see Figure 3)	250	320	400	mV
Output Offset Voltage	V_{OS} (see Figure 3)	1125	1200	1275	mV
Output Impedance	Differential		100		Ω
LVDS Outputs' Timing					
Rise Time	20% to 80%		115	220	ps
Fall Time	80% to 20%		115	220	ps
Setup Time	T_S (see Figure 2), OC-12	760	800	840	ps
Hold Time	T_H (see Figure 2), OC-12	760	800	840	ps
I^2C INTERFACE DC CHARACTERISTICS	LVCMOS				
Input High Voltage	V_{IH}	0.7 VCC			V
Input Low Voltage	V_{IL}			0.3 VCC	V
Input Current	V_{IN} = 0.1 VCC or V_{IN} = 0.9 VCC	−10.0		+10.0	μA
Output Low Voltage	V_{OL}, I_{OL} = 3.0 mA			0.4	V
I^2C INTERFACE TIMING	See Figure 11				
SCK Clock Frequency				400	kHz
SCK Pulse Width High	t_{HIGH}	600			ns
SCK Pulse Width Low	t_{LOW}	1300			ns
Start Condition Hold Time	$t_{HD;STA}$	600			ns
Start Condition Setup Time	$t_{SU;STA}$	600			ns
Data Setup Time	$t_{SU;DAT}$	100			ns
Data Hold Time	$t_{HD;DAT}$	300			ns
SCK/SDA Rise/Fall Time	T_R/T_F	20 + 0.1 Cb[1]		300	ns
Stop Condition Setup Time	$t_{SU;STO}$	600			ns
Bus Free Time Between a Stop and a Start	t_{BUF}	1300			ns
REFCLK CHARACTERISTICS	Optional lock to REFCLK mode				
Input Voltage Range	@ REFCLKP or REFCLKN				
	V_{IL}		0		V
	V_{IH}		VCC		V
Minimum Differential Input Drive			100		mV p-p
Reference Frequency		10		160	MHz
Required Accuracy			100		ppm
LVTTL DC INPUT CHARACTERISTICS					
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V
Input High Current	I_{IH}, V_{IN} = 2.4 V			5	μA
Input Low Current	I_{IL}, V_{IN} = 0.4 V	−5			μA
LVTTL DC OUTPUT CHARACTERISTICS					
Output High Voltage	V_{OH}, I_{OH} = −2.0 mA	2.4			V
Output Low Voltage	V_{OL}, I_{OL} = +2.0 mA			0.4	V

[1] Cb = total capacitance of one bus line in picofarads. If used with Hs-mode devices, faster fall times are allowed.

ABSOLUTE MAXIMUM RATINGS

$T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, VEE = 0 V, C_F = 0.47 µF, SLICEP = SLICEN = VEE, unless otherwise noted.

Table 4.

Parameter	Rating
Supply Voltage (VCC)	4.2 V
Minimum Input Voltage (All Inputs)	VEE − 0.4 V
Maximum Input Voltage (All Inputs)	VCC + 0.4 V
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

32-lead LFCSP, 4-layer board with exposed paddle soldered to VEE, θ_{JA} = 28°C/W.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING CHARACTERISTICS

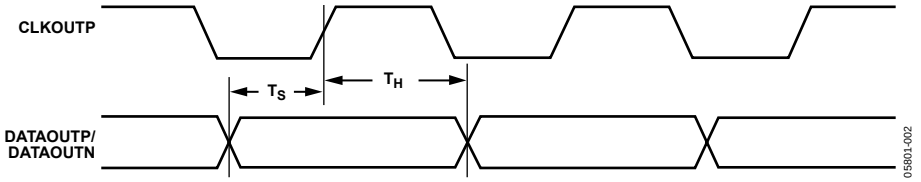


Figure 2. Output Timing

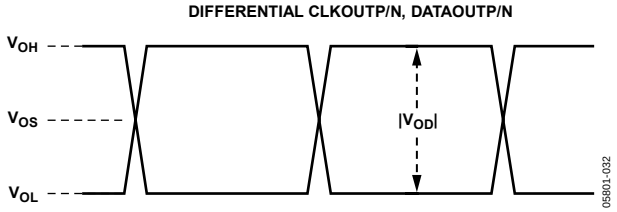


Figure 3. Differential Output Specifications

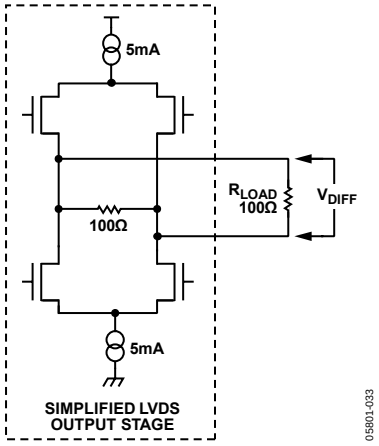


Figure 4. Differential Output Stage

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

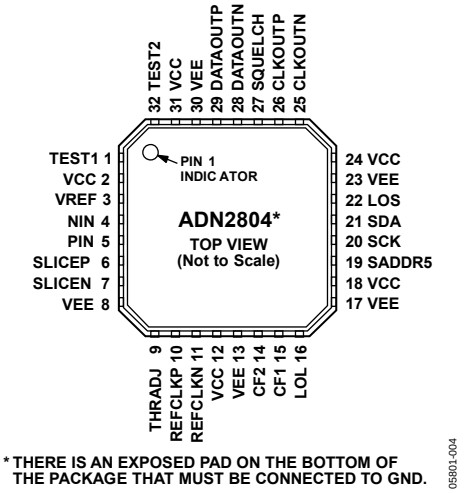


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	TEST1		Connect to VCC.
2	VCC	P	Power for Limiting Amplifier, LOS.
3	VREF	AO	Internal VREF Voltage. Decouple to GND with a 0.1 µF capacitor.
4	NIN	AI	Differential Data Input. CML.
5	PIN	AI	Differential Data Input. CML.
6	SLICEP	AI	Differential Slice Level Adjust Input.
7	SLICEN	AI	Differential Slice Level Adjust Input.
8	VEE	P	GND for Limiting Amplifier, LOS.
9	THRADJ	AI	LOS Threshold Setting Resistor.
10	REFCLKP	DI	Differential REFCLK Input. 10 MHz to 160 MHz.
11	REFCLKN	DI	Differential REFCLK Input. 10 MHz to 160 MHz.
12	VCC	P	VCO Power.
13	VEE	P	VCO GND.
14	CF2	AO	Frequency Loop Capacitor.
15	CF1	AO	Frequency Loop Capacitor.
16	LOL	DO	Loss-of-Lock Indicator. LVTTL active high.
17	VEE	P	FLL Detector GND.
18	VCC	P	FLL Detector Power.
19	SADDR5	DI	Slave Address Bit 5.
20	SCK	DI	I^2C Clock Input.
21	SDA	DI	I^2C Data Input.
22	LOS	DO	Loss-of-Signal Detect Output. Active high. LVTTL.
23	VEE	P	Output Buffer, I^2C GND.
24	VCC	P	Output Buffer, I^2C Power.
25	CLKOUTN	DO	Differential Recovered Clock Output. LVDS.
26	CLKOUTP	DO	Differential Recovered Clock Output. LVDS.
27	SQUELCH	DI	Disable Clock and Data Outputs. Active high. LVTTL.
28	DATAOUTN	DO	Differential Recovered Data Output. LVDS.
29	DATAOUTP	DO	Differential Recovered Data Output. LVDS.
30	VEE	P	Phase Detector, Phase Shifter GND.
31	VCC	P	Phase Detector, Phase Shifter Power.
32	TEST2		Connect to VCC.
Exposed Pad	Pad	P	Connect to GND.

[1] Type: P = power, AI = analog input, AO = analog output, DI = digital input, DO = digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

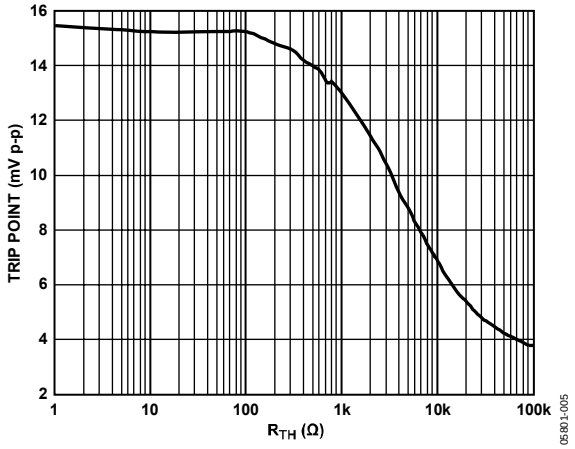


Figure 6. LOS Comparator Trip Point Programming

I²C INTERFACE TIMING AND INTERNAL REGISTER DESCRIPTION

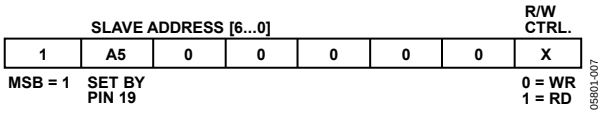


Figure 7. Slave Address Configuration

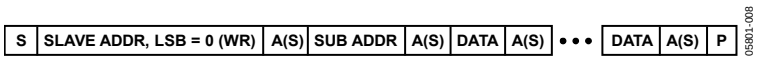


Figure 8. I²C Write Data Transfer

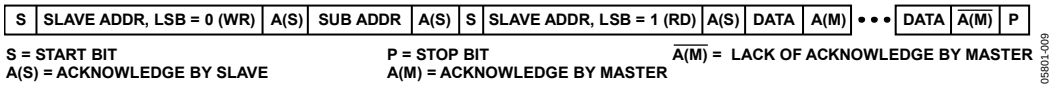


Figure 9. I²C Read Data Transfer

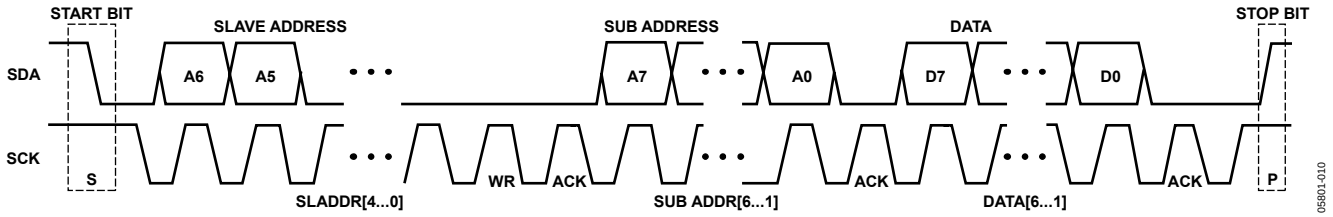


Figure 10. I²C Data Transfer Timing

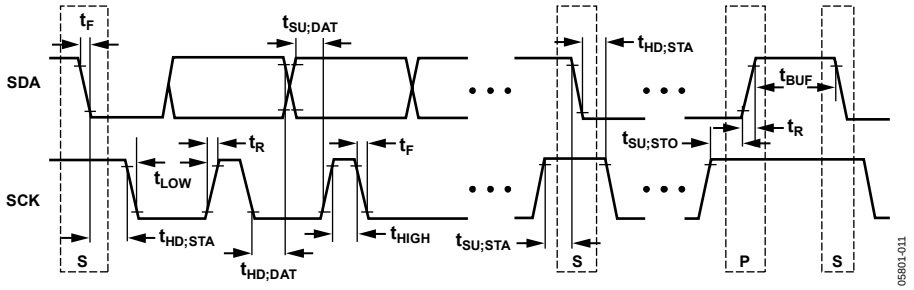


Figure 11. I²C Port Timing Diagram

Table 6. Internal Register Map[1]

Reg Name	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0
FREQ0	R	0x0	MSB							LSB
FREQ1	R	0x1	MSB							LSB
FREQ2	R	0x2	0	MSB						LSB
MISC	R	0x4	x	x	LOS status	Static LOL	LOL status	Data rate measurement complete	x	x
CTRLA	W	0x8	F_{REF} range		Data rate/DIV_F_{REF} ratio				Measure data rate	Lock to reference
CTRLB	W	0x9	Config LOL	Reset MISC[4]	System reset	0	Reset MISC[2]	0	0	0
CTRLC	W	0x11	0	0	0	0	0	Config LOS	SQUELCH mode	Output boost

[1] All writeable registers default to 0x00.

Table 7. Miscellaneous Register, MISC

D7	D6	LOS Status D5	Static LOL D4	LOL Status D3	Data Rate Measurement Complete D2	D1	D0
x	x	0 = No loss of signal 1 = Loss of signal	0 = Waiting for next LOL 1 = Static LOL until reset	0 = Locked 1 = Acquiring	0 = Measuring data rate 1 = Measurement complete	x	x

Table 8. Control Register, CTRLA[1]

F_{REF} Range			Data Rate/Div_F_{REF} Ratio					Measure Data Rate	Lock to Reference
D7	D6		D5	D4	D3	D2		D1	D0
0	0	19.44 MHz	0	1	0	1	32	Set to 1 to measure data rate	0 = Lock to input data 1 = Lock to reference clock
0	1	38.88 MHz	0	1	0	1	32		
1	0	77.76 MHz	0	1	0	1	32		
1	1	155.52 MHz	0	1	0	1	32		

[1] Where DIV_F_{REF} is the divided down reference referred to the 10 MHz to 20 MHz band (see the Reference Clock (Optional) section).

Table 9. Control Register, CTRLB

Config LOL D7	Reset MISC[4] D6	System Reset D5	D4	Reset MISC[2] D3	D2	D1	D0
0 = LOL pin normal operation 1 = LOL pin is static LOL	Write a 1 followed by 0 to reset MISC[4]	Write a 1 followed by 0 to reset ADN2804	Set to 0	Write a 1 followed by 0 to reset MISC[2]	Set to 0	Set to 0	Set to 0

Table 10. Control Register, CTRLC

D7	D6	D5	D4	D3	Config LOS D2	SQUELCH Mode D1	Output Boost D0
Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	0 = Active high LOS 1 = Active low LOS	0 = Squelch data outputs and clock outputs 1 = Squelch data outputs or clock outputs	0 = Default output swing 1 = Boost output swing

TERMINOLOGY

Input Sensitivity and Input Overdrive

Sensitivity and overdrive specifications for the quantizer involve offset voltage, gain, and noise. The relationship between the logic output of the quantizer and the analog voltage input is shown in Figure 12. For sufficiently large positive input voltage, the output is always Logic 1; similarly, for negative inputs, the output is always Logic 0. However, the transitions between output Logic Level 1 and output Logic Level 0 are not at precisely defined input voltage levels, but occur over a range of input voltages. Within this range of input voltages, the output may be either 1 or 0, or it may even fail to attain a valid logic state. The width of this zone is determined by the input voltage noise of the quantizer. The center of the zone is the quantizer input offset voltage. Input overdrive is the magnitude of signal required to guarantee the correct logic level with 1×10^{-10} confidence level.

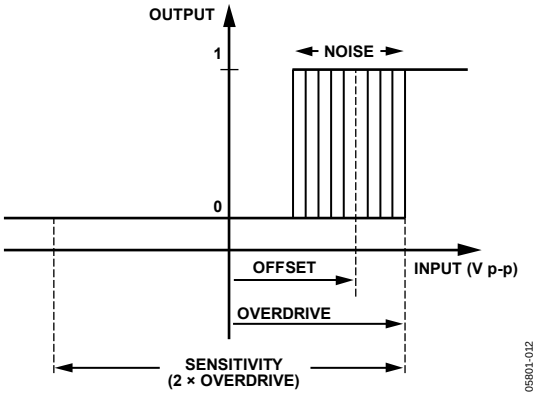


Figure 12. Input Sensitivity and Input Overdrive

Single-Ended vs. Differential

AC coupling is typically used to drive the inputs to the quantizer. The inputs are internally dc biased to a common-mode potential of ~2.5 V. Driving the ADN2804 in a single-ended fashion and observing the quantizer input with an oscilloscope probe at the point indicated in Figure 13 shows a binary signal with an average value equal to the common-mode potential and instantaneous values both above and below the average value. It is convenient to measure the peak-to-peak amplitude of this signal and call the minimum required value the quantizer sensitivity. Referring to Figure 13, the sensitivity is twice the overdrive because both positive and negative offsets need to be accommodated. The ADN2804 quantizer typically has 3.3 mV p-p sensitivity.

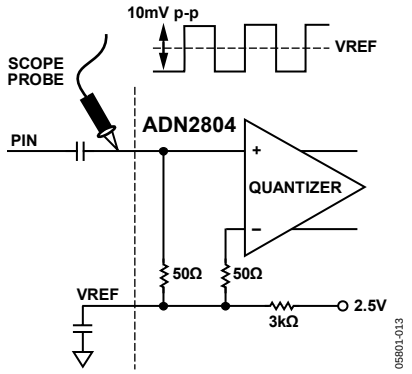


Figure 13. Single-Ended Sensitivity Measurement

When the ADN2804 is driven differentially (see Figure 14), sensitivity seems to improve if observing the quantizer input with an oscilloscope probe. This is an illusion caused by the use of a single-ended probe. A 5 mV p-p signal appears to drive the ADN2804 quantizer; however, the single-ended probe measures only half the signal. The true quantizer input signal is twice this value, because the other quantizer input is a complementary signal to the signal being observed.

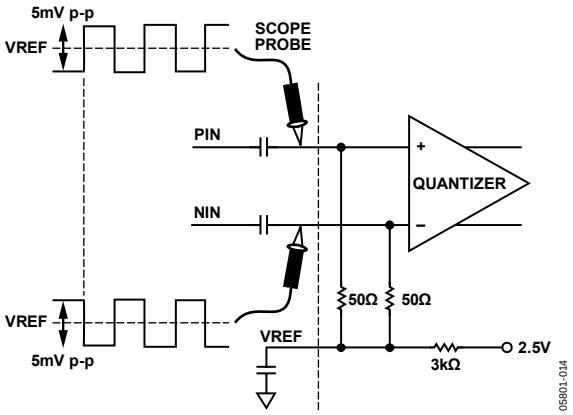


Figure 14. Differential Sensitivity Measurement

LOS Response Time

LOS response time is the delay between removal of the input signal and indication of loss of signal (LOS) at the LOS output, Pin 22. When the inputs are dc-coupled, the LOS assert time of the AD2804 is 500 ns typical and the deassert time is 400 ns typical. In practice, the time constant produced by the ac coupling at the quantizer input and the 50 Ω on-chip input termination determines the LOS response time.

JITTER SPECIFICATIONS

The ADN2804 CDR is designed to achieve the best bit-error-rate (BER) performance and to exceed the jitter transfer, generation, and tolerance specifications proposed for SONET/SDH equipment defined in the Telcordia Technologies specification.

Jitter is the dynamic displacement of digital signal edges from their long-term average positions, measured in unit intervals (UI), where 1 UI = 1 bit period. Jitter on the input data can cause dynamic phase errors on the recovered clock sampling edge. Jitter on the recovered clock causes jitter on the retimed data.

The following sections briefly summarize the specifications of jitter generation, transfer, and tolerance in accordance with the Telcordia document (GR-253-CORE, Issue 3, September 2000) for the optical interface at the equipment level and the ADN2804 performance with respect to those specifications.

Jitter Generation

The jitter generation specification limits the amount of jitter that can be generated by the device with no jitter and wander applied at the input. For SONET devices, the jitter generated must be less than 0.01 UI rms and less than 0.1 UI p-p.

Jitter Transfer

The jitter transfer function is the ratio of the jitter on the output signal to the jitter applied on the input signal vs. the frequency. This parameter measures the amount of jitter on an input signal that can be transferred to the output signal (see Figure 15). This amount is limited.

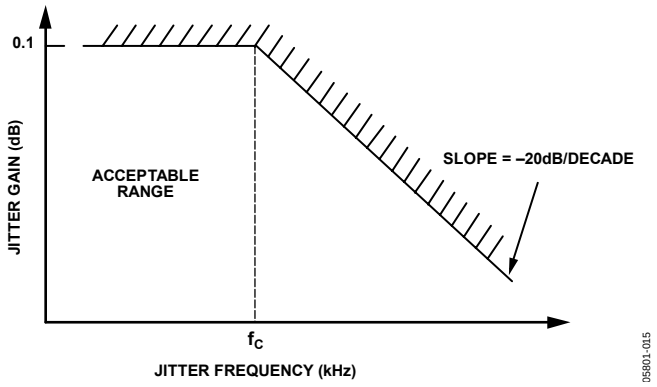


Figure 15. Jitter Transfer Curve

Jitter Tolerance

The jitter tolerance is defined as the peak-to-peak amplitude of the sinusoidal jitter applied on the input signal, which causes a 1 dB power penalty. This is a stress test intended to ensure that no additional penalty is incurred under the operating conditions (see Figure 16).

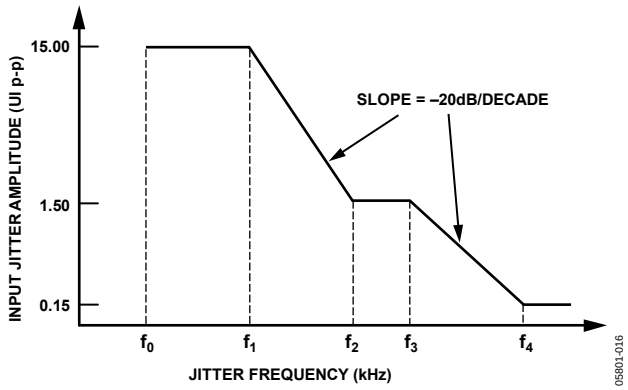


Figure 16. SONET Jitter Tolerance Mask

THEORY OF OPERATION

The ADN2804 is a delay- and phase-locked loop circuit for clock recovery and data retiming from an NRZ encoded data stream. The phase of the input data signal is tracked by two separate feedback loops, which share a common control voltage. A high speed delay-locked loop path uses a voltage controlled phase shifter to track the high frequency components of input jitter. A separate phase control loop, composed of the VCO, tracks the low frequency components of input jitter. The initial frequency of the VCO is set by yet a third loop that compares the VCO frequency with the input data frequency and sets the coarse tuning voltage. The jitter tracking phase-locked loop controls the VCO by the fine-tuning control.

The delay and phase loops together track the phase of the input data signal. For example, when the clock lags the input data, the phase detector drives the VCO to a higher frequency and increases the delay through the phase shifter; both of these actions serve to reduce the phase error between the clock and the data. The faster clock picks up phase, whereas the delayed data loses phase. Because the loop filter is an integrator, the static phase error is driven to 0°.

Another view of the circuit is that the phase shifter implements the zero required for frequency compensation of a second-order phase-locked loop, and this zero is placed in the feedback path; therefore, it does not appear in the closed-loop transfer function. Jitter peaking in a conventional second-order phase-locked loop is caused by the presence of this zero in the closed-loop transfer function. Because this circuit has no zero in the closed-loop transfer, jitter peaking is minimized.

The delay and phase loops together simultaneously provide wideband jitter accommodation and narrow-band jitter filtering. The linearized block diagram in Figure 17 shows that the jitter transfer function, Z(s)/X(s), provides excellent second-order low-pass filtering. Note that the jitter transfer has no zero, unlike an ordinary second-order phase-locked loop. This means that the main PLL loop has virtually no jitter peaking (see Figure 18), making this circuit ideal for signal regenerator applications, where jitter peaking in a cascade of regenerators can contribute to hazardous jitter accumulation.

The error transfer, e(s)/X(s), has the same high-pass form as an ordinary phase-locked loop. This transfer function can be optimized to accommodate a significant amount of wideband jitter, because the jitter transfer function, Z(s)/X(s), provides the narrow-band jitter filtering.

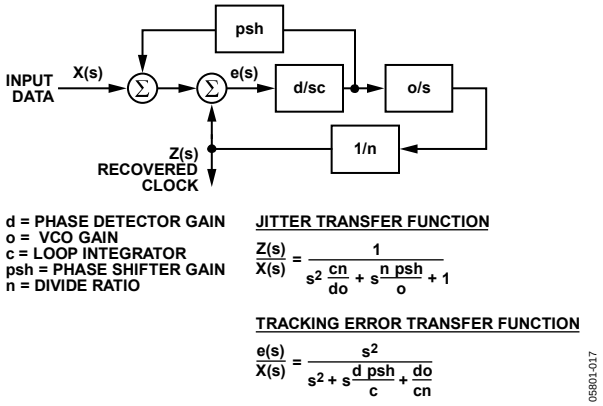


Figure 17. PLL/DLL Architecture

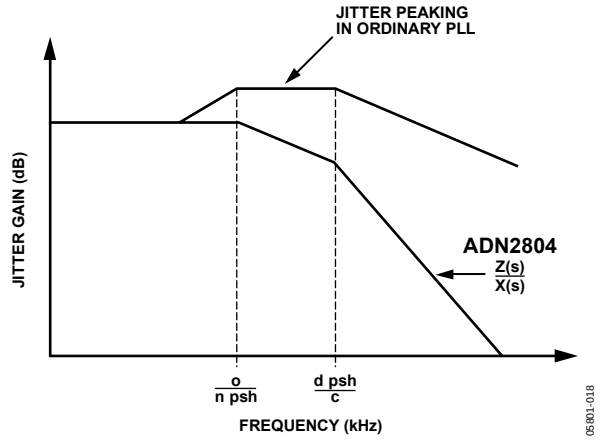


Figure 18. Jitter Response vs. Conventional PLL

The delay and phase loops contribute to overall jitter accommodation. At low frequencies of input jitter on the data signal, the integrator in the loop filter provides high gain to track large jitter amplitudes with small phase error. In this case, the VCO is frequency modulated, and jitter is tracked as in an ordinary phase-locked loop. The amount of low frequency jitter that can be tracked is a function of the VCO tuning range. A wider tuning range gives larger accommodation of low frequency jitter. The internal loop control voltage remains small for small phase errors; therefore, the phase shifter remains close to the center of its range and thus contributes little to the low frequency jitter accommodation.

At medium jitter frequencies, the gain and tuning range of the VCO are not large enough to track input jitter. In this case, the VCO control voltage becomes large and saturates, and the VCO frequency dwells at one extreme of its tuning range. The size of the VCO tuning range, therefore, has only a small effect on the jitter accommodation. The delay-locked loop control voltage is now larger; therefore, the phase shifter takes on the burden of tracking the input jitter. The phase shifter range, in UI, can be seen as a broad plateau on the jitter tolerance curve. The phase shifter has a minimum range of 2 UI at all data rates.

The gain of the loop integrator is small for high jitter frequencies; therefore, larger phase differences are needed to increase the loop control voltage enough to tune the range of the phase shifter. However, large phase errors at high jitter frequencies cannot be tolerated. In this region, the gain of the integrator determines the jitter accommodation. Because the gain of the loop integrator declines linearly with frequency, jitter accommodation is lower with higher jitter frequency. At the highest frequencies, the loop gain is very small, and little tuning of the phase shifter can be expected. In this case, jitter accommodation is determined by the eye opening of the input data, the static phase error, and the residual loop jitter generation. The jitter accommodation is roughly 0.5 UI in this region. The corner frequency between the declining slope and the flat region is the closed-loop bandwidth of the delay-locked loop, which is roughly 1.0 MHz at 622 Mbps.

FUNCTIONAL DESCRIPTION

FREQUENCY ACQUISITION

The ADN2804 acquires frequency from the data. The lock detector circuit compares the frequency of the VCO and the frequency of the incoming data. When these frequencies differ by more than 1000 ppm, LOL is asserted. This initiates a frequency acquisition cycle. When the VCO frequency is within 250 ppm of the data frequency, LOL is deasserted.

Once LOL is deasserted, the frequency-locked loop is turned off. The PLL/DLL pulls the VCO frequency in the rest of the way until the VCO frequency equals the data frequency.

The frequency loop requires a single external capacitor between CF1 and CF2, Pin 14 and Pin 15. A 0.47 µF ± 20%, X7R ceramic chip capacitor with <10 nA leakage current is recommended. Leakage current of the capacitor can be calculated by dividing the maximum voltage across the 0.47 µF capacitor, ~3 V, by the insulation resistance of the capacitor. The insulation resistance of the 0.47 µF capacitor should be greater than 300 MΩ.

LIMITING AMPLIFIER

The limiting amplifier has differential inputs (PIN/NIN) that are internally terminated with 50 Ω to an on-chip voltage reference (VREF = 2.5 V typically). The inputs are typically ac-coupled externally, although dc coupling is possible as long as the input common-mode voltage remains above 2.5 V (see Figure 27 to Figure 29 in the Applications Information section). Input offset is factory trimmed to achieve better than 3.3 mV typical sensitivity with minimal drift. The limiting amplifier can be driven differentially or in a single-ended fashion.

SLICE ADJUST

The quantizer slicing level can be offset by ±100 mV to mitigate the effect of amplified spontaneous emission (ASE) noise or duty cycle distortion by applying a differential voltage input of up to ±0.95 V to the SLICEP and SLICEN inputs. If no adjustment of the slice level is needed, SLICEP and SLICEN should be tied to VEE. The gain of the slice adjustment is ~0.11 V/V.

LOSS-OF-SIGNAL (LOS) DETECTOR

The receiver front-end LOS detector circuit detects when the input signal level falls below a user-adjustable threshold. The threshold is set with a single external resistor from Pin 9, THRADJ, to VEE. The LOS comparator trip point vs. the resistor value is shown in Figure 6. If the input level to the ADN2804 drops below the programmed LOS threshold, the output of the LOS detector, LOS (Pin 22), is asserted to Logic 1. The LOS detector's response time is ~500 ns by design, but is dominated by the RC time constant in ac-coupled applications. The LOS pin defaults to active high. However, setting Bit CTRLC[2] to 1, configures the LOS pin as active low.

There is typically 6 dB of electrical hysteresis designed into the LOS detector to prevent chatter on the LOS pin. If the input level drops below the programmed LOS threshold causing the LOS pin to assert, the LOS pin deasserts after the input level increases to 6 dB (2×) above the LOS threshold (see Figure 19).

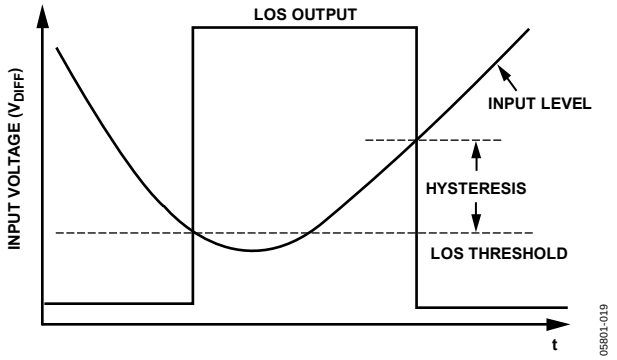


Figure 19. LOS Detector Hysteresis

The LOS detector and the SLICE level adjust can be used simultaneously on the ADN2804. This means that any offset added to the input signal by the SLICE adjust pins does not affect the LOS detector's measurement of the absolute input level.

LOCK DETECTOR OPERATION

The lock detector on the ADN2804 has three modes of operation: normal mode, REFCLK mode, and static LOL mode.

Normal Mode

In normal mode, the ADN2804 is a CDR that locks onto a 622 Mbps data rate without the use of a reference clock as an acquisition aid. In this mode, the lock detector monitors the frequency difference between the VCO and the input data frequency and deasserts the loss of lock signal, which appears on Pin 16, LOL, when the VCO is within 250 ppm of the data frequency. This enables the D/PLL, which pulls the VCO frequency in the remaining amount and acquires phase lock. Once locked, if the input frequency error exceeds 1000 ppm (0.1%), the loss-of-lock signal is reasserted and control returns to the frequency loop, which begins a new frequency acquisition. The LOL pin remains asserted until the VCO locks onto a valid input data stream to within 250 ppm frequency error. This hysteresis is shown in Figure 20.

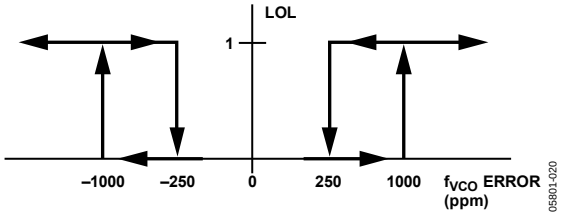


Figure 20. Transfer Function of LOL

LOL Detector Operation Using a Reference Clock

In REFCLK mode, a reference clock is used as an acquisition aid to lock the ADN2804 VCO. Lock-to-reference mode is enabled by setting CTRLA[0] to 1. The user also needs to write to the CTRLA[7, 6] and CTRLA[5:2] bits to set the reference frequency range and the divide ratio of the data rate with respect to the reference frequency. For more details, see the Reference Clock (Optional) section. In this mode, the lock detector monitors the difference in frequency between the divided down VCO and the divided down reference clock. The loss-of-lock signal, which appears on Pin 16, LOL, is deasserted when the VCO is within 250 ppm of the desired frequency. This enables the D/PLL, which pulls the VCO frequency in the remaining amount with respect to the input data and acquires phase lock. Once locked, if the input frequency error exceeds 1000 ppm (0.1%), the loss-of-lock signal is reasserted and control returns to the frequency loop, which reacquires with respect to the reference clock. The LOL pin remains asserted until the VCO frequency is within 250 ppm of the desired frequency. This hysteresis is shown in Figure 20.

Static LOL Mode

The ADN2804 implements a static LOL feature that indicates if a loss-of-lock condition has ever occurred. This feature remains asserted, even if the ADN2804 regains lock, until the static LOL bit is manually reset. The I²C register bit, MISC[4], is the static LOL bit. If there is ever an occurrence of a loss-of-lock condition, this bit is internally asserted to logic high. The MISC[4] bit remains high even after the ADN2804 has reacquired lock to a new data rate. This bit can be reset by writing a 1 followed by 0 to I²C Register Bit CTRLB[6]. Once reset, the MISC[4] bit remains deasserted until another loss-of-lock condition occurs.

Writing a 1 to I²C Register Bit CTRLB[7] causes the LOL pin, Pin 16, to become a static LOL indicator. In this mode, the LOL pin mirrors the contents of the MISC[4] bit and has the functionality described in the previous paragraph. The CTRLB[7] bit defaults to 0. In this mode, the LOL pin operates in the normal operating mode, that is, it is asserted only when the ADN2804 is in acquisition mode and deasserts when the ADN2804 has reacquired lock.

SQUELCH MODES

Two modes for the SQUELCH pin are available with the ADN2804: squelch data outputs and clock outputs mode and squelch data outputs or clock outputs mode. Squelch data outputs and clock outputs mode is selected when CTRLC[1] is 0 (default mode). In this mode, when the SQUELCH input, Pin 27, is driven to a TTL high state, both the data outputs (DATAOUTN and DATAOUTP) and the clock outputs (CLKOUTN and CLKOUTP) are set to the zero state to suppress downstream processing. If the squelch function is not required, Pin 27 should be tied to VEE.

Squelch data outputs or clock outputs mode is selected when CTRLC[1] is 1. In this mode, when the SQUELCH input is driven to a high state, the DATAOUTN and DATAOUTP pins are squelched. When the SQUELCH input is driven to a low state, the CLKOUTN and CLKOUTP pins are squelched. This is especially useful in repeater applications, where the recovered clock may not be needed.

I²C INTERFACE

The ADN2804 supports a 2-wire, I²C-compatible serial bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCK), carry information to and from any device connected to the bus. Each slave device is recognized by a unique address. The ADN2804 has two possible 7-bit slave addresses for both read and write operations. The MSB of the 7-bit slave address is factory programmed to 1. B5 of the slave address is set by Pin 19, SADDR5. Slave Address Bits [4:0] are defaulted to all 0s. The slave address consists of the seven MSBs of an 8-bit word. The LSB of the word either sets a read or write operation (see Figure 7). Logic 1 corresponds to a read operation, while Logic 0 corresponds to a write operation.

To control the device on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCK remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address and the R/W bit). The bits are transferred from MSB to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCK lines, waiting for the start condition and correct transmitted address. The R/W bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADN2804 acts as a standard slave device on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses plus the R/W bit. The ADN2804 has eight subaddresses to enable the user-accessible internal registers (see Table 6 through Table 10). It, therefore, interprets the first byte as the device address and the second byte as the starting subaddress. Auto-increment mode is supported, allowing data to be read from or written to the starting subaddress and each subsequent address without manually addressing the subsequent subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all registers.

Stop and start conditions can be detected at any stage of the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCK high period, the user should issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADN2804 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while reading back in auto-increment mode, then the highest subaddress register contents continue to be output until the master device issues a no acknowledge. This indicates the end of a read. In a no-acknowledge condition, the SDATA line is not pulled low on the ninth pulse. See Figure 8 and Figure 9 for sample write and read data transfers and Figure 10 for a more detailed timing diagram.

Additional Features Available via the I²C Interface

LOS Configuration

The LOS detector output, Pin 22, can be configured to be either active high or active low. If CTRLC[2] is set to Logic 0 (default), the LOS pin is active high when a loss-of-signal condition is detected. Writing a 1 to CTRLC[2] configures the LOS pin to be active low when a loss-of-signal condition is detected.

System Reset

A frequency acquisition can be initiated by writing a 1 followed by a 0 to the I²C Register Bit CTRLB[5]. This initiates a new frequency acquisition while keeping the ADN2804 in its previously programmed operating mode, as set in Registers CTRL[A], CTRL[B], and CTRL[C].

REFERENCE CLOCK (OPTIONAL)

A reference clock is not required to perform clock and data recovery with the ADN2804; however, support for an optional reference clock is provided. The reference clock can be driven differentially or in a single-ended fashion. If the reference clock is not being used, REFCLKP should be tied to VCC, and REFCLKN can be left floating or tied to VEE (the inputs are internally terminated to VCC/2). See Figure 21 through Figure 23 for sample configurations.

The REFCLK input buffer accepts any differential signal with a peak-to-peak differential amplitude of greater than 100 mV (for example, LVPECL or LVDS) or a standard single-ended, low voltage TTL input, providing maximum system flexibility. Phase noise and duty cycle of the reference clock are not critical, and 100 ppm accuracy is sufficient.

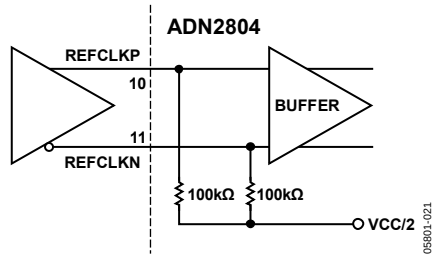


Figure 21. Differential REFCLK Configuration

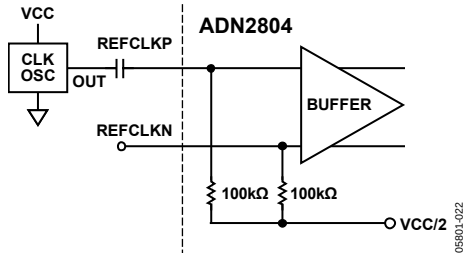


Figure 22. Single-Ended REFCLK Configuration

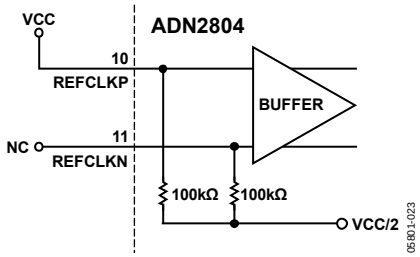


Figure 23. No REFCLK Configuration

There are two mutually exclusive uses, or modes, of the reference clock. The reference clock can be used either to help the ADN2804 lock onto data or to measure the frequency of the incoming data to within 0.01%. The modes are mutually exclusive because in the first use the user knows exactly what the data rate is and wants to force the part to lock onto only that data rate, and in the second use the user does not know what the data rate is and wants to measure it.

Lock-to-reference mode is enabled by writing a 1 to I^2C Register Bit CTRLA[0]. Fine data rate readback mode is enabled by writing a 1 to I^2C Register Bit CTRLA[1]. Writing a 1 to both of these bits at the same time causes an indeterminate state and is not supported.

Using the Reference Clock to Lock onto Data

In this mode, the ADN2804 locks onto a frequency derived from the reference clock according to

$$Data\ Rate/2^{CTRLA[5:2]} = REFCLK/2^{CTRLA[7,\ 6]}$$

The user must provide a reference clock that is a function of the data rate. By default, the ADN2804 expects a reference clock of 19.44 MHz. Other options are 38.88 MHz, 77.76 MHz, and 155.52 MHz, which are selected by programming CTRLA[7, 6]. CTRLA[5:2] should be programmed to [0101] for all cases.

Table 11. CTRLA Settings

CTRLA[7, 6]	Range (MHz)	CTRLA[5:2]	Ratio
00	19.44	0101	2^5
01	38.88	0101	2^5
10	77.76	0101	2^5
11	155.52	0101	2^5

For example, if the reference clock frequency is 38.88 MHz and the input data rate is 622.08 Mbps, CTRLA[7, 6] is set to [01] to produce a divided-down reference clock of 19.44 MHz, and CTRLA[5:2] is set to [0101], that is, 5, because

$$622.08\ Mbps/19.44\ MHz = 2^5$$

In this mode, if the ADN2804 loses lock for any reason, it relocks onto the reference clock and continues to output a stable clock.

While the ADN2804 is operating in lock-to-reference mode, a 0 to 1 transition should be written into the CTRLA[0] bit to initiate a lock-to-reference clock command.

Using the Reference Clock to Measure Data Frequency

The user can also provide a reference clock to measure the recovered data frequency. In this case, the user provides a reference clock, and the ADN2804 compares the frequency of the incoming data to the incoming reference clock and returns a ratio of the two frequencies to within 0.01% (100 ppm) accuracy. The accuracy error of the reference clock is added to the accuracy of the ADN2804 data rate measurement. For example, if a 100 ppm accuracy reference clock is used, the total accuracy of the measurement is within 200 ppm.

The reference clock can range from 10 MHz to 160 MHz. By default, the ADN2804 expects a reference clock between 10 MHz and 20 MHz. If the reference clock is between 20 MHz and 40 MHz, 40 MHz and 80 MHz, or 80 MHz and 160 MHz, the user must configure the ADN2804 for the correct reference frequency range by setting two bits of the CTRLA register, CTRLA[7, 6]. Using the reference clock to determine the frequency of the incoming data does not affect the manner in which the part locks onto data. In this mode, the reference clock is used only to determine the frequency of the data.

Prior to reading back the data rate using the reference clock, the CTRLA[7, 6] bits must be set to the appropriate frequency range with respect to the reference clock being used. A fine data rate readback is then executed as follows:

1. Write a 1 to CTRLA[1]. This enables the fine data rate measurement capability of the ADN2804. This bit is level sensitive and can perform subsequent frequency measurements without being reset.
2. Reset MISC[2] by writing a 1 followed by a 0 to CTRLB[3]. This initiates a new data rate measurement.
3. Read back MISC[2]. If it is 0, the measurement is not complete. If it is 1, the measurement is complete and the data rate can be read back on FREQ[22:0]. The time for a data rate measurement is typically 80 ms.
4. Read back the data rate from FREQ2[6:0], FREQ1[7:0], and FREQ0[7:0].

The data rate can be determined by

$$f_{DATARATE} = \left(FREQ[22.0] \times f_{REFCLK}\right) / 2^{(14 + SEL\_RATE)}$$

where:
FREQ[22:0] is the reading from FREQ2[6:0] (MSB byte, FREQ1[7:0], and FREQ0[7:0] (LSB byte).
$f_{DATARATE}$ is the data rate (Mbps).
f_{REFCLK} is the REFCLK frequency (MHz).
SEL_RATE is the setting from CTRLA[7, 6].

For example, if the reference clock frequency is 32 MHz, SEL_RATE = 1, because the reference frequency falls into the 20 MHz to 40 MHz range, setting CTRLA[7, 6] to [01],. Assume for this example that the input data rate is 622.08 Mb/s (OC12). After following Step 1 through Step 4, the value that is read back on FREQ[22:0] = 0x9B851, which is equal to 637×10^3. Plugging this value into the equation yields

$$637e3 \times 32e6/2^{(14+1)} = 622.08 \text{ Mbps}$$

If subsequent frequency measurements are required, CTRLA[1] should remain set to 1. It does not need to be reset. The measurement process is reset by writing a 1 followed by a 0 to CTRLB[3]. This initiates a new data rate measurement. Follow Step 2 through Step 4 to read back the new data rate.

Note that a data rate readback is valid only if LOL is low. If LOL is high, the data rate readback is invalid.

Table 12.

D22	D21 ... D17	D16	D15	D14 ... D9	D8	D7	D6 ... D1	D0
FREQ2[6:0]			FREQ1[7:0]			FREQ0[7:0]		

APPLICATIONS INFORMATION

PCB DESIGN GUIDELINES

Proper RF PCB design techniques must be used for optimal performance.

Power Supply Connections and Ground Planes

Use of one low impedance ground plane is recommended. The VEE pins should be soldered directly to the ground plane to reduce series inductance. If the ground plane is an internal plane and connections to the ground plane are made through vias, multiple vias can be used in parallel to reduce the series inductance, especially on Pin 23, which is the ground return for the output buffers. The exposed pad should be connected to the GND plane using plugged vias so that solder does not leak through the vias during reflow.

Use of a 22 µF electrolytic capacitor between VCC and VEE is recommended at the location where the 3.3 V supply enters the PCB. When using 0.1 µF and 1 nF ceramic chip capacitors, they should be placed between ADN2804 supply pins VCC and VEE, as close as possible to the ADN2804 VCC pins.

If connections to the supply and ground are made through vias, the use of multiple vias in parallel helps to reduce series inductance, especially on Pin 24, which supplies power to the high speed CLKOUTP/CLKOUTN and DATAOUTP/DATAOUTN output buffers. Refer to Figure 24 for the recommended connections.

By placing the power supply and GND planes adjacent to each other and using close spacing between the planes, excellent high frequency decoupling can be realized. The capacitance is given by

$$C_{PLANE} = 0.88\varepsilon_r A/d\,(\text{pF})$$

where:

ε_r is the dielectric constant of the PCB material.
A is the area of the overlap of power and GND planes (cm^2).
d is the separation between planes (mm).
For FR-4, $\varepsilon_r = 4.4$ and d = 0.25 mm; therefore,
$C_{PLANE} \sim 15.5A$ (pF)

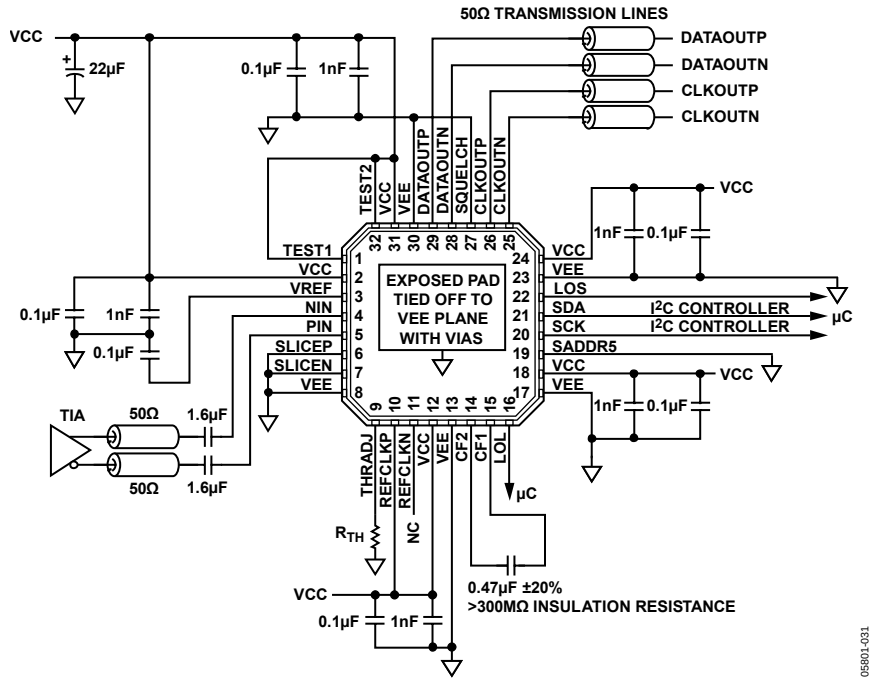


Figure 24. Typical ADN2804 Applications Circuit

Transmission Lines

Minimizing reflections in the ADN2804 requires use of 50 Ω transmission lines for all pins with high frequency input and output signals, including PIN, NIN, CLKOUTP, CLKOUTN, DATAOUTP, and DATAOUTN (also REFCLKP and REFCLKN, if a high frequency reference clock is used, such as 155 MHz). It is also necessary for the PIN/NIN input traces to be matched in length and for the CLKOUTP/CLKOUTN and DATAOUTP/DATAOUTN output traces to be matched in length to avoid skew between the differential traces.

The high speed inputs, PIN and NIN, are internally terminated with 50 Ω to an internal reference voltage (see Figure 25). A 0.1 µF is recommended between VREF, Pin 3, and GND to provide an ac ground for the inputs.

As with any high speed, mixed-signal design, take care to keep all high speed digital traces away from sensitive analog nodes.

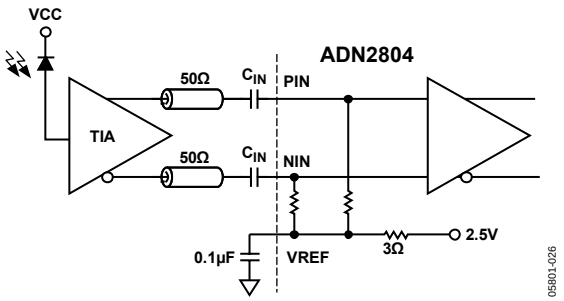


Figure 25. ADN2804 AC-Coupled Input Configuration

Soldering Guidelines for Lead Frame Chip Scale Package

The lands on the 32-lead LFCSP are rectangular. The printed circuit board (PCB) pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a central exposed pad. The pad on the PCB should be at least as large as this exposed pad. The user must connect the exposed pad to VEE using plugged vias so that solder does not leak through the vias during reflow. This ensures a solid connection from the exposed pad to VEE.

Choosing AC Coupling Capacitors

AC coupling capacitors at the input (PIN, NIN) and output (DATAOUTP, DATAOUTN) of the ADN2804 can be optimized for the application. When choosing the capacitors, the time constant formed with the two 50 Ω resistors in the signal path must be considered. When a large number of consecutive identical digits (CIDs) are applied, the capacitor voltage can droop due to baseline wander (see Figure 26), causing pattern-dependent jitter (PDJ).

The user must determine how much droop is tolerable and choose an ac coupling capacitor based on that amount of droop. The amount of PDJ can then be approximated based on the capacitor selection. The actual capacitor value selection can require some trade-offs between droop and PDJ.

For example, assuming that 2% droop can be tolerated, the maximum differential droop is 4%. Normalizing to V p-p:

$Droop = \Delta V = 0.04\ \text{V} = 0.5\ \text{V p-p}\ (1 - e^{-t/\tau})$; therefore, $\tau = 12t$

where:
τ is the RC time constant (C is the ac coupling capacitor, R = 100 Ω seen by C).
t is the total discharge time, which is equal to nT, where n is the number of CIDs, and T is the bit period.

The capacitor value can then be calculated by combining the equations for τ and t:

$$C = 12\ nT/R$$

Once the capacitor value is selected, the PDJ can be approximated as

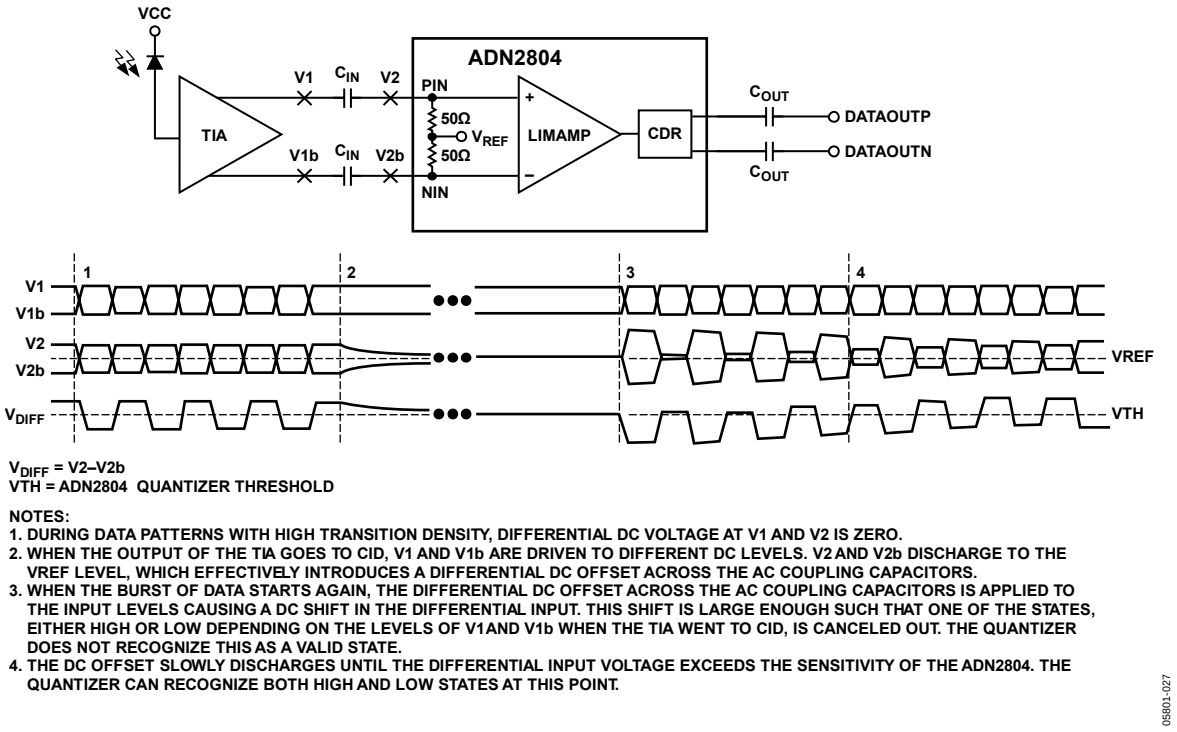
$$PDJ_{pspp} = 0.5\ t_r(1 - e^{(-nT/RC)})/0.6$$

where:

PDJ_{pspp} is the amount of pattern-dependent jitter allowed (<0.01 UI p-p typical).

t_r is the rise time, which is equal to $0.22/BW$, where $BW \sim 0.7$ (bit rate).

Note that this expression for t_r is accurate only for the inputs. The output rise time for the ADN2804 is ~100 ps regardless of the data rate.



V_{DIFF} = V2–V2b
VTH = ADN2804 QUANTIZER THRESHOLD

NOTES:
1. DURING DATA PATTERNS WITH HIGH TRANSITION DENSITY, DIFFERENTIAL DC VOLTAGE AT V1 AND V2 IS ZERO.
2. WHEN THE OUTPUT OF THE TIA GOES TO CID, V1 AND V1b ARE DRIVEN TO DIFFERENT DC LEVELS. V2 AND V2b DISCHARGE TO THE VREF LEVEL, WHICH EFFECTIVELY INTRODUCES A DIFFERENTIAL DC OFFSET ACROSS THE AC COUPLING CAPACITORS.
3. WHEN THE BURST OF DATA STARTS AGAIN, THE DIFFERENTIAL DC OFFSET ACROSS THE AC COUPLING CAPACITORS IS APPLIED TO THE INPUT LEVELS CAUSING A DC SHIFT IN THE DIFFERENTIAL INPUT. THIS SHIFT IS LARGE ENOUGH SUCH THAT ONE OF THE STATES, EITHER HIGH OR LOW DEPENDING ON THE LEVELS OF V1 AND V1b WHEN THE TIA WENT TO CID, IS CANCELED OUT. THE QUANTIZER DOES NOT RECOGNIZE THIS AS A VALID STATE.
4. THE DC OFFSET SLOWLY DISCHARGES UNTIL THE DIFFERENTIAL INPUT VOLTAGE EXCEEDS THE SENSITIVITY OF THE ADN2804. THE QUANTIZER CAN RECOGNIZE BOTH HIGH AND LOW STATES AT THIS POINT.

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Figure 26. Example of Baseline Wander

DC-COUPLED APPLICATION

The inputs to the ADN2804 can also be dc-coupled. This may be necessary in burst mode applications, where there are long periods of CIDs, and baseline wander cannot be tolerated. If the inputs to the ADN2804 are dc-coupled, care must be taken not to violate the input range and common-mode level requirements of the ADN2804 (see Figure 27 through Figure 29). If dc coupling is required and the output levels of the TIA do not adhere to the levels shown in Figure 28, level shifting must be performed and/or an attenuator must be placed between the TIA outputs and the ADN2804 inputs.

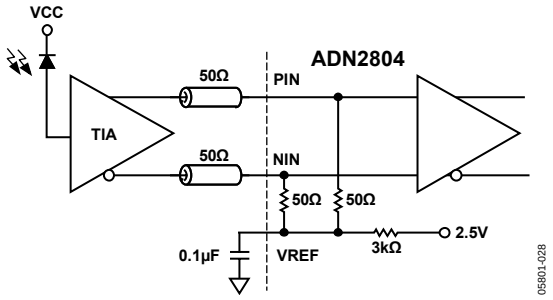


Figure 27. DC-Coupled Application

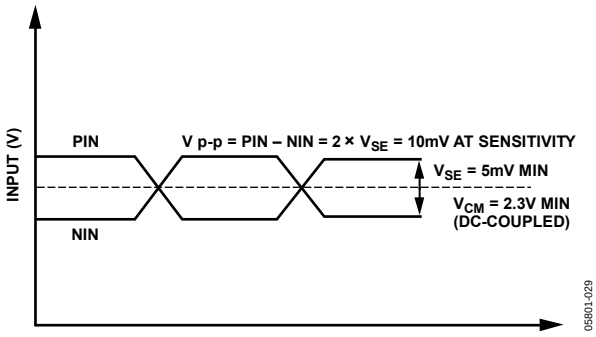


Figure 28. Minimum Allowed DC-Coupled Input Levels

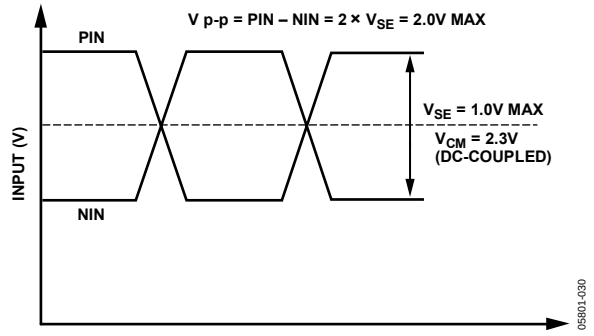
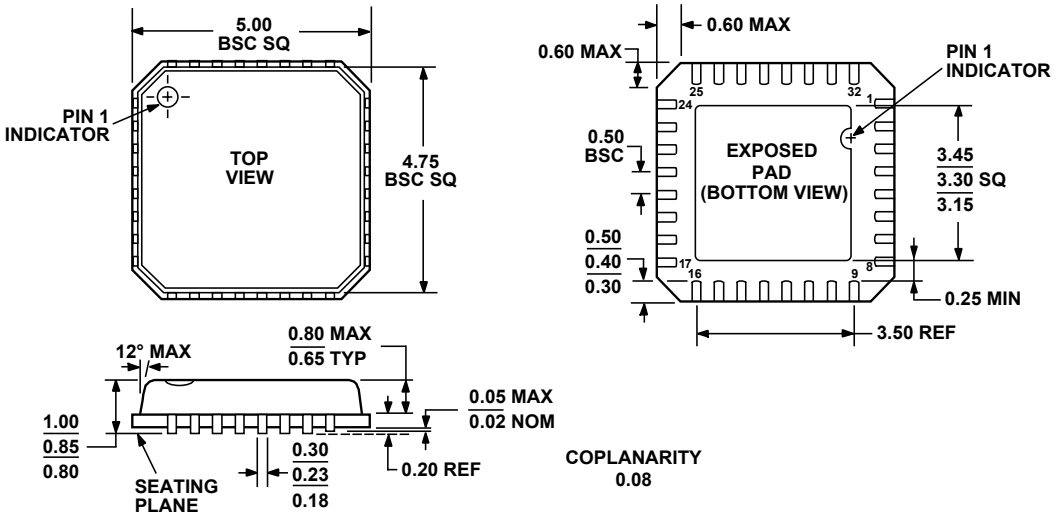


Figure 29. Maximum Allowed DC-Coupled Input Levels

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 30. 32-Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADN2804ACPZ[1]	−40°C to +85°C	32-Lead LFCSP_VQ	CP-32-3
ADN2804ACPZ-500RL7[1]	−40°C to +85°C	32-Lead LFCSP_VQ, Tape-Reel, 500 pieces	CP-32-3
ADN2804ACPZ-RL7[1]	−40°C to +85°C	32-Lead LFCSP_VQ, Tape-Reel, 1500 pieces	CP-32-3
EVAL-ADN2804EB		Evaluation Board	

[1] Z = Pb-free part.

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