Application Note
AP2001 Dual Buck Converter

Contents

1. AP2001 Specification

1.1 Features

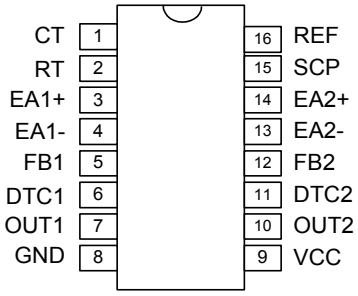
- Dual PWM Control Circuitry
- Operating voltage can be up to 50V
- Adjustable Dead Time Control (DTC)
- Under voltage Lockout (UVLO) Protection
- Short Circuit Protection (SCP)
- Variable Oscillator Frequency..... 500Khz Max
- 2.5V voltage reference Output
- 16-pin PDIP and SOP packages

1.2 General Description

The AP2001 integrates Pulse-width-Modulation (PWM) control circuit into a single chip, mainly designs for power-supply regulator. All the functions included an on-chip 2.5V reference output, two error amplifiers, an adjustable oscillator, two dead-time comparators, UVLO, SCP, DTC circuitry, and dual common-emitter (CE) output transistor circuit. Recommend the output CE transistors as pre-driver for Driving externally. The DTC can provide from 0% to 100%. Switching frequency can be adjustable by trimming RT and CT. During low VCC situation, the UVLO makes sure that the outputs are off until the internal circuit is operational normally.

1.3 Pin Assignments

(Top View)

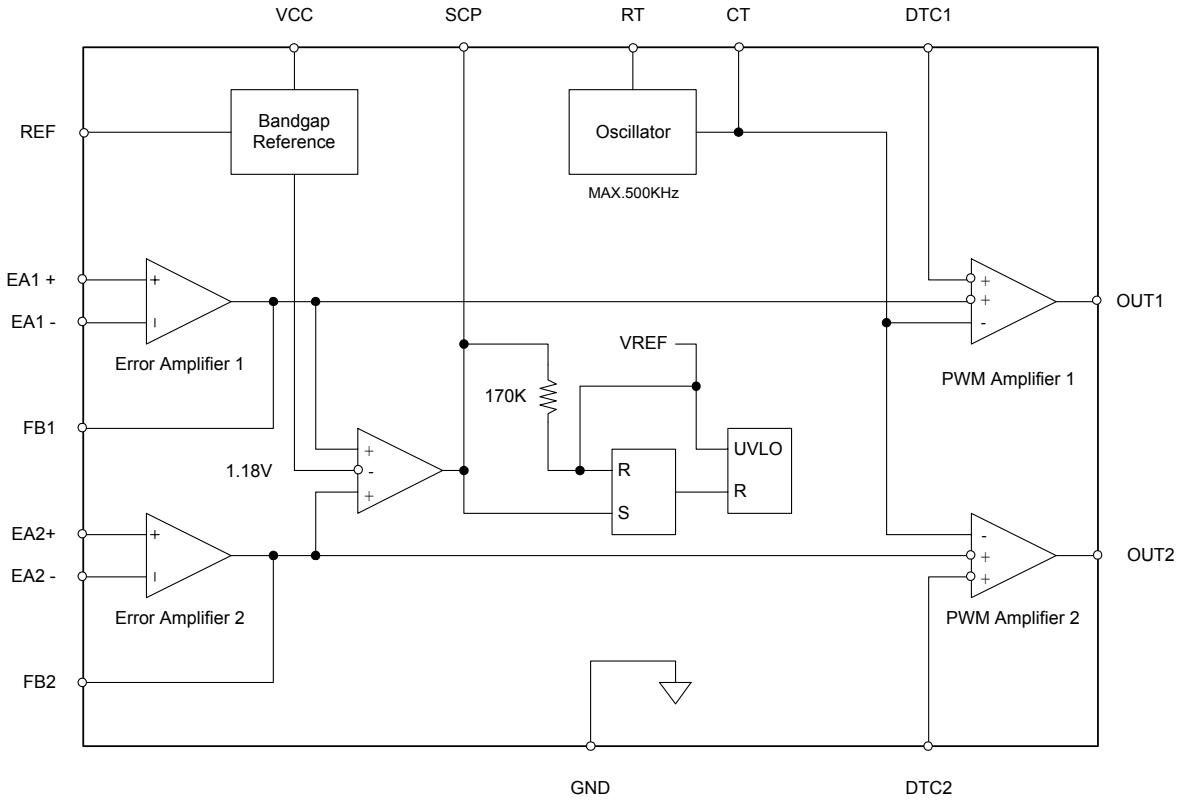


PDIP/SOP

1.4 Pin Descriptions

Name	Description
CT	Timing Capacitor
RT	Timing Resistor
EA+	Error Amplifier Input(+)
EA -	Error Amplifier Input(-)
FB	Feedback Loop Compensation
DTC	Dead Time Control
OUT	Pre-driver Output
GND	Ground
VCC	Supply Voltage
SCP	Short Circuit Protection
REF	Voltage Reference

1.5 Block Diagram



1.6 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage	40	V
V_I	Amplifier input voltage	20	V
V_O	Collector output voltage	40	V
Io	Collector output current	21	mA
T_{OP}	Operating temperature range	-20 to +85	°C
T_{ST}	Storage temperature range	-65 to +150	°C
T_{LEAD}	Lead temperature 1.6 mm(1/16 inch) from case for 10 seconds	260	°C

2. Hardware

2.1 Introduction

The dual-buck demo board supply two constant dc output voltage that are 3.3V and 5V. This board can supply output power up to 15W for buck1 output (5V / 3A) and up to 10W for buck2 output (3.3V / 3A). Using a dc input voltage of 10.8 V to 13.2 V, full load efficiency up to 86 percent. This type of converter converts an unregulated input voltage to 2 regulated output voltage that they are always lower than the input voltage. The control method used in the board is fixed frequency, variable on-time pulse-width-modulation (PWM). The feedback method used is voltage-mode control. Other features of the board include undervoltage lockout (UVLO), short-circuit protection (SCP), and adjustable dead time control (DTC).

2.2 Typical Application

The AP2001 may operate in either the CCM (Continuous Conduction Mode) or the DCM (Discontinuous Conduction Mode). The following applications are designed for CCM (Continuous Conduction Mode) operation. That is, the inductor current is not allowed to fall to zero. To compare the disadvantage and advantage for CCM and DCM, the main disadvantage of CCM is the inherent stability problems (caused by the right-half-plane zero and the double pole in the small-signal control to output voltage transfer function). However, The main disadvantage of DCM that peak currents of switch and diode are larger than CCM when converting. Using power switch and output diode with larger current and power dissipation ratings should solve this issue of large peak current. The designer has to use larger output capacitors, and take more effort on EMI/RFI solution also. Designer could make a choice for each mode. For a low loading current, DCM is preferred for buck. If the load current requirement is high, CCM is preferred for buck. *Figure 1* shows the basic buck topology. When the switch SW is turned on, energy is stored in the inductor L and it has constant voltage "$V_L = V_I - V_O$", the inductor current i_L ramps up at a slope determined by the input voltage. Diode D is off during this period. Once the switch, SW, turns off, diode D starts to conduct and the energy stored in the inductor is released to the load. Current in the inductor ramps down at a slope determined by the difference between the input and output voltages.

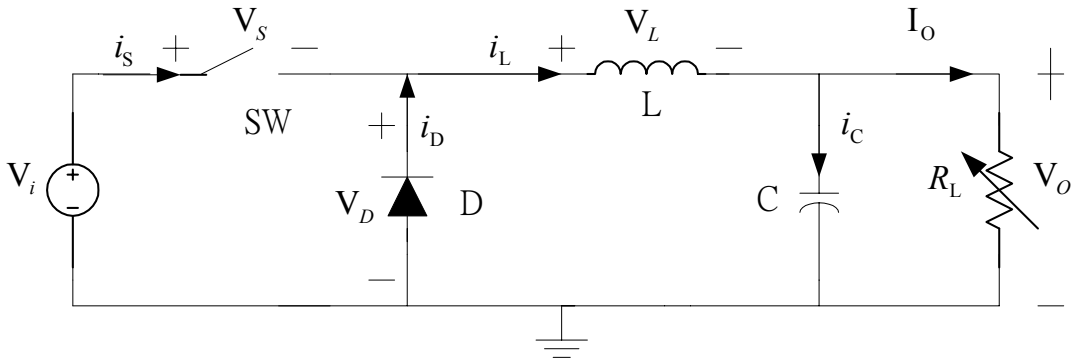


Figure 1. Typical Buck Converter Topology

2.3 Input / Output Connections

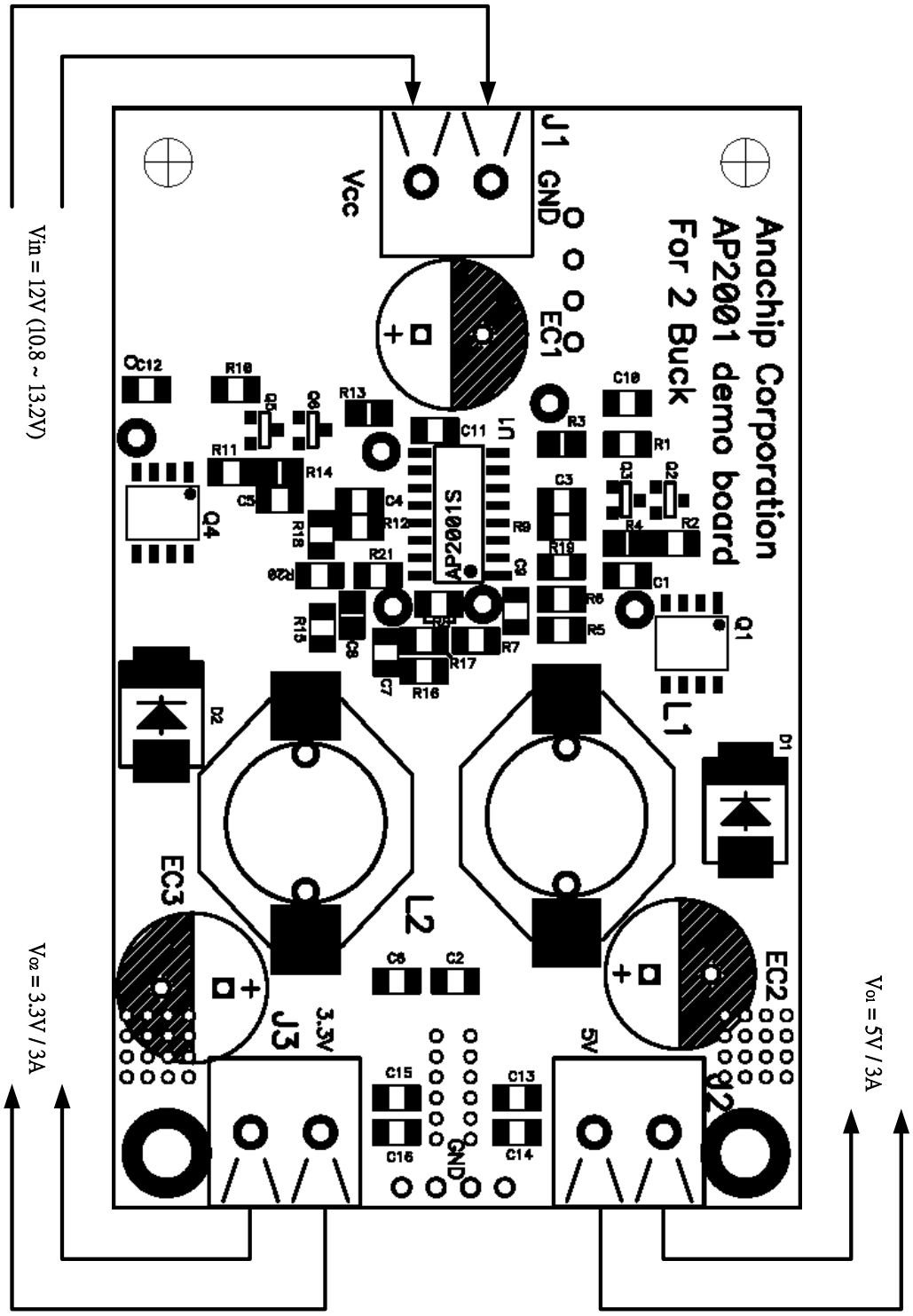


Figure 3. I/O Connections

2.4 Schematic

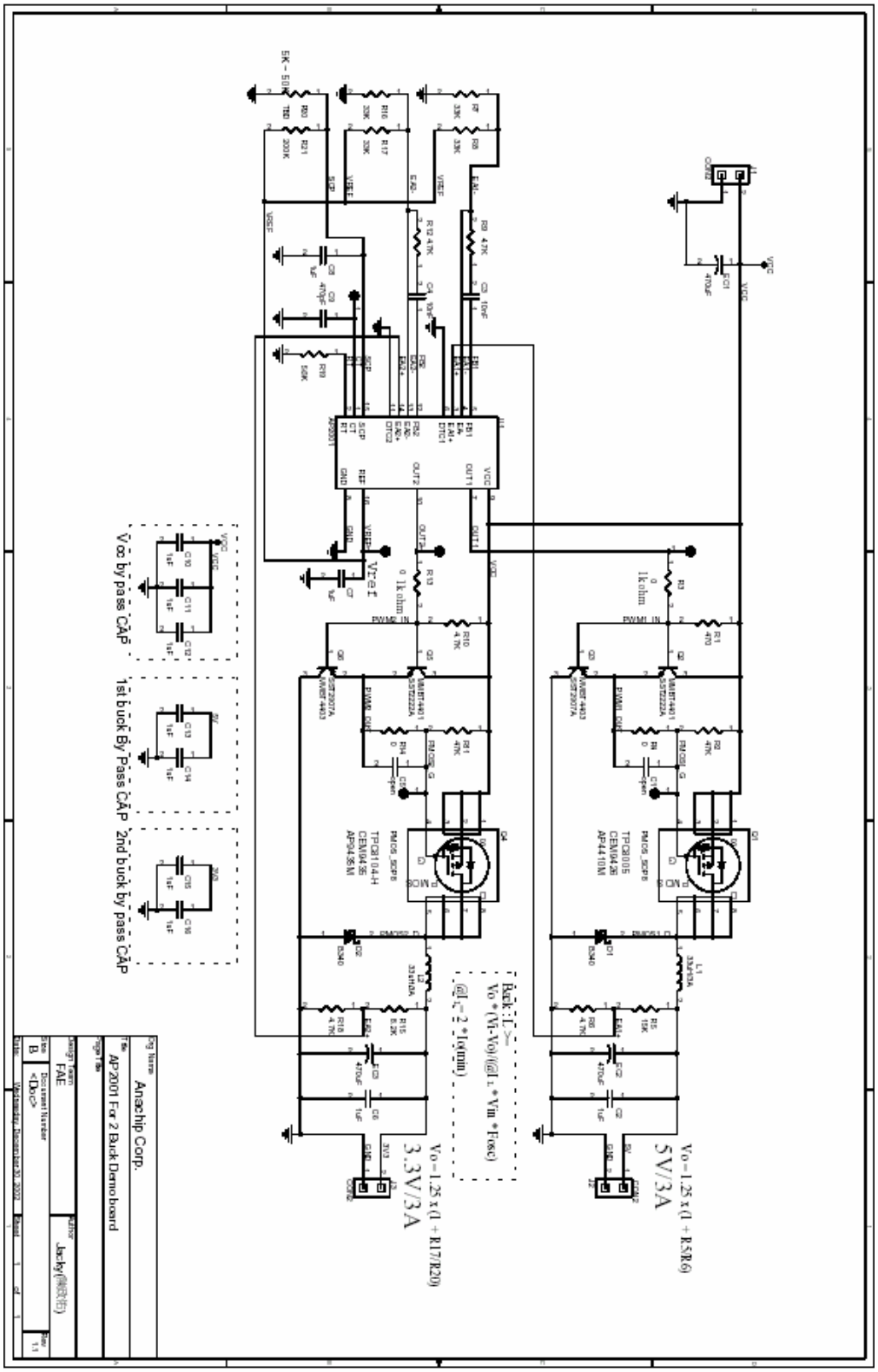


Figure 4. 2_buck demo board schematic

2.5 Board of Materials

No.	Value	Q'ty	Part Reference	Description	Manufacturers	Part Number
1	open	1	C1 C5	Don't install	Philips	
2	1uF	10	C2 C6 C7 C10 C11 C12 C13 C14 C15 C16	Ceramic Chip CAP. 1uF 25V ±10% K X7R 0805	Philips	
3	10nF	2	C3 C4	Ceramic Chip CAP. 10nF 25V ±10% K X7R 0805	Philips	
4	1uF	1	C8	Ceramic Chip CAP. 1uF 25V ±10% K X7R 0805	Philips	
5	470pF	1	C9	Ceramic Chip CAP. 470pF 25V ±10% K X7R 0805	Philips	
6	B340	2	D1 D2	Schottky Diode 3A 40V	DIODES	B340A
7	470uF	3	EC1 EC2 EC3	Electrolysis Capacitors		
8	CON2	3	J1 J2 J3	2P PCB Terminal Block	DINKLE	ELK508V-02P
9	33uH/3A	1	L1 L2	TOROID COILS 33uH 3A	Star Electronics	
10	PMOS_SOP8	2	Q1 Q4	P-Channel MOSFET -30V -3A ↑	CET APEC	CEM4435 AP4435M
11	MMBT4401	2	Q3 Q6	NPN BJT 40V 0.6A SOT-23	ROHM DIODES	SST2222A MMBT4401
12	MMBT4403	2	Q2 Q5	PNP BJT -40V -0.6A SOT-23	ROHM DIODES	SST2907A MMBT4403
13	470	1	R1	Chip Resistance 470 1/8W ±10% J 0805	Yageo(RL Series)	
14	47K	2	R2 R11	Chip Resistance 47K 1/8W ±10% J 0805	Yageo(RL Series)	
15	0	4	R3 R4 R13 R14	Chip Resistance 0 1/8W ±10% J 0805	Yageo(RL Series)	
16	15K	1	R5	Chip Resistance 15K 1/8W ±10% J 0805	Yageo(RL Series)	
17	4.7K	5	R6 R9 R10 R12 R18	Chip Resistance 4.7K 1/8W ±10% J 0805	Yageo(RL Series)	
18	33K	4	R7 R8 R16 R17	Chip Resistance 33K 1/8W ±10% J 0805	Yageo(RL Series)	
19	8.2K	1	R15	Chip Resistance 8.2K 1/8W ±10% J 0805	Yageo(RL Series)	
20	5.6K	1	R19	Chip Resistance 5.6K 1/8W ±10% J 0805	Yageo(RL Series)	
21	TBD	1	R20	To be define (5K ~ 50K)	Yageo(RL Series)	
22	200K	1	R21	Chip Resistance 22K 1/8W ±10% J 0805	Yageo(RL Series)	
23	AP2001	1	U1	Monolithic Dual Channel PWM Controller	Anachip	AP2001S

2.6 Board Layout

Board size is 80mm(W)x50mm(L)

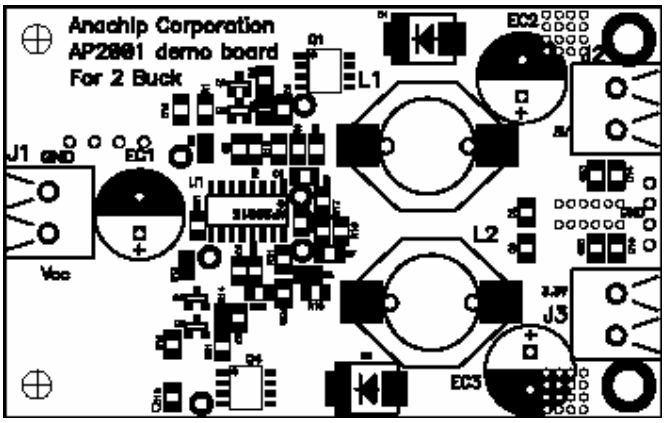


Figure 5. Silkscreen layer

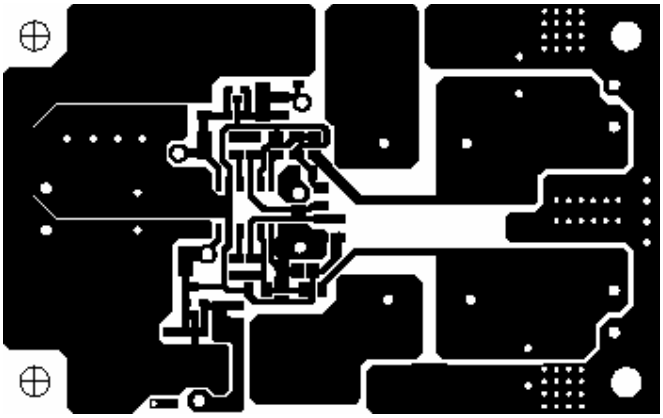


Figure 6. Top layer

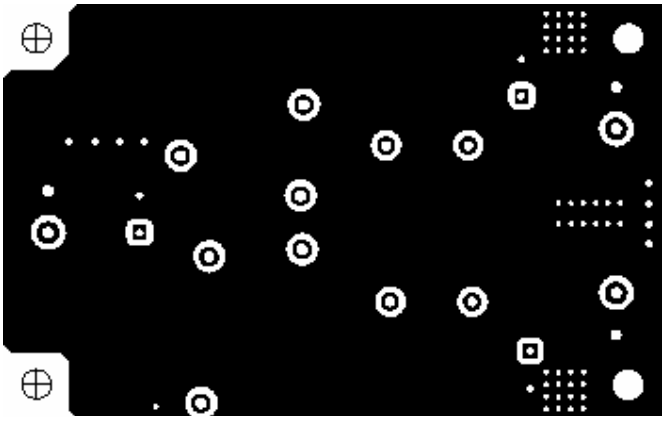


Figure 7. Bottom layer

3. Design Procedure

3.1 Introduction

The AP2001 integrated circuit is dual PWM controller, It operates over a wide input voltage range. This together with its low cost makes it a very popular choice for use in PWM controller. This section will describe the AP2001 to design procedure. The operation and the design of the dual-buck converter will also be discussed in detail.

3.2 Operating Specifications

Specification	Min	Typ	Max	Units
Input Voltage Range	10.8	12	13.2	V
Output Buck1 Voltage Range		5		V
Output Buck2 Voltage Range		3.3		V
Output Current (Buck1) Range	0.3	3		A
Output Current (Buck2) Range	0.3	3		A
Operating Frequency	180	200	220	KHz
Output Ripple		50		mV
Efficiency			86	%

Table 1. Operating Specifications

3.3 Design Procedures

This section describes the steps to design continuous-mode buck and boost converter, and explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop. A switching frequency of 200 kHz was chosen.

Example calculations accompany the design equations. Since this is a fixed output converter, all example calculations apply to the converter with output voltage is 3.3V/5V and input voltage set to 12 V, unless specified otherwise. The first quantity to be determined is the converter the duty cycle value.

$$\text{Duty ratio} \quad D = \frac{V_o + V_d}{V_{in} - V_{ds(sat)}} = \frac{T_{on}}{T_s} \quad , \quad 0 \leqq D \leqq 1$$

Assuming the commutating diode forward voltage V_d = 0.5 V and the power switch on voltage $V_{ds(sat)}$ = 0.1V, the duty cycle for V_o = 3.3V and V_{in} = 10.8, 12, 13.2 is 0.36, 0.32, 0.29 respectively; The duty cycle for V_o = 5V and V_{in} = 10.8, 12, 13.2 is 0.51, 0.46 ,0.42 respectively.

3.3.1 Selection of the buck inductor (L)

A buck converter uses a single-stage LC filter. Choose an inductor to maintain continuous-mode operation down to 10 percent ($I_{o(min)}$) of the rated output load:

ΔI_L = 2 x 10% x I_o = 2 x 0.1 x 3 = 0.6A (For 5V and 3.3V)

The inductor "L" value is:

$$L \geqq \frac{(V_{in} - V_{ds(sat)} - V_o) \times D_{min}}{\Delta I_L \times f_s} = \frac{(13.2 - 0.1 - 3.3) \times 0.29}{0.6 \times (200 \times 10^{3})} = 23.7\,\mu H \quad \text{For 3.3V}$$

$$L \geqq \frac{(V_{in} - V_{ds(sat)} - V_o) \times D_{min}}{\Delta I_L \times f_s} = \frac{(13.2 - 0.1 - 5) \times 0.42}{0.6 \times (200 \times 10^{3})} = 28.4\,\mu H \quad \text{For 5V}$$

So we can choose 33 μH for output voltage "3.3V" and "5V".

3.3.2 Selection of the output capacitor (C_{out})

Assuming that all of the inductor ripple current flows through the capacitor and the effective series resistance (ESR) is zero, the capacitance needed is:

$$C_{out} \geqq \frac{\Delta I_L}{8 \times f_s \times \Delta V_o} = \frac{0.6}{8 \times (200 \times 10^{3}) \times 0.05} = 7.5\,\mu F$$

Assuming the capacitance is very large, the ESR needed to limit the ripple to 50 mV is:

$$ESR \leqq \frac{\Delta V_o}{\Delta I_o} = \frac{0.05}{0.6} = 0.083\,\Omega$$

The output filter capacitor should be rated at least ten times the calculated capacitance and 30–50 percent lower than the calculated ESR. This design used a 470 μF/25V OS-Con capacitor in parallel with a ceramic to reduce ESR.

3.3.3 Selection of the power switch (MOSFET)

Based on the preliminary estimate, $R_{DS(on)}$ should be less than 0.10 V ÷ 3A = 33mΩ. The **CEM4435**(*CET*) is a -30V p-channel MOSFET with $R_{DS(on)}$ = 35mΩ. Power dissipation (conduction + switching losses) can be estimated as:

$$P_{MOSFET} = I_o^2 \times R_{ds(on)} \times D_{max} + [0.5 \times V_{in} \times I_o \times (t_r + t_f) \times f_s]$$

Assuming total switching time (t_r + t_f) is 150 ns, a 55°C maximum ambient temperature, and thermal impedance $R_{\theta JA}$ = 50°C/W , thus:

$$P_{MOSFET} = (3 \times 3 \times 0.035 \times 0.36) + [0.5 \times 12 \times 3 \times (0.15 \times 10^{(-6)}) \times (200 \times 10^{3}) = 0.65W$$

$T_J = T_A + (R_{\theta JA} \times P_{MOSFET}) = 55 + (50 \times 0.65) = 87.5°C$……***(For 3.3V)***

$P_{MOSFET} = (3 \times 3 \times 0.035 \times 0.51) + [0.5 \times 12 \times 3 \times (0.15 \times 10^{(-6)}) \times (200 \times 10^3) = 0.7W$

$T_J = T_A + (R_{\theta JA} \times P_{MOSFET}) = 55 + (50 \times 0.7) = 90°C$……***(For 5V)***

3.3.4 Selection of the Rectifier (D)

The catch rectifier conducts during the time interval when the MOSFET is off. The **B340** (*DIODES*) is a 3A, 40V schottky rectifier in a SMC power surface-mount package. The power dissipation is:

$P_D = I_o \times V_d \times (1 - D_{min}) = 3 \times 0.5 \times (1 - 0.29) = 1.065W$……***(For 3.3V)***

$P_D = I_o \times V_d \times (1 - D_{min}) = 3 \times 0.5 \times (1 - 0.42) = 0.87W$……..***(For 5V)***

Assuming a 55°C maximum ambient temperature, and thermal impedance $R_{\theta JA}$ = 15°C/W , thus:

$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (15 \times 1.065) = 70.975°C$…….. ***(For 3.3V)***

$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (15 \times 0.87) = 68.05°C$…….. ***(For 5V)***

3.3.5 Selection of the input capacitor (C_{in})

The RMS current rating of the input capacitor can be calculated from the following formula. The capacitor manufacturers data sheet must be checked to assure that this current rating is not exceeded.

$I_{in(rms)} = 2\sqrt{[D \times (I_{o(max)} + I_{o(min)}) \times (I_{o(max)} - I_{o(min)}) + (\triangle I_L{}^2)/3]} = \sqrt{[0.36 \times (3 + 0.3) \times (3 - 0.3) + 0.36/3]}$

$= 2 \times 1.8A = 3.6A$

This capacitor should be located close to the IC using short leads and the voltage rating should be approximately 2 times the maximum input voltage. We select input capacitor value “470uF/25V”.

4. Voltage monitor by AP434

In some applications, the output voltage is concerned too high to damage the IC. To avoid the IC being damaged, comparing output voltage with a reference could monitor the output voltage. AP434 is a monolithic IC that includes one independent OP-Amp and another OP-Amp, which the non-inverting input is wired to a fixed voltage reference. AP434 data sheet provides the low cost and space saving of voltage monitoring function.

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