



ALPHA & OMEGA
SEMICONDUCTOR

AOB403

P-Channel Enhancement Mode Field Effect Transistor

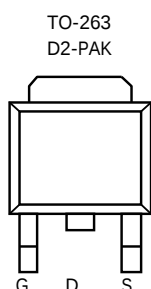


General Description

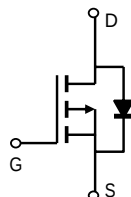
The AOB403 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. With the excellent thermal resistance of the D2-PAK package, this device is well suited for high current load applications. *Standard product AOB403 is Pb-free (meets ROHS & Sony 259 specifications). AOB403L is a Green Product ordering option. AOB403 and AOB403L are electrically identical.*

Features

V_{DS} (V) = -60V
 I_D = -30A (V_{GS} = -10V)
 $R_{DS(ON)} < 44m\Omega$ (V_{GS} = -10V) @ 30A
 $R_{DS(ON)} < 55m\Omega$ (V_{GS} = -4.5V) @ 20A



Top View
Drain Connected to
Tab



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$ -30	A
		$T_C=100^\circ\text{C}$ -20	
Pulsed Drain Current ^C	I_{DM}	-60	
Avalanche Current ^C	I_{AR}	-26	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	134	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$ 83	W
		$T_C=100^\circ\text{C}$ 42	
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$ 2.2	W
		$T_A=70^\circ\text{C}$ 1.45	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10\text{s}$ 10	12	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State 45	55	$^\circ\text{C/W}$
Maximum Junction-to-Case ^C	$R_{\theta JC}$	Steady-State 1.35	1.8	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-48V, V _{GS} =0V T _J =55°C		-0.003	-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1	-1.9	-3	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-60			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-30A T _J =125°C		36 51	44 62	mΩ
		V _{GS} =-4.5V, I _D =-20A		43	55	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-30A		50		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.73	-1	V
I _S	Maximum Body-Diode Continuous Current				-30	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-30V, f=1MHz		2977	3600	pF
C _{oss}	Output Capacitance			241		pF
C _{rss}	Reverse Transfer Capacitance			153		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		2	2.4	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge (10V)	V _{GS} =-10V, V _{DS} =-30V, I _D =-30A		44.6	54	nC
Q _g (4.5V)	Total Gate Charge (4.5V)			20.8	25	nC
Q _{gs}	Gate Source Charge			9.9		nC
Q _{gd}	Gate Drain Charge			10		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-30V, R _L =1Ω, R _{GEN} =3Ω		13.7		ns
t _r	Turn-On Rise Time			8.3		ns
t _{D(off)}	Turn-Off DelayTime			37		ns
t _f	Turn-Off Fall Time			9.7		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-30A, dI/dt=100A/μs		40	48	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-30A, dI/dt=100A/μs		56		nC

A: The value of R_{qJA} is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation PDSM is based on R_{qJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation PD is based on T_J(MAX)=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_J(MAX)=175°C.

D: The R_{qJA} is the sum of the thermal impedance from junction to case R_{qJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 ms pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_J(MAX)=175°C.

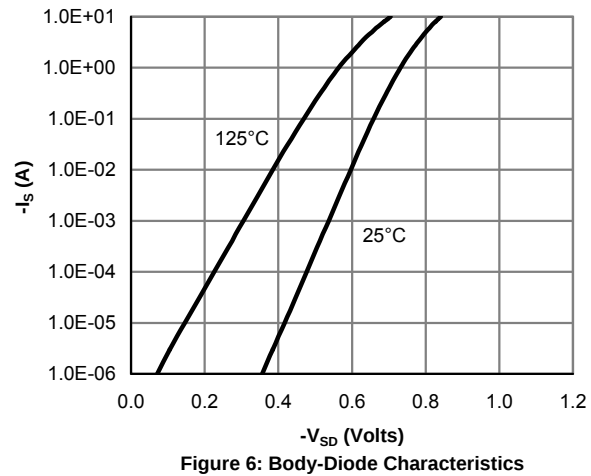
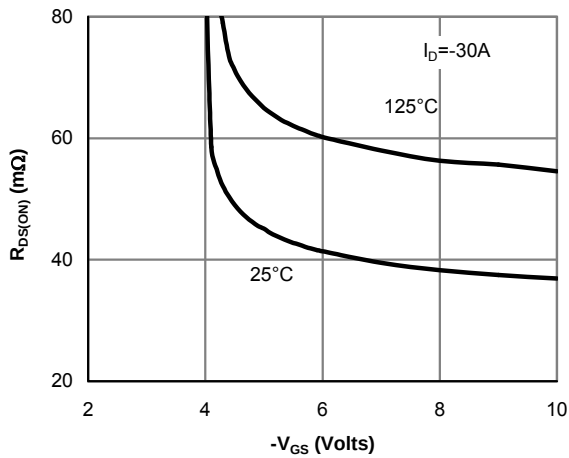
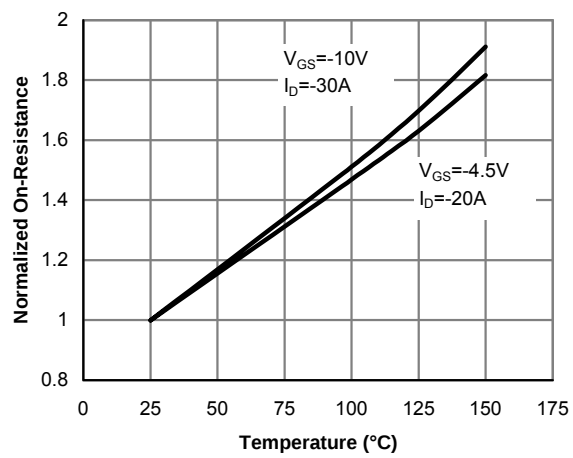
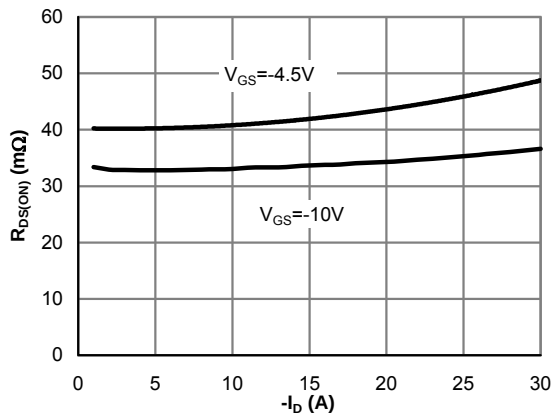
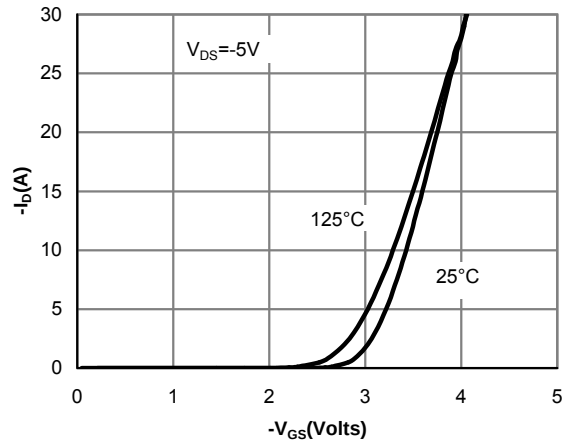
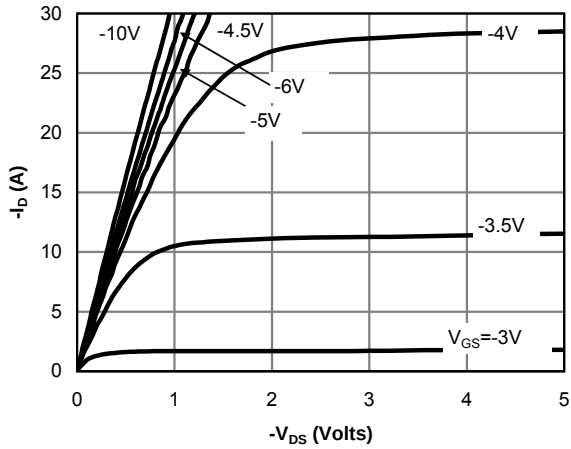
G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

Rev1:May2005

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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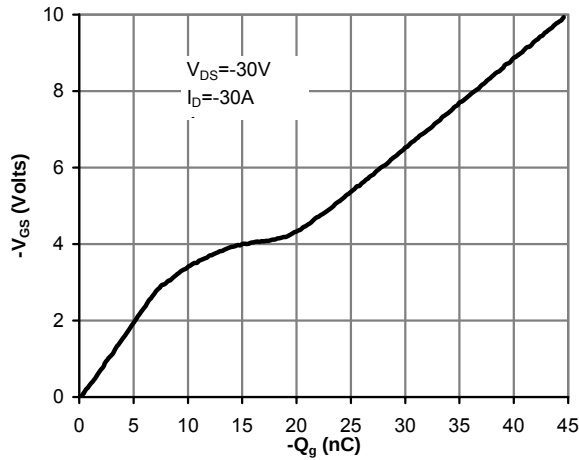


Figure 7: Gate-Charge Characteristics

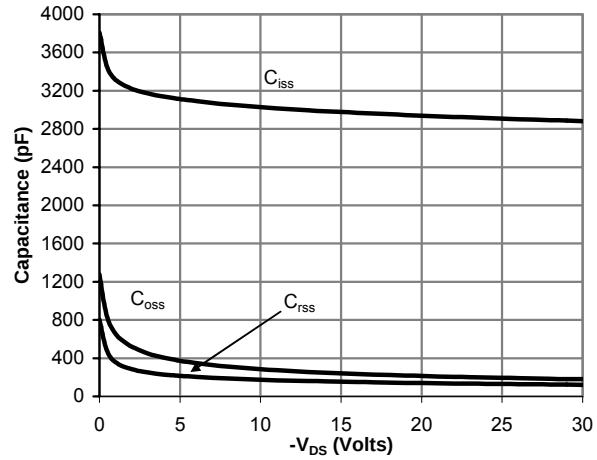


Figure 8: Capacitance Characteristics

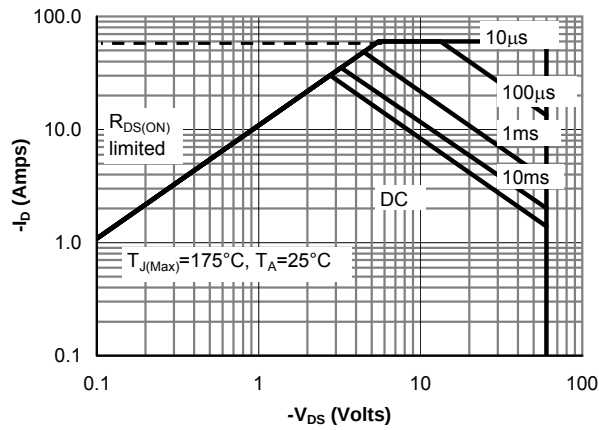


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

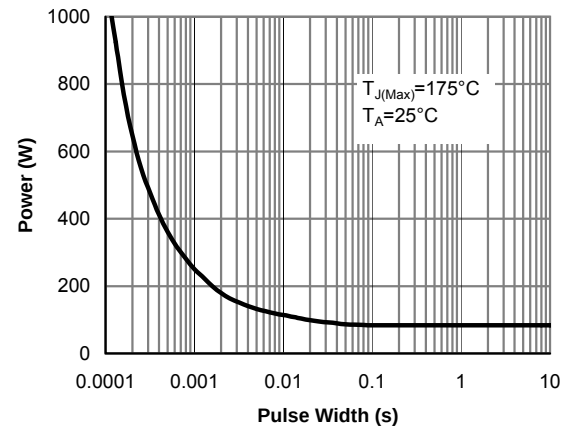


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

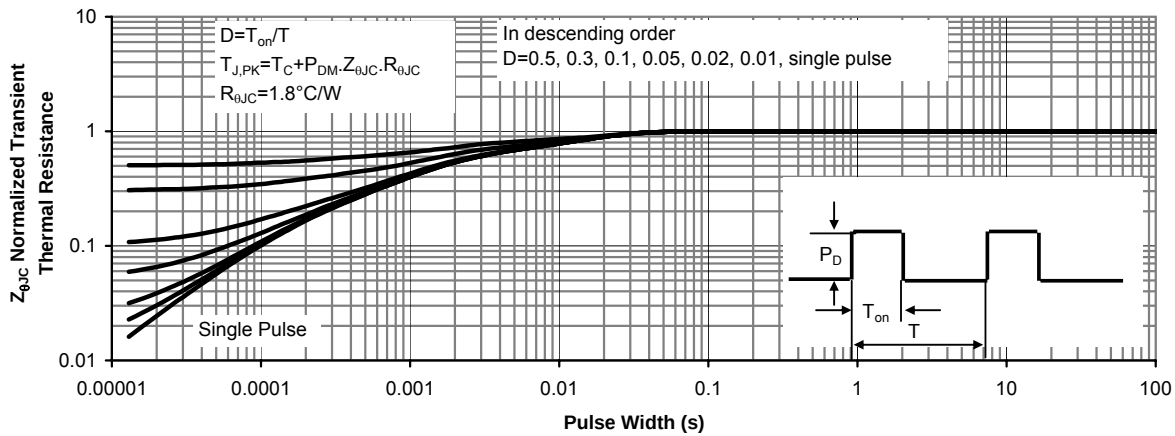


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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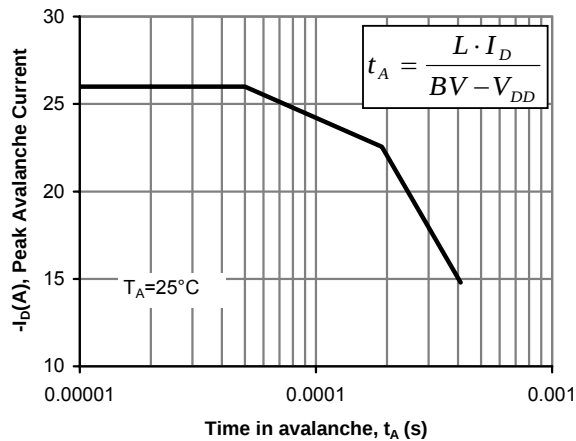


Figure 12: Single Pulse Avalanche capability

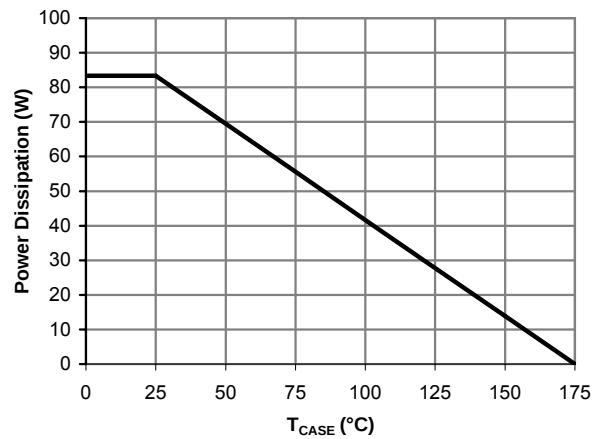


Figure 13: Power De-rating (Note B)

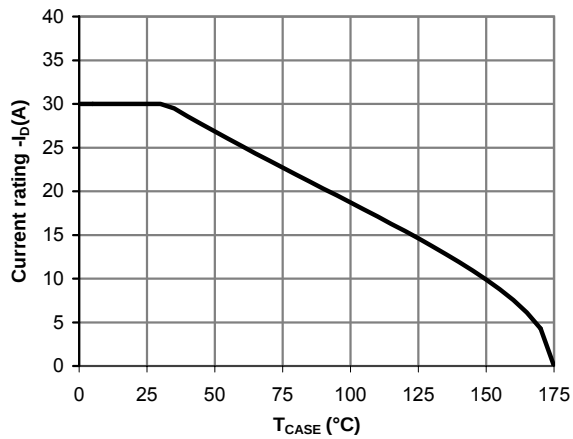


Figure 14: Current De-rating (Note B)

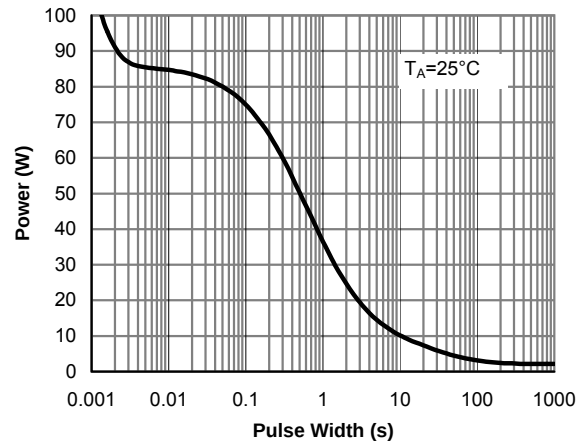


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

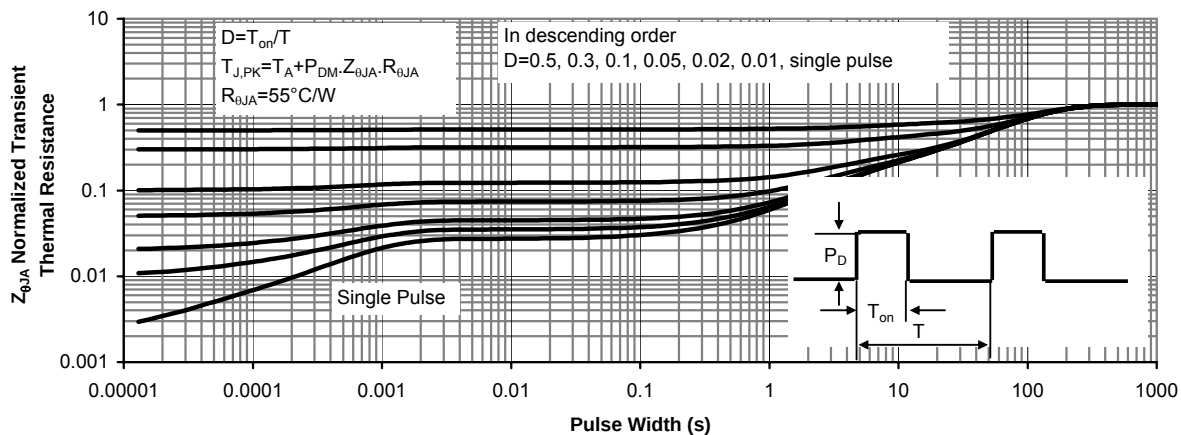


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)