

AOP806

Dual N-Channel Enhancement Mode Field Effect Transistor

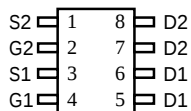
General Description

The AOP806 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications.
Standard Product AOP806 is Pb-free (meets ROHS & Sony 259 specifications).

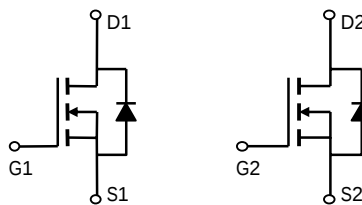
Features

V_{DS} (V) = 75V
 I_D = 3.4A (V_{GS} = 10V)
 $R_{DS(ON)}$ < 132m Ω (V_{GS} = 10V)
 $R_{DS(ON)}$ < 168m Ω (V_{GS} = 4.5V)

UIS TESTED!
Rg,Ciss,Coss,Crss Tested



PDIP-8



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum		Units
		10 Sec	Steady State	
Drain-Source Voltage	V_{DS}	75		V
Gate-Source Voltage	V_{GS}	± 25		V
Continuous Drain Current ^{AF}	$T_A=25^\circ\text{C}$	3.4	2.7	A
	$T_A=70^\circ\text{C}$	2.7	2.1	
Pulsed Drain Current ^B	I_{DM}	15		
Power Dissipation	$T_A=25^\circ\text{C}$	2.5	1.6	W
	$T_A=70^\circ\text{C}$	1.6	1	
Avalanche Current ^B	I_{AR}	10		A
Repetitive avalanche energy 0.3mH ^B	E_{AR}	15		mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ\text{C}$

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10\text{s}$	$R_{\theta JA}$	40	50	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	Steady-State		67	80	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	Steady-State	$R_{\theta JL}$	33	40	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =10mA, V _{GS} =0V	75			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =75V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±25V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	2.3	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	15			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =3.4A T _J =125°C		108 162	132 198	mΩ
		V _{GS} =4.5V, I _D =2A		128	168	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =3.4A		10		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.77	1	V
I _S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, f=1MHz		290	380	pF
C _{oss}	Output Capacitance			54		pF
C _{rss}	Reverse Transfer Capacitance			24		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		2.4	3.5	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =30V, I _D =3.4A		5.1	7	nC
Q _g (4.5V)	Total Gate Charge			2.3		nC
Q _{gs}	Gate Source Charge			1.0		nC
Q _{gd}	Gate Drain Charge			1.2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =30V, R _L =8.8Ω, R _{GEN} =3Ω		4		ns
t _r	Turn-On Rise Time			3.4		ns
t _{D(off)}	Turn-Off DelayTime			14.4		ns
t _f	Turn-Off Fall Time			2.4		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =3.4A, dI/dt=100A/μs		30.2	45	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =3.4A, dI/dt=100A/μs		21.5		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F. The current rating is based on the t_s ≤ 10s thermal resistance rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

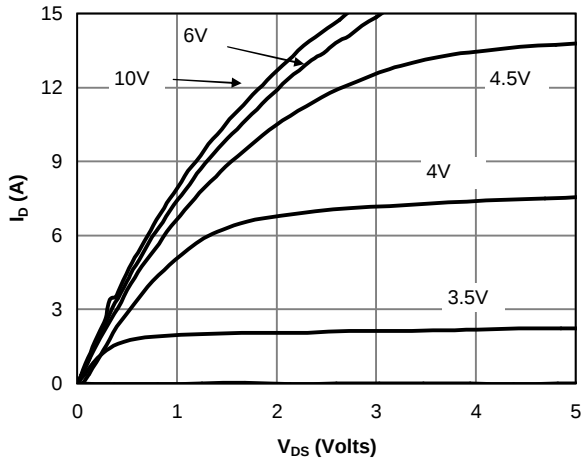


Figure 1: On-Region Characteristics

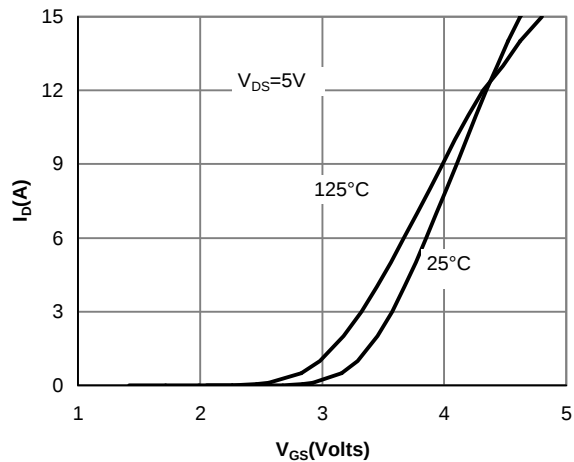


Figure 2: Transfer Characteristics

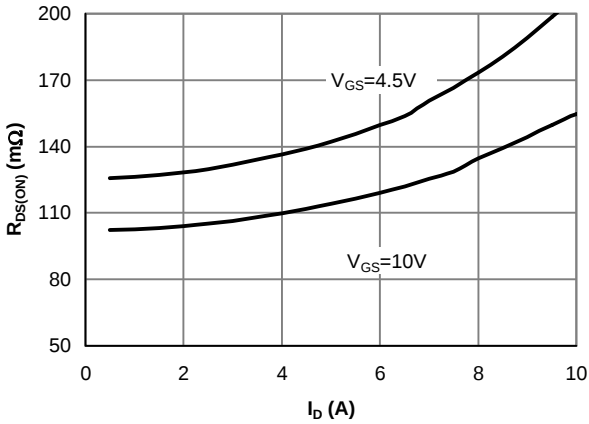


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

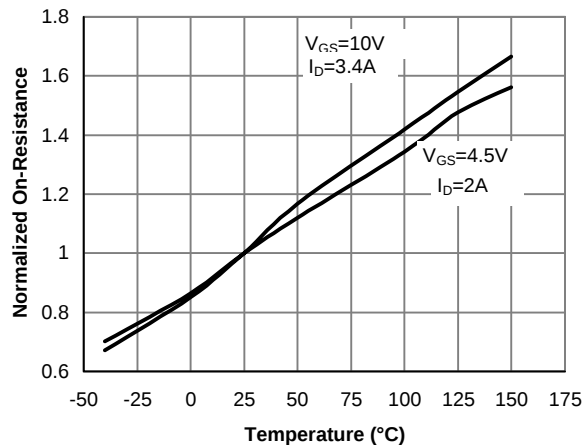


Figure 4: On-Resistance vs. Junction Temperature

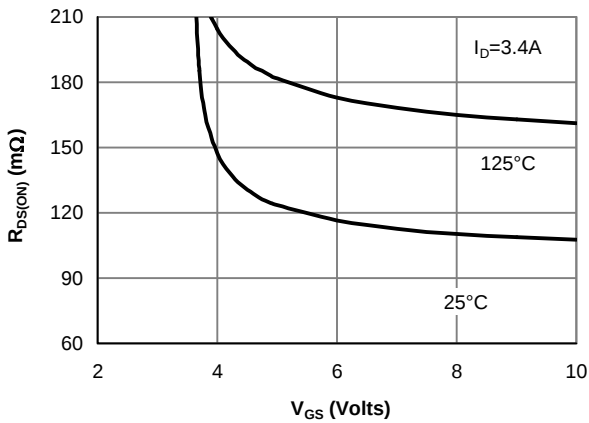


Figure 5: On-Resistance vs. Gate-Source Voltage

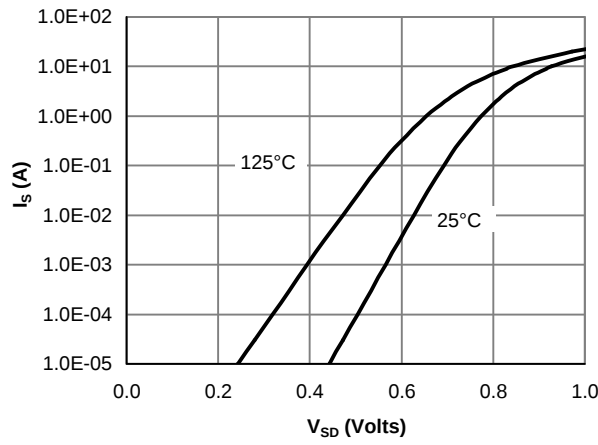


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

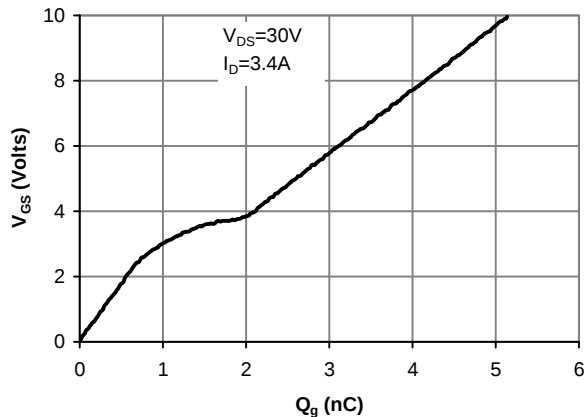


Figure 7: Gate-Charge Characteristics

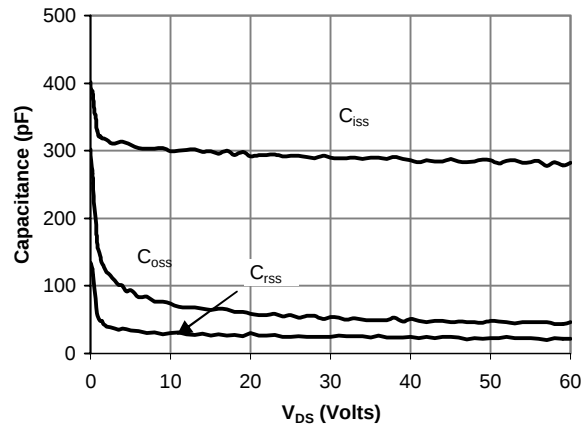


Figure 8: Capacitance Characteristics

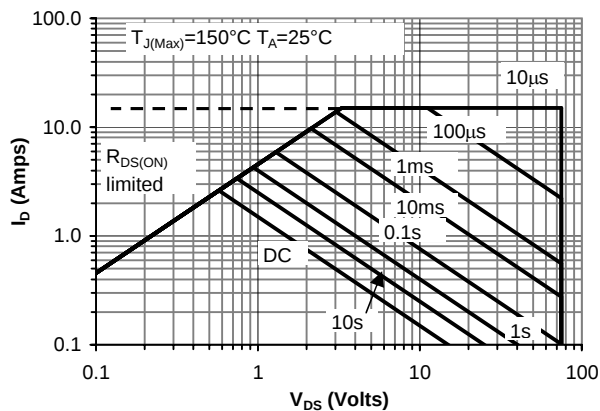


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

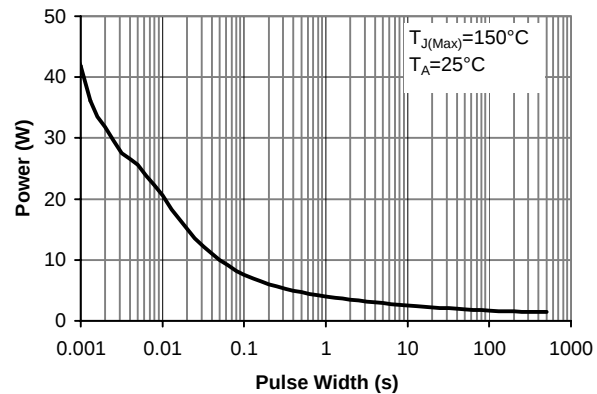


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

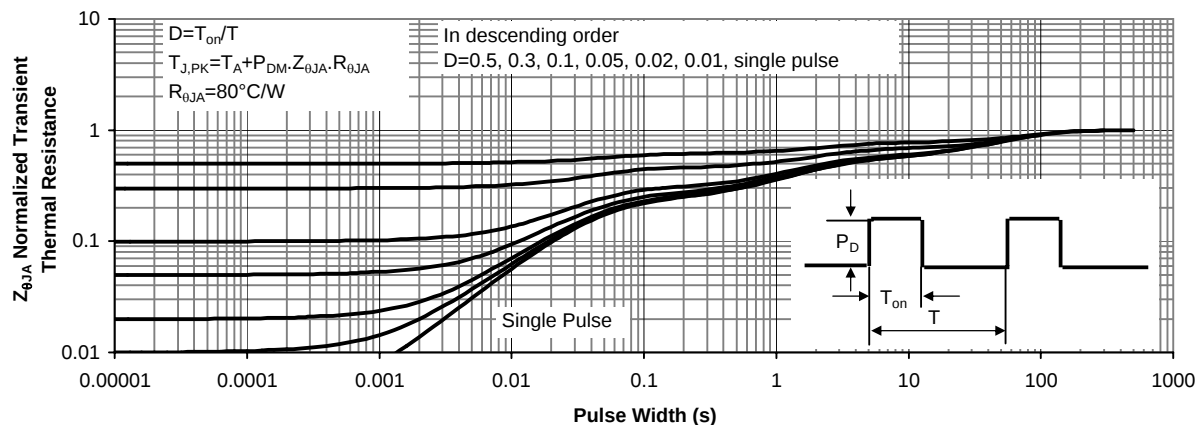


Figure 11: Normalized Maximum Transient Thermal Impedance