T-03-15

VARO®

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DLS 061

3 Amp Schottky Barrier Rectifiers

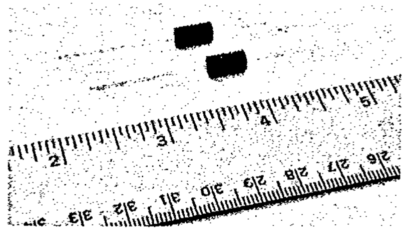
January 1980

20 Volt, 30 Volt and 40 Volt V_{RRM}

.475 Volt v_F at i_F = 3.0 Amp

Very Fast Recovery Time

Minimum Sized, Low Cost Epoxy Encapsulation

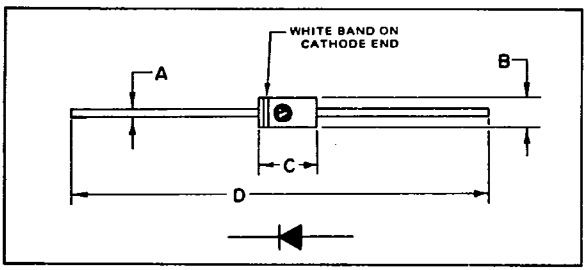


MAXIMUM RATINGS (At T_A = 25°C unless otherwise noted)	SYMBOL	VSK320	VSK330	VSK340	UNITS
DC Blocking Voltage Working Peak Reverse Voltage Peak Repetitive Reverse Voltage	V_{RM} V_{RWM} V_{RRM}	20	30	40	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	14	21	28	Volts
Average Rectified Forward Current (Fig. 5 & 6)	I_o		3.0		Amps
Ambient Temp. @ Rated V_{RM}, $R_{\theta JA} \leq 24°$ C/W	T_A	85	80	75	°C
Peak Surge Current (non-rep), 300µs Pulse Width (Fig.4)	I_{FSM}		250		Amps
Peak Surge Current (non-rep), ½ cycle, 60Hz (Fig. 4)	I_{FSM}		150		Amps
Operating Junction Temperature	T_J		–65 to +150*		°C
Storage Temperature	T_{STG}		–65 to +150		°C

* $V_{RM} \leq 0.1\ V_{RM}$ Max, $R_{\theta JA} \leq 32°$ C/W

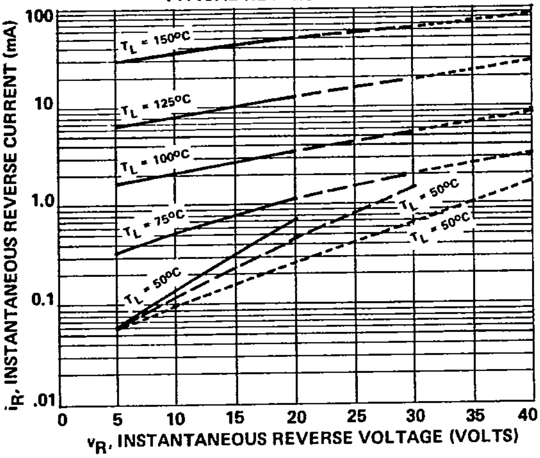
ELECTRICAL CHARACTERISTICS (At T_A = 25°C unless otherwise noted)	SYMBOL	VSK320	VSK330	VSK340	UNITS
Maximum Instantaneous Forward Voltage Drop (1) See Fig. 2 for Typical v_F — i_F = 1.0 Amp i_F = 3.0 Amps i_F = 10.0 Amps	v_F		.400 .475 .750		Volts
Maximum Instantaneous Reverse Current at Rated V_{RM} (1) See Fig. 1 for Typical i_R — T_L = 25° C T_L = 100° C	i_R		3.0 30.0		mA

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2%



LTR.	INCHES	MILLIMETERS
A	.048 — .052 Dia.	1,22 — 1,32 Dia.
B	.190 — .225	4,83 — 5,72
C	.370 — .390	9,40 — 9,91
D	2.75	69,85

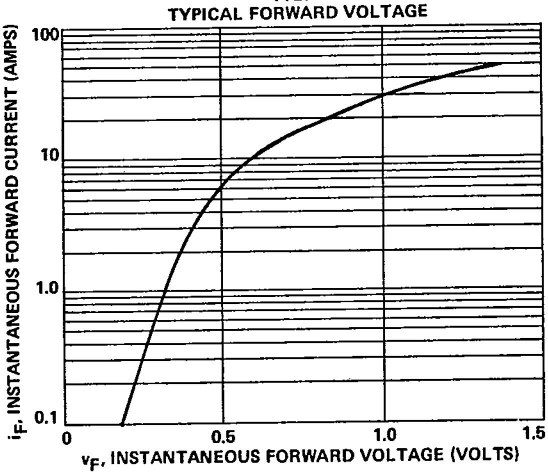
FIG. 1.
TYPICAL REVERSE CURRENT



VSK320
VSK330
VSK340
PULSE WIDTH - 300 μsec

T_L = LEAD TEMP. MEASURED .03"–.79mm FROM RECTIFIER BODY WITH 40 GAUGE THERMOCOUPLE

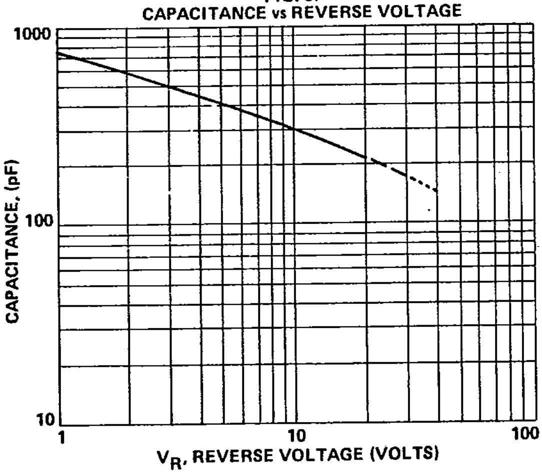
FIG. 2.
TYPICAL FORWARD VOLTAGE



PULSE WIDTH = 300 μsec

T_A = 25°C

FIG. 3.
CAPACITANCE vs REVERSE VOLTAGE



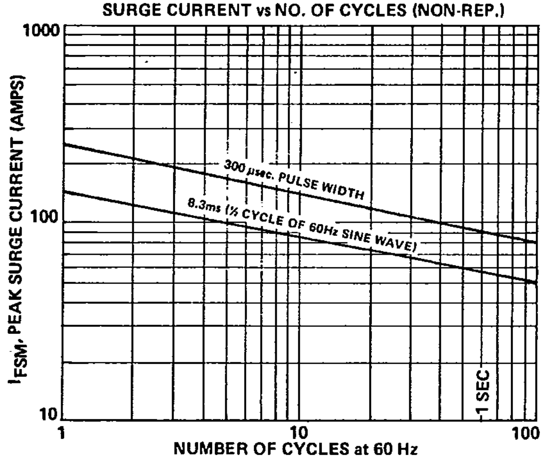
VSK320
VSK330
VSK340
T_A = 25°C
TEST FREQ. = 100 kHz

The current flow in a Schottky barrier rectifier is due to majority carrier conduction and is not affected by reverse recovery transients due to stored charge and minority carrier injection as in conventional PN diodes.

The Schottky barrier rectifier may be considered for purposes of circuit analysis, as an ideal diode in parallel with a variable capacitance equal in value to the junction capacitance. See Figure 3.

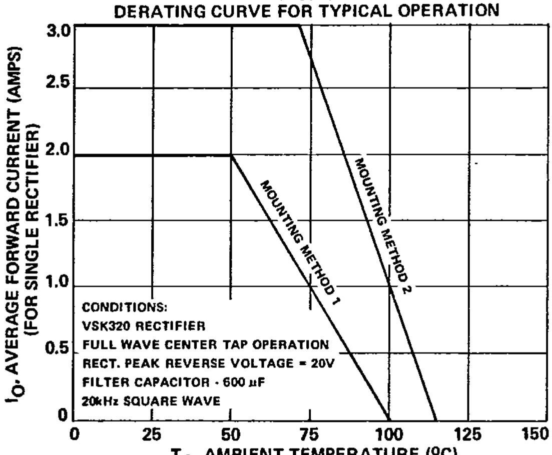
3 Amp Schottky Barrier Rectifiers

FIG. 4.
SURGE CURRENT vs NO. OF CYCLES (NON-REP.)

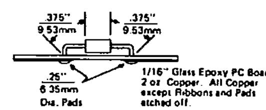


T_A = 25°C

FIG. 5.
DERATING CURVE FOR TYPICAL OPERATION



MOUNTING METHOD 1



MOUNTING METHOD 2 – TOP VIEW

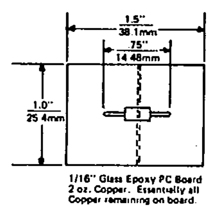
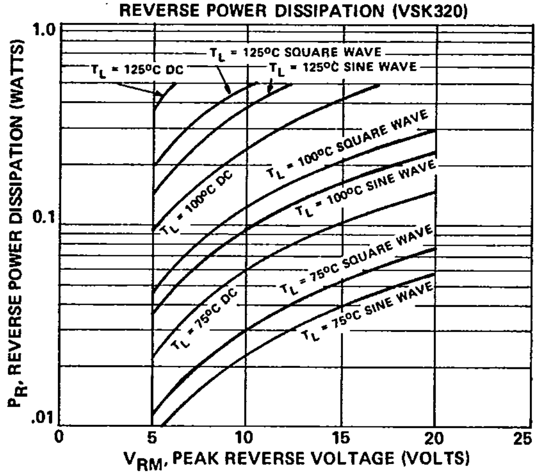
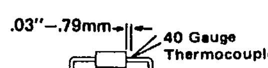


FIG. 6(A).
REVERSE POWER DISSIPATION (VSK320)





REVERSE POWER MULTIPLIES 1.32x FOR EACH 5°C TEMP. INCREASE.

USE THIS MULTIPLIER FOR INTERPOLATION BETWEEN CURVES SHOWN ON FIGURES 6(A), 6(B), 6(C),

USE 75°C CURVES FOR ALL CASE TEMP. BELOW 75°C.

FIG. 6(B)
REVERSE POWER DISSIPATION (VSK330)

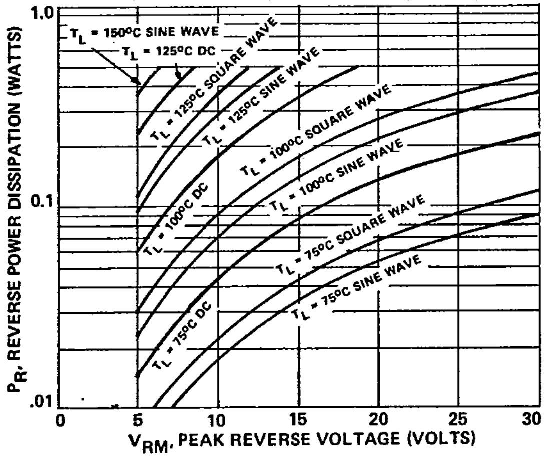


FIG. 6(C)
REVERSE POWER DISSIPATION (VSK340)

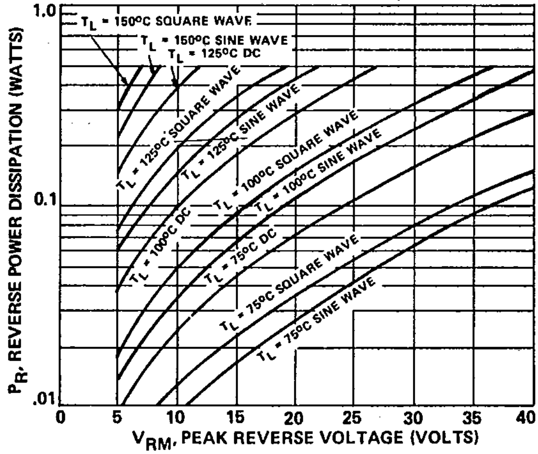


FIG. 6(D).
FORWARD POWER DISSIPATION
VSK320, VSK330, VSK340

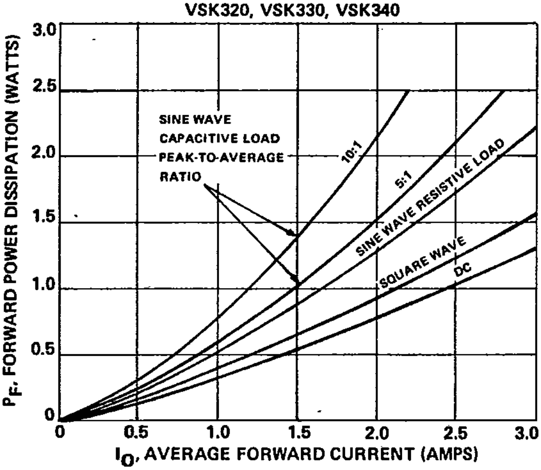
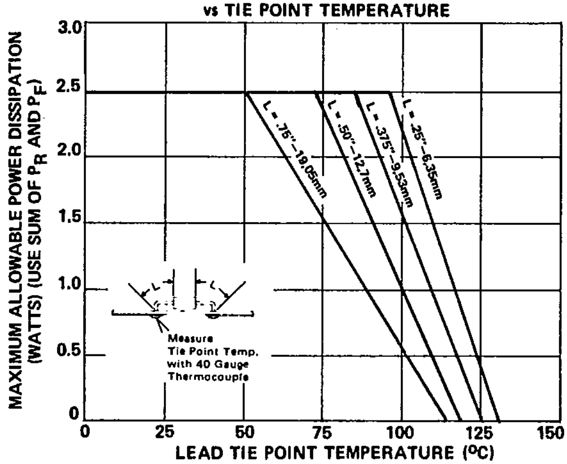


FIG. 6(E)
MAXIMUM ALLOWABLE POWER DISSIPATION
vs TIE POINT TEMPERATURE



Thermal Considerations:

1. The derating curve of figure 5 may be used for initial design work.
2. Use the curves of figure 6 to study the voltage / current / temperature parameters. These curves are helpful in determining the rectifier capability when connected to a tie point whose temperature is influenced by other heat producing components. To use these curves, add the reverse power dissipation from figure 6 (A), (B) or (C) to the forward power dissipation from figure 6 (D) then go to figure 6 (E) to find the maximum allowable tie point temperature.
3. The heat sink design (tie point) must be designed to keep the temperature at this point below that shown on the figure 6 (E) curve. Thermal runaway is entirely possible on marginal designs due to the inherently large reverse leakage of Schottky barrier rectifiers and the fact that reverse power multiplies about 1.32 times for each 5° C of temperature increase.
4. The curves of figure 6 (E) were based on full rated reverse bias voltage. Slightly higher tie point temperatures can be tolerated at lower voltages. We recommend that all designs be verified at an ambient temperature at least 10° C higher than the maximum at which the equipment will ever have to operate.
5. If the application is such that DC reverse bias is applied nearly 100% of the time, all temperature points on curve 6 (E) should be reduced 13° C.
6. These thermal resistances apply: $R_{\Theta JL}$ (measured 1/32" from epoxy) = 6° C/W and the lead = 25° C/W per inch when equal heatsinking is applied to each lead.

