80C51FA/83C51FA
EVENT-CONTROL CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER

Automotive

- **Extended Automotive Temperature Range (−40°C to +125°C Ambient)**
- **High Performance CHMOS Process**
- **Three 16-Bit Timer/Counters**
  - **Timer 2 is an Up/Down Timer/Counter**
- **Programmable Counter Array with:**
  - **High Speed Output,**
  - **Compare/Capture,**
  - **Pulse Width Modulator,**
  - **Watchdog Timer Capabilities**
- **8K On-Chip ROM**
- **256 Bytes of On-Chip Data RAM**
- **Boolean Processor**
- **32 Programmable I/O Lines**
- **7 Interrupt Sources**
- **Programmable Serial Channel with:**
  - **Framing Error Detection**
  - **Automatic Address Recognition**
- **TTL and CMOS Compatible Logic Levels**
- **64K External Program Memory Space**
- **64K External Data Memory Space**
- **MCS® 51 Microcontroller Fully Compatible Instruction Set**
- **Power Saving Idle and Power Down Modes**
- **ONCE (On-Circuit Emulation) Mode**
- **Available in PLCC and PDIP Packages**
  (See Packaging Specification, Order #231369)
- **Available in 12 MHz and 16 MHz Versions**

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 8 Kbytes of the program memory can reside in the on-chip ROM. In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 80C51FA/83C51FA is a single-chip control oriented microcontroller which is fabricated on Intel's CHMOS III (83C51FA) ROM technology. For the remainder of this datasheet references to the ROMless (80C51FA) and ROM (83C51FA) versions will be denoted as 83C51FA. Being a member of the MCS® 51 microcontroller family, the 83C51FA uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS 51 microcontroller products. The 83C51FA is an enhanced version of the 87C51. It's added features make it an even more powerful microcontroller for applications that require Pulse Width Modulation, High Speed I/O, and up/down counting capabilities such as brake and traction control. It also has a more versatile serial channel that facilitates multi-processor communications.

NOTICE:

This datasheet contains information on products in full production. Specifications within this datasheet are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

February 1995 **Order Number: 270501-007**

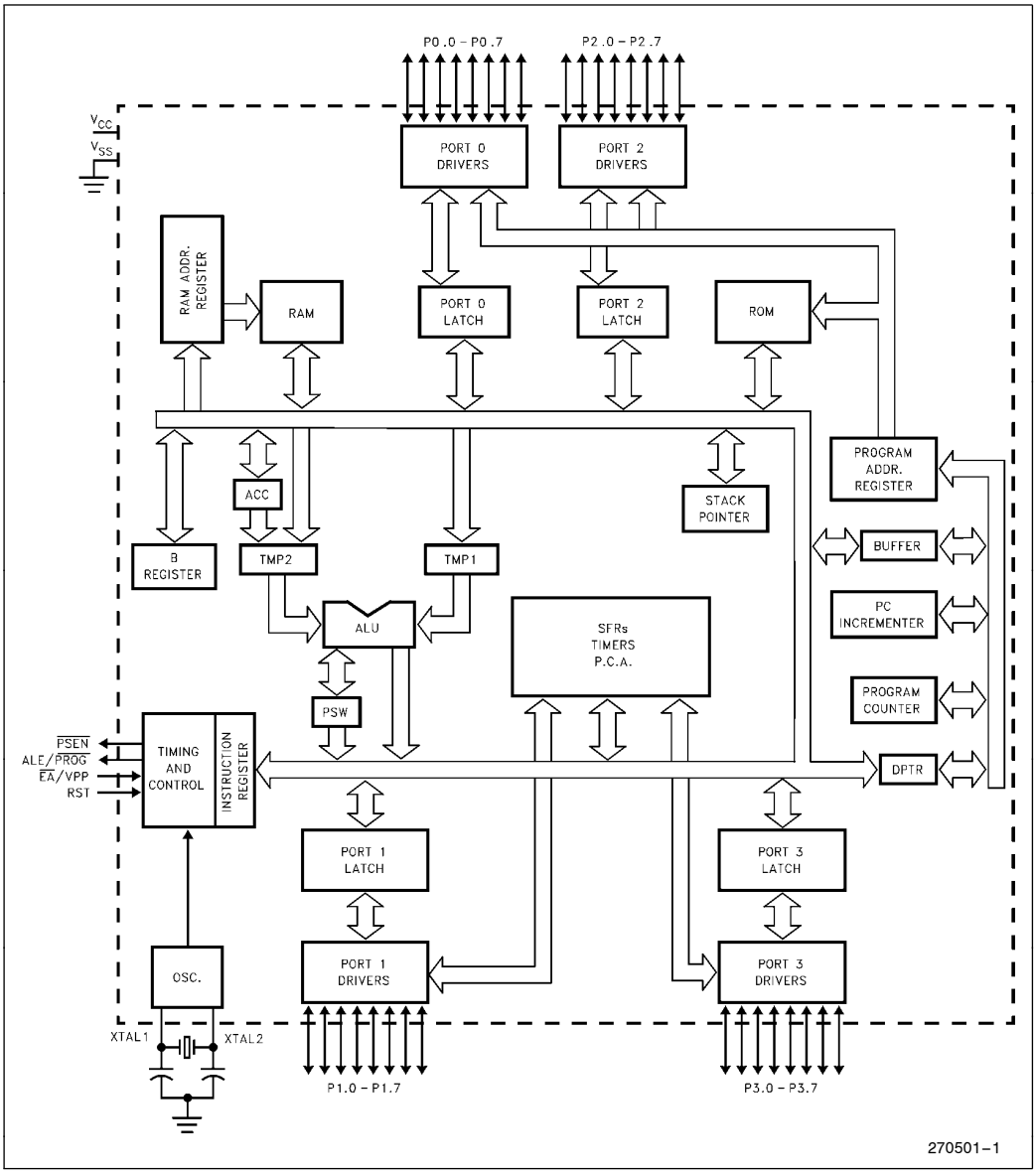


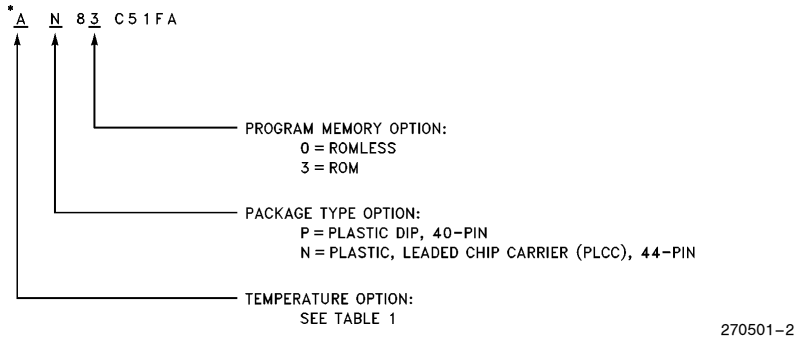
Figure 1. 83C51FA Block Diagram

80C51FA/83C51FA PRODUCT OPTIONS

Intel's extended and automotive temperature range products are designed to meet the needs of those applications whose operating requirements exceed commercial standards.

With the commercial standard temperature range, operational characteristics are guaranteed over the temperature range of 0°C to 70°C ambient. With the extended temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +85°C ambient. For the automotive temperature range option, operational characteristics are guaranteed over the temperature range of −40°C to +125°C ambient.

As shown in Figure 2 temperature, burn-in, and package options are identified by a one- or two-letter prefix to the part number.



***Example:**
AN83C51FA indicates an automotive temperature range version of the 83C51FA in a PLCC package with 8 Kbyte ROM program memory.

Figure 2. MCS® 51 Microcontroller Product Family Nomenclature

Table 1. Temperature Options

Temperature Classification	Temperature Designation	Operating Temperature °C Ambient	Burn-In Options
Extended	T	−40 to +85	Standard
	L	−40 to +85	Extended
Automotive	A	−40 to +125	Standard
	B	−40 to +125	Extended

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting1's, and can source and sink several LS TTL inputs.

Port 0 outputs the code bytes during program verification. External pullup resistors are required during program verification.

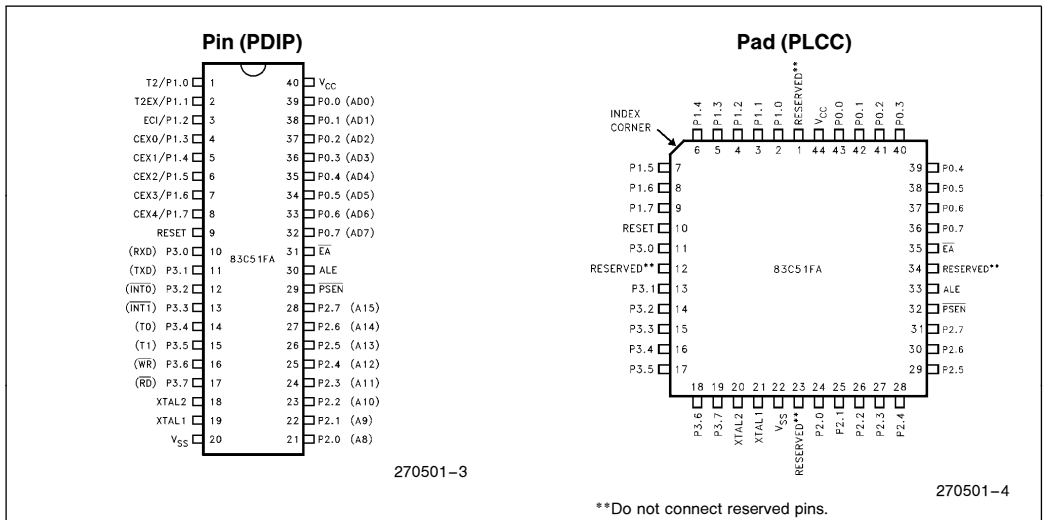
Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the datasheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the 83C51FA:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2)
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)
P1.2	ECI (External Count Input to the PCA)
P1.3	CEX0 (External I/O for Compare/ Capture Module 0)
P1.4	CEX1 (External I/O for Compare/ Capture Module 1)
P1.5	CEX2 (External I/O for Compare/ Capture Module 2)
P1.6	CEX3 (External I/O for Compare/ Capture Module 3)
P1.7	CEX4 (External I/O for Compare/ Capture Module 4)

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the datasheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit



**Do not connect reserved pins.

Diagrams are for pin reference only. Package sizes are not to scale.

Figure 3. Pin Connections

addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the datasheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS 51 microcontroller family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RESET: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE/$\overline{PROG}$: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

Throughout the remainder of this datasheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the 83C51FA is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

XTAL1: Input to the inverting oscillator amplifier.

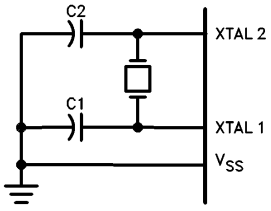
XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 4. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 5. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the datasheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.



C1, C2 = 30 pF ±10 pF for Crystals
For Ceramic Resonators, contact resonator manufacturer.

Figure 4. Oscillator Connections

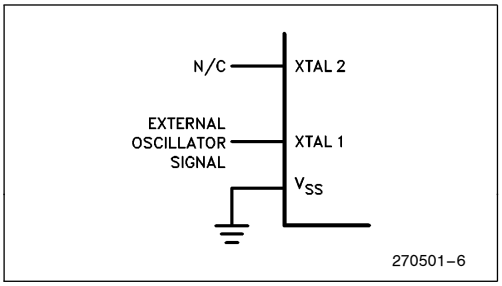


Figure 5. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode.

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values if the Power Down mode is terminated with an interrupt.

On the 83C51FA either a hardware reset or external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

DESIGN CONSIDERATION

When the Idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE (''On-Circuit Emulation'') Mode facilitates testing and debugging of systems using the 83C51FA without the 83C51FA having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins float, the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 83C51FA is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 2. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Applications Handbook, and Application Note AP-252, ''Designing with the 80C51BH.''

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature
Under Bias ..... −40°C to +125°C

Storage Temperature ..... −65°C to +150°C

Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V

I_{OL} I/O Pin ..... 15 mA

Power Dissipation 1.5W
(Based on PACKAGE heat transfer limitations, not device power consumption)

Typical Junction Temperature (T_J) ..... +135°C
(Based upon Ambient Temperature at +125°C)

Typical Thermal Resistance
Junction-to-Ambient (θ_{JA})
PDIP ..... 45°C/W
PLCC ..... 46°C/W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

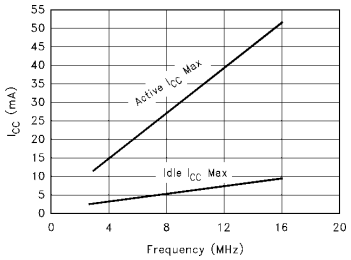
DC CHARACTERISTICS: (T_A = −40°C to +125°C; V_{CC} = 5V ±10%; V_{SS} = 0V)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL2, RST, $\overline{EA}$)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2 and 3)			0.45	V	I_{OL} = 1.6 mA(1)
V_{OL1}	Output Low Voltage (Port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$)			0.45	V	I_{OL} = 20 I_{OL} = 3.2 mA(1) I_{OL} = 7.0 mA
V_{OH}	Output High Voltage (Ports 1, 2 and 3 ALE/$\overline{PROG}$ and $\overline{PSEN}$)	2.4			V	I_{OH} = −60 μA
		0.9 V_{CC}			V	I_{OH} = −10 μA(2)
V_{OH1}	Output High Voltage	2.4			V	I_{OH} = −800 μA
	(Port 0 in External Bus Mode)	0.9 V_{CC}			V	I_{OH} = −80 μA(2)
I_{IL}	Logical 0 Input Current (Ports 1, 2 and 3)		−10	−50	μA	V_{IN} = 0.45V
I_{LI}	Input leakage Current (Port 0)		0.02	±10	μA	V_{IN} = V_{IL} or V_{IH}

DC CHARACTERISTICS: ($T_A = -40°C$ to $+125°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$) (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, and 3)		−265	−650	μA	$V_{IN} = 2V$
RRST	RST Pulldown Resistor	40	100	225	KΩ	
CIO	Pin Capacitance		10		pF	@1MHz, 25°C
I_{CC}	Power Supply Current: Running at 12 MHz (Figure 5) Idle Mode at 12 MHz (Figure 5) Power Down Mode (I_{PD})			 40 15 150	 mA mA μA	(Note 3)

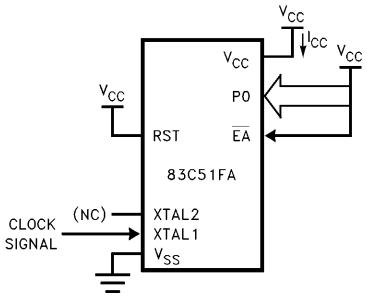
NOTES:
1. Capacitive loading on Ports 0 and 2 may cause noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operations. In applications where capacitance loading exceeds 100 pFs, the noise pulse on the ALE signal may exceed 0.8V. In these cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an Address Latch with a Schmitt Trigger Strobe input.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.
3. See Figures 6–9 for test conditions. Minimum V_{CC} for Power Down is 2.0V.
4. Typicals are based on limited number of samples, and are not guaranteed. The values listed are at room temperature and 5.0V.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per Port Pin: 10 mA
   Maximum I_{OL} per 8-Bit Port -
   Port 0: 26 mA
   Ports 1, 2, and 3: 15 mA
   Maximum Total I_{OL} for all Output Pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
6. Contact Intel for design-in information.



270501–7

I_{CC} Max at other frequencies is given by:
Active Mode
I_{CC} Max = (3 × Osc Freq) + 4
Idle Mode
I_{CC} Max = (0.49 × Osc Freq) + 1.6
Where Osc Freq is in MHz, I_{CC} is in mA.

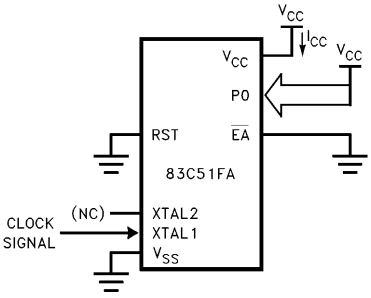
Figure 6. I_{CC} vs Frequency



270501–8

TCLCH = TCHCL = 5 ns

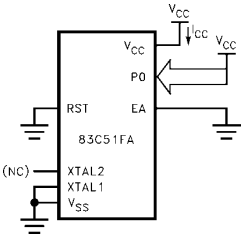
Figure 7. I_{CC} Test Condition, Active Mode
All other pins disconnected.



270501–9

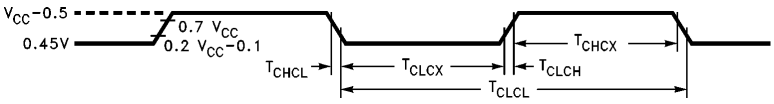
TCLCH = TCHCL = 5 ns

Figure 8. I_{CC} Test Condition Idle Mode.
All other pins disconnected.



270501–10

Figure 9. I_{CC} Test Condition,
Power Down Mode.
All other pins disconnected.
V_{CC} = 2.0V to 5.5V.



270501–11

Figure 10. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

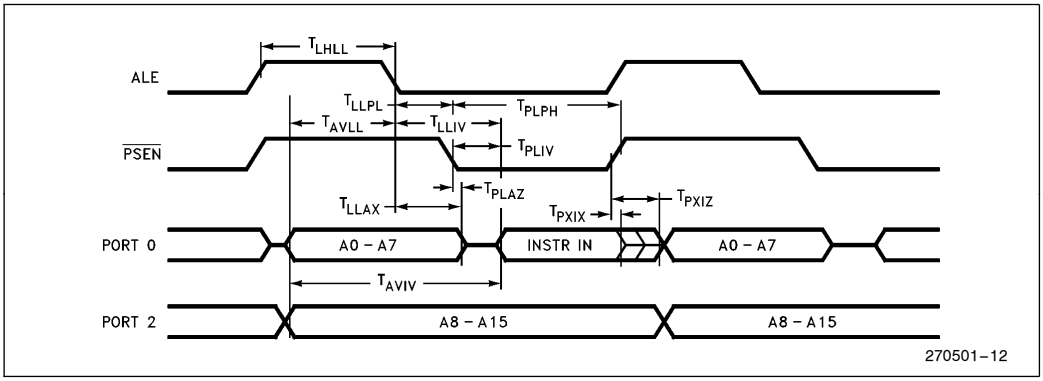
T_{AVLL} = Time from Address Valid to ALE Low
T_{LLPL} = Time from ALE Low to PSEN Low

AC CHARACTERISTICS ($T_A = -40°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$ and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

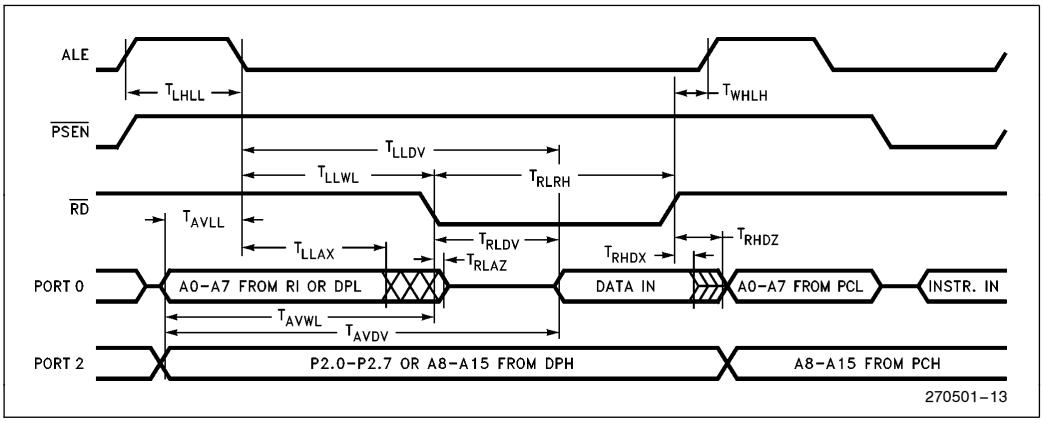
EXTERNAL MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/T_{CLCL}$	Oscillator Frequency			3.5	16	MHz
T_{LHLL}	ALE Pulse Width	127		$2T_{CLCL}-40$		ns
T_{AVLL}	Address Valid to ALE Low	43		$T_{CLCL}-40$		ns
T_{LLAX}	Address Hold After ALE Low	53		$T_{CLCL}-30$		ns
T_{LLIV}	ALE Low to Valid Instruction In		224		$4T_{CLCL}-110$	ns
T_{LLPL}	ALE Low to $\overline{\text{PSEN}}$ Low	53		$T_{CLCL}-30$		ns
T_{PLPH}	$\overline{\text{PSEN}}$ Pulse Width	205		$3T_{CLCL}-45$		ns
T_{PLIV}	$\overline{\text{PSEN}}$ Low to Valid Instruction In		135		$3T_{CLCL}-115$	ns
T_{PXIX}	Input Instr Hold After $\overline{\text{PSEN}}$ Trans	0		0		ns
T_{PXIZ}	Input Instr Float After $\overline{\text{PSEN}}$ Trans		59		$T_{CLCL}-25$	ns
T_{AVIV}	Address to Valid Instruction In		302		$5T_{CLCL}-115$	ns
T_{PLAZ}	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
T_{RLRH}	$\overline{\text{RD}}$ Pulse Width	400		$6T_{CLCL}-100$		ns
T_{WLWH}	$\overline{\text{WR}}$ Pulse Width	400		$6T_{CLCL}-100$		ns
T_{RLDV}	$\overline{\text{RD}}$ Low to Valid Data In		242		$5T_{CLCL}-175$	ns
T_{RHDX}	Data Hold After $\overline{\text{RD}}$ High	−10		−10		ns
T_{RHDZ}	Data Float After $\overline{\text{RD}}$ High		107		$2T_{CLCL}-60$	ns
T_{LLDV}	ALE Low to Valid Data In		507		$8T_{CLCL}-160$	ns
T_{AVDV}	Address Valid to Valid Data In		575		$9T_{CLCL}-175$	ns
T_{LLWL}	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	$3T_{CLCL}-50$	$3T_{CLCL}+50$	ns
T_{AVWL}	Data Valid to $\overline{\text{WR}}$ Low	203		$4T_{CLCL}-130$		ns
T_{QVWX}	Address Valid before $\overline{\text{WR}}$ Low	23		$T_{CLCL}-50$		ns
T_{WHQX}	Data Hold after $\overline{\text{WR}}$ High	33		$T_{CLCL}-50$		ns
T_{QVWH}	Data Valid to $\overline{\text{WE}}$ High	433		$7T_{CLCL}-150$		ns
T_{RLAZ}	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
T_{WHLH}	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	$T_{CLCL}-40$	$T_{CLCL}+40$	ns

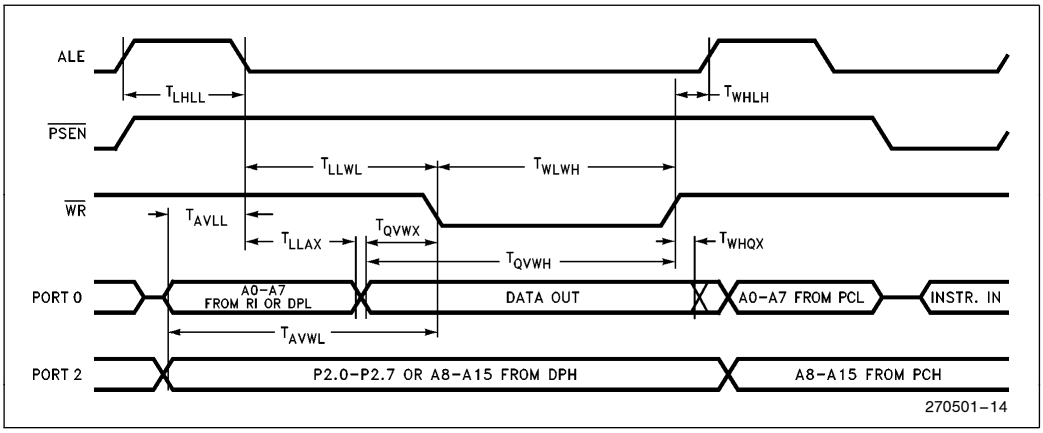
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

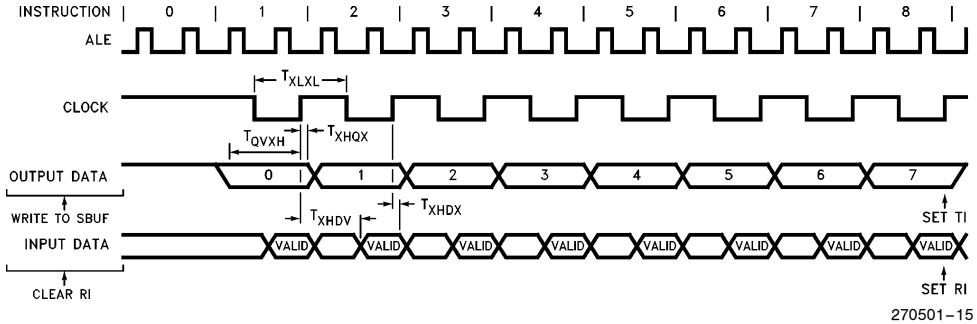


SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: $T_A = -40°C$ to $+125°C$; $V_{CC} = 5V \pm 10\%$; $V_{SS} = 0V$; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
T_{XLXL}	Serial Port Clock Cycle Time	1		$12T_{CLCL}$		μs
T_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10T_{CLCL} - 133$		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	50		$2T_{CLCL} - 117$		ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10T_{CLCL} - 133$	ns

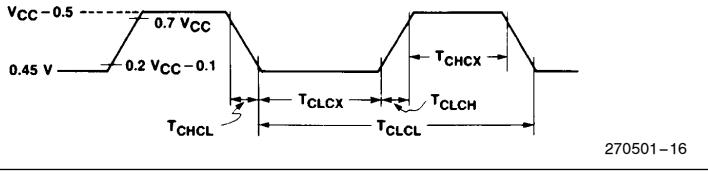
SHIFT REGISTER MODE TIMING WAVEFORMS



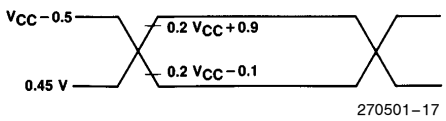
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
$1/T_{CLCL}$	Oscillator Frequency	3.5	16	MHz
T_{CHCX}	High Time	20		ns
T_{CLCX}	Low Time	20		ns
T_{CLCH}	Rise Time		20	ns
T_{CHCL}	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



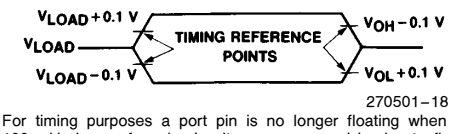
AC TESTING INPUT, OUTPUT WAVEFORMS



270501–17

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{OL} max for a Logic "0".

FLOAT WAVEFORMS



270501–18

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA. This is for Ports 1, 2 and 3.

DATASHEET REVISION HISTORY

The following are key differences between this datasheet and the -006 version:

1. The "preliminary" status was dropped and replaced with production status (no label).
2. Trademarks were updated.

The following are key differences between the -006 and the -005 version of the datasheet:

1. Preliminary notice has been added to the Title page.
2. Figure 3 Pin Connections has been modified, RST pin is now RESET pin.
3. RST pin description is now RESET pin description.
4. Figure 6 I_{CC} vs. Frequency has been corrected to show test conditions.
5. I_{CC} Max spec has been corrected.
6. A.C. Characteristic table $1/T_{CLCL}$ spec has been changed to have a Max frequency of 16 MHz.

The following are key differences between the -005 and the -004 version of the datasheet:

1. "NC" pin labels changed to "Reserved" in Figure 3.
2. Capacitor value for ceramic resonators deleted in Figure 4.

The following are the key differences between the -003 version of the 8XC51FA datasheet and the -004 version of the 80C51FA/83C51FA datasheet:

1. Removed references to EPROM from the 8XC51FA datasheet.
2. Revised Figure 4, "Oscillator Connections".

The following are the key differences between the -002 and the -003 version of this datasheet:

1. Dropped word "maximum" from I_{OL} in the Absolute Maximum Rating table.
2. Dropped $\overline{EA}$ from I_{LI} specification of the DC table.
3. Corrected TQVWH specification (from TTCLCL − 70 to TCLCL − 150).
4. Added note on external clock capacitance loading.
5. Changed the title to 80C51FA/83C51FA Event-Control CHMOS Single-Chip 8-Bit Microcontroller.
6. Added pin count to Figure 1.
7. Changed I_{LI} to $\pm 10\ \mu A$.
8. Added I_{CC} Power Down Mode 150 nA.