



# AU6320

**USB2.0 CF Card Reader Controller**

**Technical Reference Manual**



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# **1. Introduction**

## **1.1 Description**

The AU6320 is a single chip integrated USB 2.0 multimedia card reader controller that enables PC/DVD/Printer to read/write CF (Compact Flash) widely used in digital camera, cell phone, PDA and MP3 player to store digital photos and compressed music. Performance of AU6320 is maximized by implementing the latest and fastest card specification available from the industry.

The AU6320 is designed in shared pin architecture to meet cost and space regulate for Notebook end reunite.

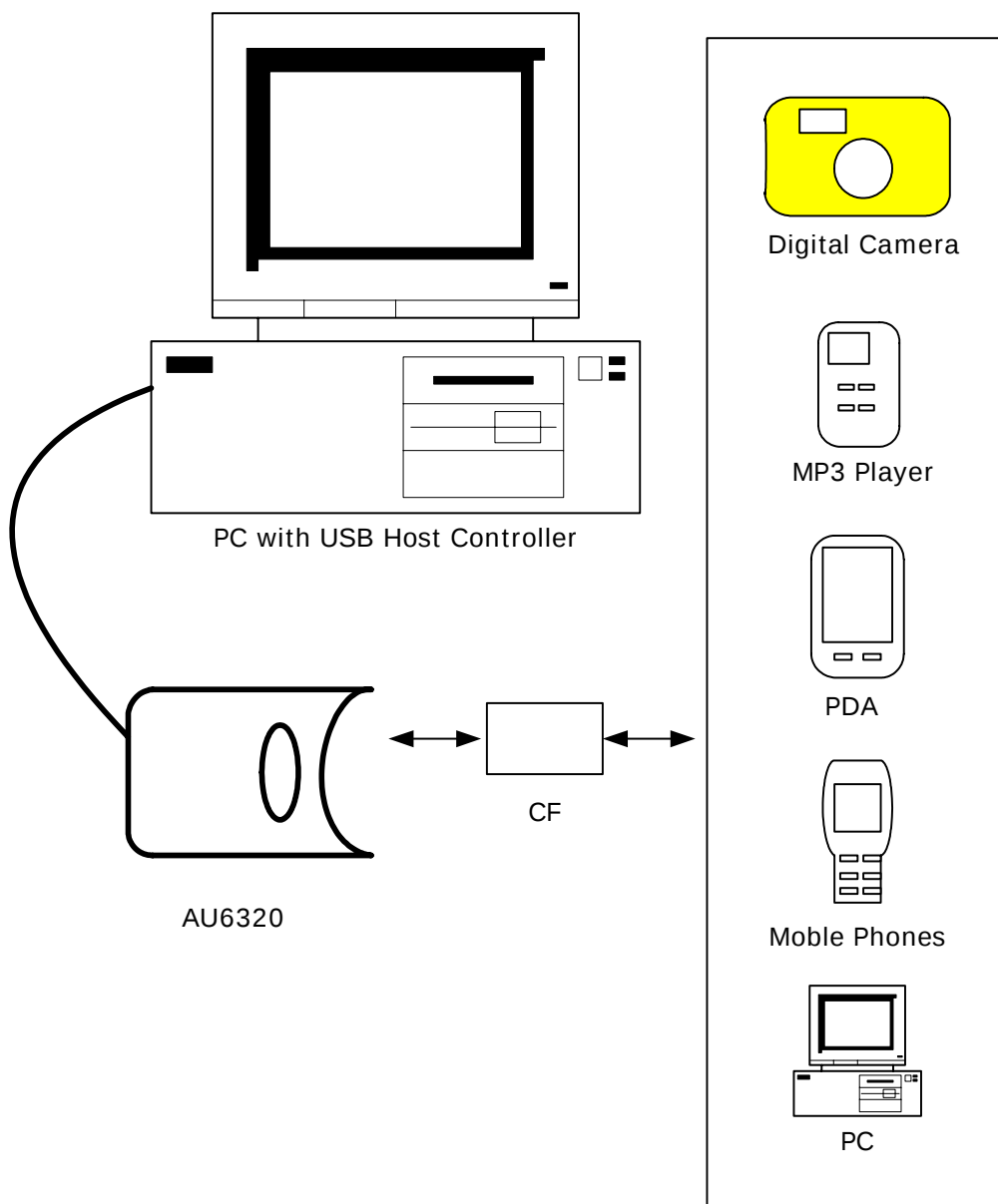
## **1.2 Features**

- Support USB V2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport V1.0
- Support CF compatible flash card, including Micro Drive (CF type II).
- Support CF 4.0 Ultra DMA mode.
- Hardware DMA engine integrated for performance enhancement.
- Work with default driver from Windows ME/2000/XP/Vista and Mac OS X; Windows 98/2000(SP1/SP2) and Mac OS 9 are supported by vendor driver from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer optimize performance
- Support slot-to-slot read/write operation
- Support Dynamic Icon Utility
- Support LED for bus operating indication
- Power switch integrated to reduce production BOM cost
- 30MHz 8051 CPU
- Built in 3.3V to 1.8V regulator
- Runs at 12MHz crystal
- Available in 48-pin LQFP package

## 2. Application Block Diagram

Following application diagram demonstrates a typical card reader using the AU6320 chip. By connecting the card reader to a desktop or notebook PC through USB bus, the AU6320 becomes a bus-powered, high speed USB card reader, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

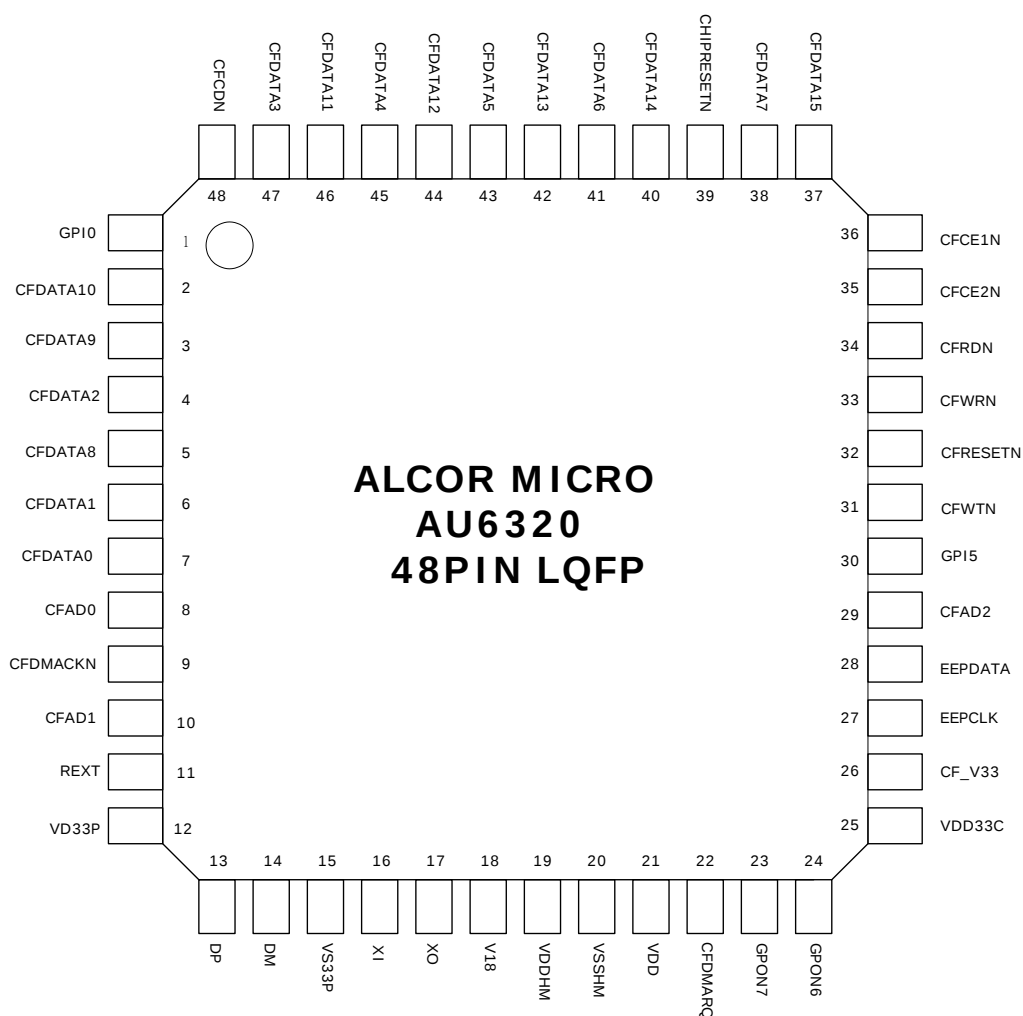
Figure 2.1 Block Diagram



## 3. Pin Assignment

AU6320 is available in 48-pin LQFP package. Below diagram shows signal name of each pin and table in the following page describes each pin in detail.

**Figure 3.1 AU6320 Pin Assignment Diagram**



**Table 3.1 AU6320 Pin Descriptions**

| Pin # | Pin Name | I/O | Description                                                                                |
|-------|----------|-----|--------------------------------------------------------------------------------------------|
| 1     | GPI0     | I   | Slot Mode Select. '0' for 4 LUN [Default]. '1' for 1 LUN.                                  |
| 2     | CFDATA10 | IO  | CF Data10                                                                                  |
| 3     | CFDATA9  | IO  | CF Data9                                                                                   |
| 4     | CFDATA2  | IO  | CF Data2                                                                                   |
| 5     | CFDATA8  | IO  | CF Data8                                                                                   |
| 6     | CFDATA1  | IO  | CF Data1                                                                                   |
| 7     | CFDATA0  | IO  | CF Data0                                                                                   |
| 8     | CFAD0    | O   | CF Address0                                                                                |
| 9     | CFDMACKN | O   |                                                                                            |
| 10    | CFAD1    | O   | CF Address1                                                                                |
| 11    | REXT     | IO  | External Resistor 330 to Ground                                                            |
| 12    | VD33P    | PWR | 3.3V Power Source for UTMI                                                                 |
| 13    | DP       | IO  | DP                                                                                         |
| 14    | DM       | IO  | DM                                                                                         |
| 15    | VS33P    | GND | Ground Power                                                                               |
| 16    | XI       | I   | 12MHz Crystal Input                                                                        |
| 17    | XO       | O   | 12MHz Crystal Output                                                                       |
| 18    | V18      | PWR | Core Power 1.8V                                                                            |
| 19    | VDDHM    | PWR | 3.3V Power Source for IO pad                                                               |
| 20    | VSSHM    | GND | 3.3V ground for IO pad                                                                     |
| 21    | VDD      | PWR | Core Power 1.8V Input                                                                      |
| 22    | CFDMARQ  | I   |                                                                                            |
| 23    | GPON7    | O   | Card access LED.                                                                           |
| 24    | GPON6    | O   | CF power indicator. '0' for on. '1' for off. Reserved for external PMOS for CF card power. |
| 25    | VDD33C   | PWR | 3.3V power for PMOS                                                                        |
| 26    | CF_V33   | PWR | CF Power                                                                                   |
| 27    | EEPCLK   | O   | EEPCLK                                                                                     |
| 28    | EEPDATA  | IO  | EEPDATA                                                                                    |
| 29    | CFAD2    | O   | CF Address2                                                                                |
| 30    | GPI5     | I   | Device current consumption value. "1":250mA for WHQL; "0":100mA for normal mode            |
| 31    | CFWTN    | I   | CF WTN                                                                                     |

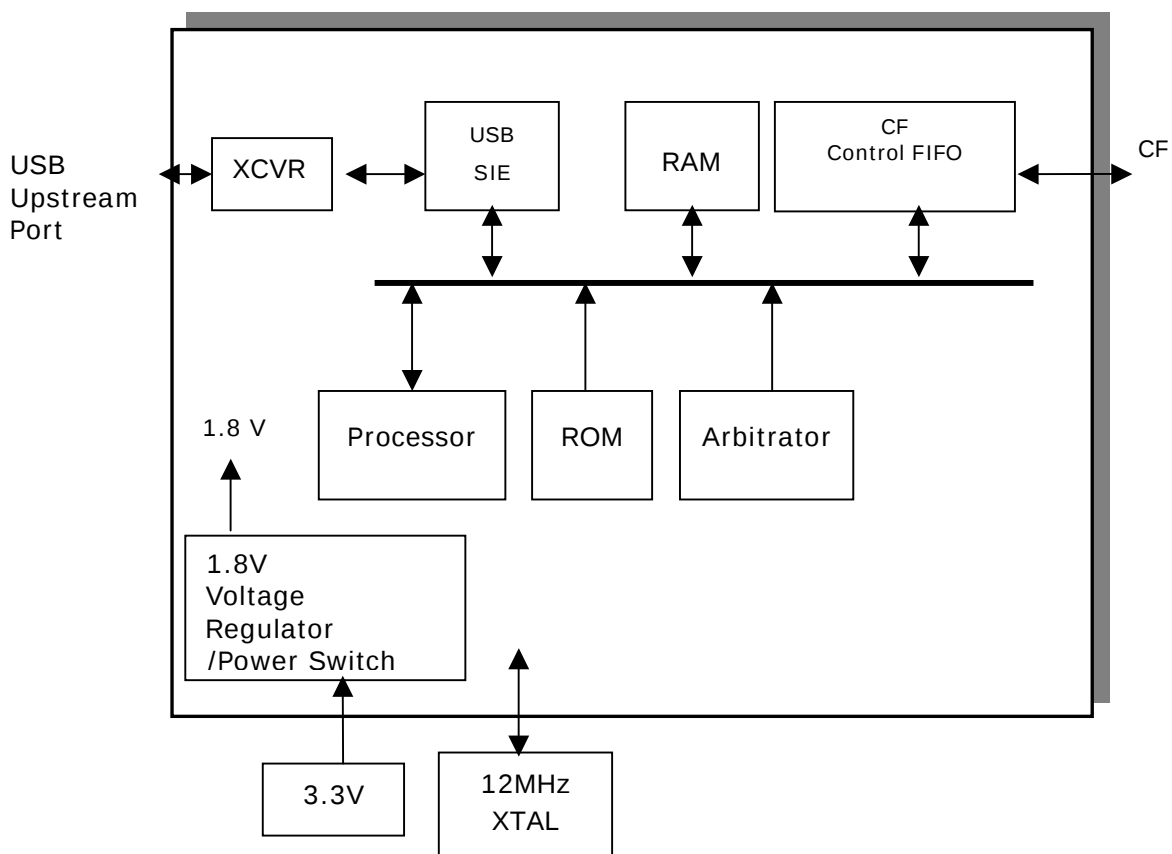


| Pin # | Pin Name   | I/O | Description                                   |
|-------|------------|-----|-----------------------------------------------|
| 32    | CFRESETN   | O   | CF Reset                                      |
| 33    | CFWRN      | O   | CF WRN                                        |
| 34    | CFRDN      | O   | CF RDN                                        |
| 35    | CFCE2N     | O   | CFCE2N                                        |
| 36    | CFCE1N     | O   | CFCE1N                                        |
| 37    | CFDATA15   | IO  | CF Data15                                     |
| 38    | CFDATA7    | IO  | CF Data7                                      |
| 39    | CHIPRESETN | I   | Chip Reset                                    |
| 40    | CFDATA14   | IO  | CF Data14                                     |
| 41    | CFDATA6    | IO  | CF Data6                                      |
| 42    | CFDATA13   | IO  | CF Data13                                     |
| 43    | CFDATA5    | IO  | CF Data5                                      |
| 44    | CFDATA12   | IO  | CF Data12                                     |
| 45    | CFDATA4    | IO  | CF Data4                                      |
| 46    | CFDATA11   | IO  | CF Data11                                     |
| 47    | CFDATA3    | IO  | CF Data3                                      |
| 48    | CFCDN      | I   | CF Card Detect ("0":Detected; "1":Undetected) |

## 4. System Architecture and Reference Design

### 4.1 AU6320 Block Diagram

Figure 4.1 AU6320 Block Diagram





## 5. Electrical Characteristics

### 5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

| SYMBOL           | PARAMETER            | RATING                        | UNITS |
|------------------|----------------------|-------------------------------|-------|
| V <sub>DDH</sub> | Power Supply         | -0.3 to 3.6                   | V     |
| V <sub>IN</sub>  | Input Signal Voltage | -0.3 to V <sub>DDH</sub> +0.3 | V     |
| T <sub>STG</sub> | Storage Temperature  | -40 to 150                    | °C    |

### 5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

| SYMBOL                             | PARAMETER             | MIN  | TYP | MAX  | UNITS |
|------------------------------------|-----------------------|------|-----|------|-------|
| V <sub>DDH</sub>                   | Power Supply          | 3.0  | 3.3 | 3.6  | V     |
| V <sub>DD</sub><br>V <sub>18</sub> | Digital Supply        | 1.62 | 1.8 | 1.98 | V     |
| V <sub>IN</sub>                    | Input Signal Voltage  | 0    | 3.3 | 3.6  | V     |
| T <sub>OPR</sub>                   | Operating Temperature | 0    |     | 85   | °C    |

### 5.3 General DC Characteristics

Table 5.3 General DC Characteristics

| SYMBOL           | PARAMETER                         | CONDITIONS              | MIN | TYP | MAX | UNITS |
|------------------|-----------------------------------|-------------------------|-----|-----|-----|-------|
| I <sub>IN</sub>  | Input current                     | No pull-up or pull-down | -10 | ±1  | 10  | μA    |
| I <sub>OZ</sub>  | Tri-state leakage current         |                         | -10 | ±1  | 10  | μA    |
| C <sub>IN</sub>  | Input capacitance                 | Pad Limit               |     | 2.8 |     | pF    |
| C <sub>OUT</sub> | Output capacitance                | Pad Limit               |     | 2.8 |     | pF    |
| C <sub>BID</sub> | Bi-directional buffer capacitance | Pad Limit               |     | 2.8 |     | pF    |

## 5.4 DC Electrical Characteristics of 3.3V I/O Cells

**Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells**

| SYMBOL    | PARAMETER                        | CONDITIONS                      | Limits |         |     | UNIT          |
|-----------|----------------------------------|---------------------------------|--------|---------|-----|---------------|
|           |                                  |                                 | MIN    | TYP     | MAX |               |
| $V_{DDH}$ | Power supply                     | 3.3V I/O                        | 3.0    | 3.3     | 3.6 | V             |
| $V_{il}$  | Input low voltage                | LVTTL                           |        |         | 0.8 | V             |
| $V_{ih}$  | Input high voltage               |                                 | 2.0    |         |     | V             |
| $V_{ol}$  | Output low voltage               | $ I_{ol}  = 2 \sim 16\text{mA}$ |        |         | 0.4 | V             |
| $V_{oh}$  | Output high voltage              | $ I_{oh}  = 2 \sim 16\text{mA}$ | 2.4    |         |     | V             |
| $R_{pu}$  | Input pull-up resistance         | PU=high, PD=low                 | 55     | 75      | 110 | K $\Omega$    |
| $R_{pd}$  | Input pull-down resistance       | PU=low, PD=high                 | 40     | 75      | 150 | K $\Omega$    |
| $I_{in}$  | Input leakage current            | $V_{in} = V_{DDH}$ or 0         | -10    | $\pm 1$ | 10  | $\mu\text{A}$ |
| $I_{oz}$  | Tri-state output leakage current |                                 | -10    | $\pm 1$ | 10  | $\mu\text{A}$ |

## 5.5 USB Transceiver Characteristics

**Table 5.5 Electrical characteristics**

| Symbol     | Parameter                | Conditions                         | Min. | Typ. | Max. | Unit |
|------------|--------------------------|------------------------------------|------|------|------|------|
| VD33P      | Analog supply Voltage    |                                    | 3.0  | 3.3  | 3.6  | V    |
| VDD<br>V18 | Digital supply Voltage   |                                    | 1.62 | 1.8  | 1.98 | V    |
| $I_{CC}$   | Operating supply current | High speed operating<br>at 480 MHz |      |      | 55   | mA   |

**Table 5.6 Static characteristic : Digital pin**

| Symbol        | Parameter                 | Conditions | Min.     | Typ. | Max. | Unit |
|---------------|---------------------------|------------|----------|------|------|------|
| Input levels  |                           |            |          |      |      |      |
| $V_{IL}$      | Low-level input voltage   |            |          |      | 0.8  | V    |
| $V_{IH}$      | High-level input voltage  |            | 2.0      |      |      | V    |
| Output levels |                           |            |          |      |      |      |
| $V_{OL}$      | Low-level output voltage  |            |          |      | 0.2  | V    |
| $V_{OH}$      | High-level output voltage |            | VDDH-0.2 |      |      | V    |

**Table 5.7 Static characteristic : Analog I/O pins (DP/DM)**

| Symbol                                 | Parameter                                           | Conditions                                                                   | Min. | Typ. | Max. | Unit     |
|----------------------------------------|-----------------------------------------------------|------------------------------------------------------------------------------|------|------|------|----------|
| USB2.0 Transceiver ( HS )              |                                                     |                                                                              |      |      |      |          |
| Input Levels ( differential receiver ) |                                                     |                                                                              |      |      |      |          |
| $V_{HSDIFF}$                           | High speed differential input sensitivity           | $ V_{I(DP)}-V_{I(DM)} $<br>measured at the connection as application circuit | 300  |      |      | mV       |
| $V_{HSCM}$                             | High speed data signaling common mode voltage range |                                                                              | -50  |      | 500  | mV       |
| $V_{HSSQ}$                             | High speed squelch detection threshold              | Squelch detected                                                             |      |      | 100  | mV       |
|                                        |                                                     | No squelch detected                                                          | 150  |      |      | mV       |
| $V_{HSDSC}$                            | High speed disconnection detection threshold        | Disconnection detected                                                       | 625  |      |      | mV       |
|                                        |                                                     | Disconnection not detected                                                   |      |      | 525  | mV       |
| Output Levels                          |                                                     |                                                                              |      |      |      |          |
| $V_{HSOI}$                             | High speed idle level output voltage(differential)  |                                                                              | -10  |      | 10   | mV       |
| $V_{HSOL}$                             | High speed low level output voltage(differential)   |                                                                              | -10  |      | 10   | mV       |
| $V_{HSOH}$                             | High speed high level output voltage(differential)  |                                                                              | -360 |      | 400  | mV       |
| $V_{CHIRPJ}$                           | Chirp-J output voltage ( differential )             |                                                                              | 700  |      | 1100 | mV       |
| $V_{CHIRPK}$                           | Chirp-K output voltage ( differential )             |                                                                              | -900 |      | -500 | mV       |
| Resistance                             |                                                     |                                                                              |      |      |      |          |
| $R_{DRV}$                              | Driver output impedance                             | Equivalent resistance used as internal chip only                             | 3    | 6    | 9    | $\Omega$ |

|                                       |                                                     |                                                |      |    |      |   |
|---------------------------------------|-----------------------------------------------------|------------------------------------------------|------|----|------|---|
|                                       |                                                     | Overall resistance including external resistor | 40.5 | 45 | 49.5 |   |
| Termination                           |                                                     |                                                |      |    |      |   |
| $V_{TERM}$                            | Termination voltage for pull-up resistor on pin RPU |                                                | 3.0  |    | 3.6  | V |
| USB1.1 Transceiver (FS)               |                                                     |                                                |      |    |      |   |
| Input Levels (differential receiver)  |                                                     |                                                |      |    |      |   |
| $V_{DI}$                              | Differential input sensitivity                      | $ V_{I(DP)} - V_{I(DM)} $                      | 0.2  |    |      | V |
| $V_{CM}$                              | Differential common mode voltage                    |                                                | 0.8  |    | 2.5  | V |
| Input Levels (single-ended receivers) |                                                     |                                                |      |    |      |   |
| $V_{SE}$                              | Single ended receiver threshold                     |                                                | 0.8  |    | 2.0  | V |
| Output levels                         |                                                     |                                                |      |    |      |   |
| $V_{OL}$                              | Low-level output voltage                            |                                                | 0    |    | 0.3  | V |
| $V_{OH}$                              | High-level output voltage                           |                                                | 2.8  |    | 3.6  | V |

**Table 5.8 Dynamic characteristic : Analog I/O pins (DP/DM)**

| Symbol                 | Parameter                                                  | Conditions                                    | Min. | Typ. | Max. | Unit |
|------------------------|------------------------------------------------------------|-----------------------------------------------|------|------|------|------|
| Driver Characteristics |                                                            |                                               |      |      |      |      |
| High-Speed Mode        |                                                            |                                               |      |      |      |      |
| $t_{HSR}$              | High-speed differential rise time                          |                                               | 500  |      |      | ps   |
| $t_{HSF}$              | High-speed differential fall time                          |                                               | 500  |      |      | ps   |
| Full-Speed Mode        |                                                            |                                               |      |      |      |      |
| $t_{FR}$               | Rise time                                                  | CL=50pF ; 10 to 90% of $ V_{OH} - V_{OL} $ ;  | 4    |      | 20   | ns   |
| $t_{FF}$               | Fall time                                                  | CL=50pF ; 90 to 10% of $ V_{OH} - V_{OL} $ ;  | 4    |      | 20   | ns   |
| $t_{FRMA}$             | Differential rise/fall time matching ( $t_{FR} / t_{FF}$ ) | Excluding the first transition from idle mode | 90   |      | 110  | %    |
| $V_{CRS}$              | Output signal crossover voltage                            | Excluding the first transition from idle mode | 1.3  |      | 2.0  | V    |

## 5.6 Power Switch Feature

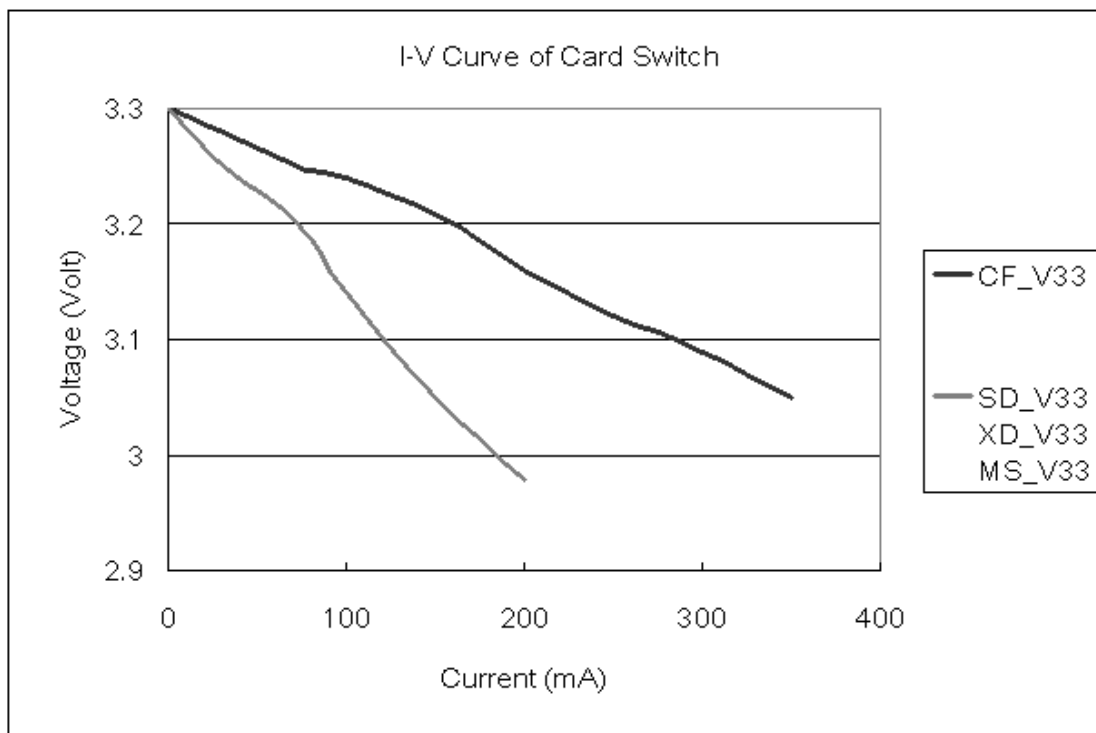


Figure 5.1 Built-in card power switch I-V curve

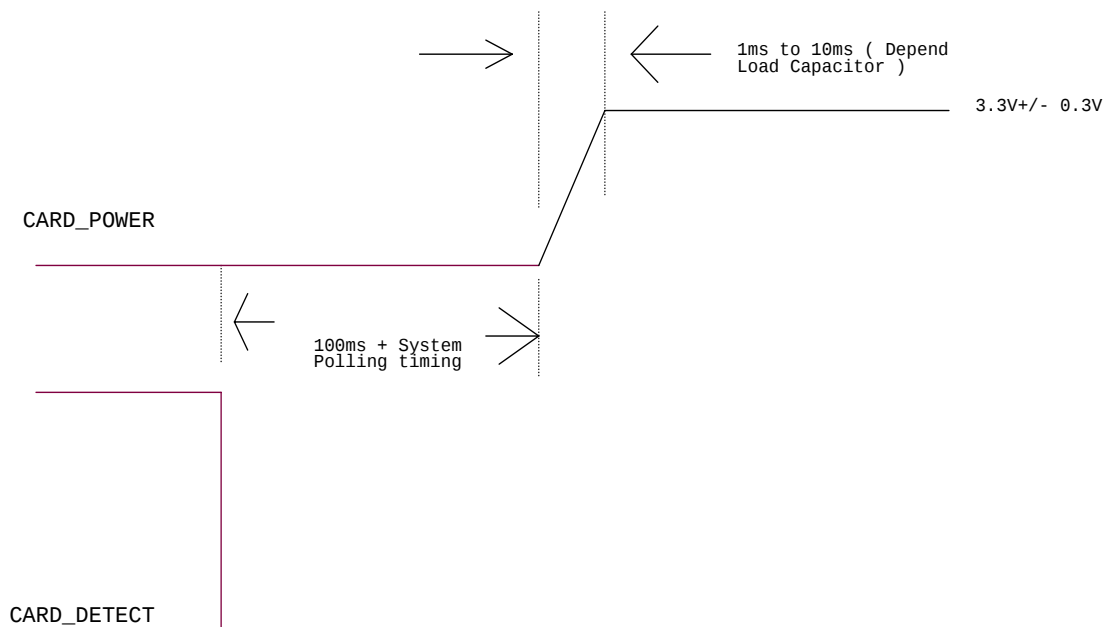
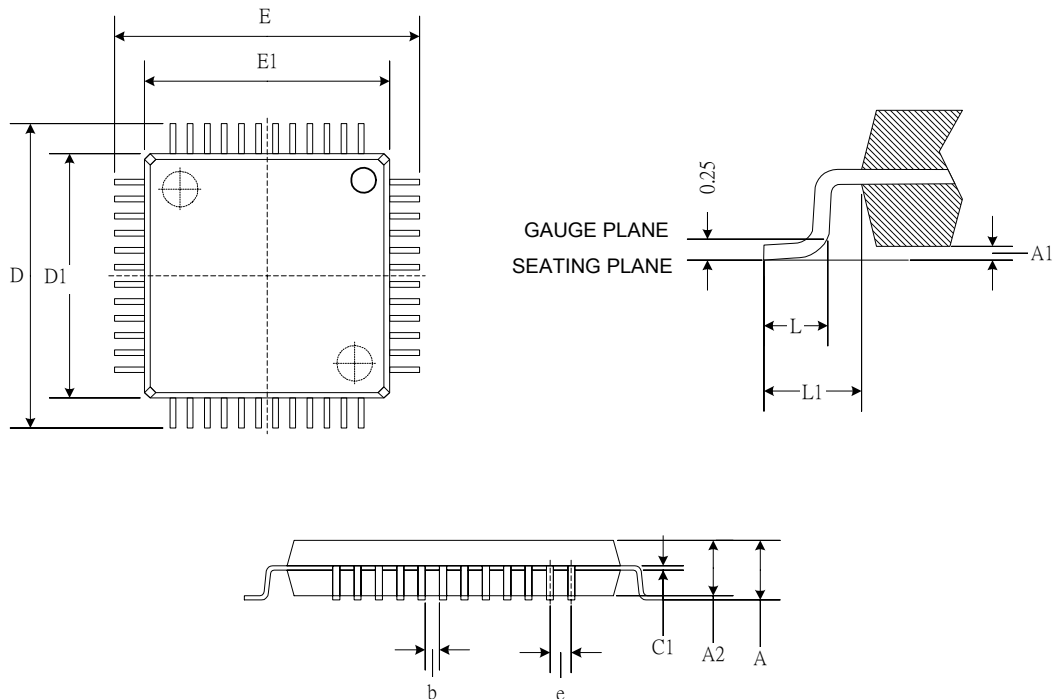


Figure 5.2 Card Detect Power-in Timing

## 6. Mechanical Information

Figure 6.1 Mechanical Information Diagram



| SYMBOLS | MIN.     | MAX. |
|---------|----------|------|
| A       | --       | 1.6  |
| A1      | 0.05     | 0.15 |
| A2      | 1.35     | 1.45 |
| c1      | 0.09     | 0.16 |
| D       | 9.00 BSC |      |
| D1      | 7.00 BSC |      |
| E       | 9.00 BSC |      |
| E1      | 7.00 BSC |      |
| e       | 0.5 BSC  |      |
| b       | 0.17     | 0.27 |
| L       | 0.45     | 0.75 |
| L1      | 1 REF    |      |

1. JEDEC OUTLINE: MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm



## 7. Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

|             |                                     |
|-------------|-------------------------------------|
| <b>SIE</b>  | Serial Interface Engine             |
| <b>CF</b>   | Compact Flash                       |
| <b>UTMI</b> | USB Transceiver Macrocell Interface |

## About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader...etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.