AX88772A/AX88172A
Low-pin-count
USB 2.0 to 10/100M Fast Ethernet Controller

Features

Document No: AX88x72A/V1.1/12/24/07

- Single chip USB 2.0 to 10/100M Fast Ethernet controller – AX88772A
- Single chip USB 2.0 to MII, single chip MII to Ethernet and USB Bridging controller in Dual-PHY mode (submitted for US patent application) – AX88172A

- **USB Device Interface**
  - Integrates on-chip USB 2.0 transceiver and SIE compliant to USB Spec 1.1 and 2.0
  - Supports USB Full and High Speed modes with Bus-Power or Self-Power capability
  - Supports 4 or 6 programmable endpoints on USB interface
  - High performance packet transfer rate over USB bus using proprietary burst transfer mechanism (submitted for US patent application)
  - Supports USB to Ethernet bridging or vice versa in hardware

- **Fast Ethernet Controller**
  - Integrates 10/100Mbps Fast Ethernet MAC/PHY
  - IEEE 802.3 10BASE-T/100BASE-TX compatible
  - Supports twisted pair crossover detection and auto-correction (HP Auto-MDIX)
  - Embedded 16KB SRAM for RX packet buffering and 8KB SRAM for TX packet buffering
  - Supports both Full-duplex with flow control and Half-duplex with backpressure operation
  - Supports 2 VLAN ID filtering, received VLAN Tag (4 bytes) can be stripped off or preserved
  - MAC/PHY loop-back diagnostic capability

- **Support Wake-on-LAN Function**
  - Supports Suspend Mode and Remote Wakeup via Link-up, Magic packet, MS wakeup frame and external pin
  - Optional PHY power down during Suspend Mode

- **Versatile External Media Interface**
  - Optional MII interface in MAC mode allows AX88172A to work with external 100BASE-FX Ethernet PHY or HomePNA PHY
  - Optional Reverse-MII or Reverse-RMII interface in PHY mode allows AX88172A to work with external HomePlug PHY or glueless MAC-to-MAC connections
  - Optional Reverse-MII interface in Dual-PHY mode allows AX88172A to act as an Ethernet PHY or USB 2.0 PHY for external MAC device that needs Ethernet and USB in system application

- Supports 256/512 bytes (93c56/93c66) of serial EEPROM (for storing USB Descriptors)
- Supports automatic loading of Ethernet ID, USB Descriptors and Adapter Configuration from EEPROM after power-on initialization
- Provides optional serial interface, I2C, SPI and UART
- Integrates on-chip voltage regulator and only requires a single 3.3V power supply
- 12MHz and 25Mhz clock input from either crystal or oscillator source
- Integrates on-chip power-on reset circuit
- Small form factor with 64-pin LQFP (AX88772A) or 80-pin TQFP (AX88172A) RoHS compliant package
- Operating temperature range: 0˚C to 70˚C.

Product Description

The AX88772A/AX88172A Low-pin-count USB 2.0 to 10/100M Fast Ethernet controller is a high performance and highly integrated ASIC which enables low cost, small form factor, and simple plug-and-play Fast Ethernet network connection capability for desktops, notebook PC's, Ultra-Mobile PC's, docking stations, game consoles, digital-home appliances, and any embedded system using a standard USB port.

The AX88772A/AX88172A features a USB interface to communicate with a USB Host Controller and is compliant with USB specification V1.1 and V2.0. The AX88772A/AX88172A implements 10/100Mbps Ethernet LAN function based on IEEE802.3, and IEEE802.3u standards with 24KB of embedded SRAM for packet buffering. The AX88772A/AX88172A integrates an on-chip 10/100Mbps Ethernet PHY to simplify system design.

The AX88172A provides an optional External Media Interface (EMI) for external PHY or external MAC for different application purposes. The EMI can be a media-independent interface (MII) for implementing 100BASE-FX Ethernet or HomePNA functions. The EMI can also be a Reverse-MII or Reverse Reduced-MII (Reverse-RMII) for glueless MAC-to-MAC connections to any MCU with Ethernet MAC MII or RMII interface. In addition, the EMI can be configured to Dual-PHY mode allowing AX88172A to act as an Ethernet PHY or USB 2.0 PHY for external MAC device that needs Ethernet and USB interfaces in their system applications. The optional serial interface such as I2C, SPI, and UART are provided as a control channel from the USB Host Controller to communicate with the external MCU chip.

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Target Applications

PC/Internet


USB Dongle


Docking Station


Port Replicator
for Mobile Computer


USB KVME
Switch


Internet Security
USB Key


Card Reader


UWB/802.11n/WiMAX
USB Dongle


Media Gateway


UMPC


Pocketable Computer

Consumer Electronics


Portable Media Player


ePiano


TiVo Box


Game Console


IP STB


DVD-Recorder/DVR


IPTV

Figure 1 : Target Applications

Typical System Block Diagrams

- **Hosted by USB to operate with internal Ethernet PHY only**

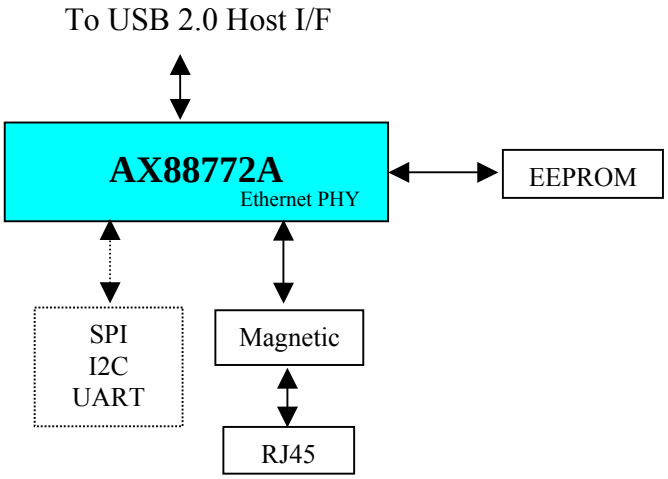

Figure 2 : USB 2.0 to LAN Adaptor (MAC mode)

- **Hosted by USB to operate with either internal Ethernet PHY or EMI (in MAC mode)**

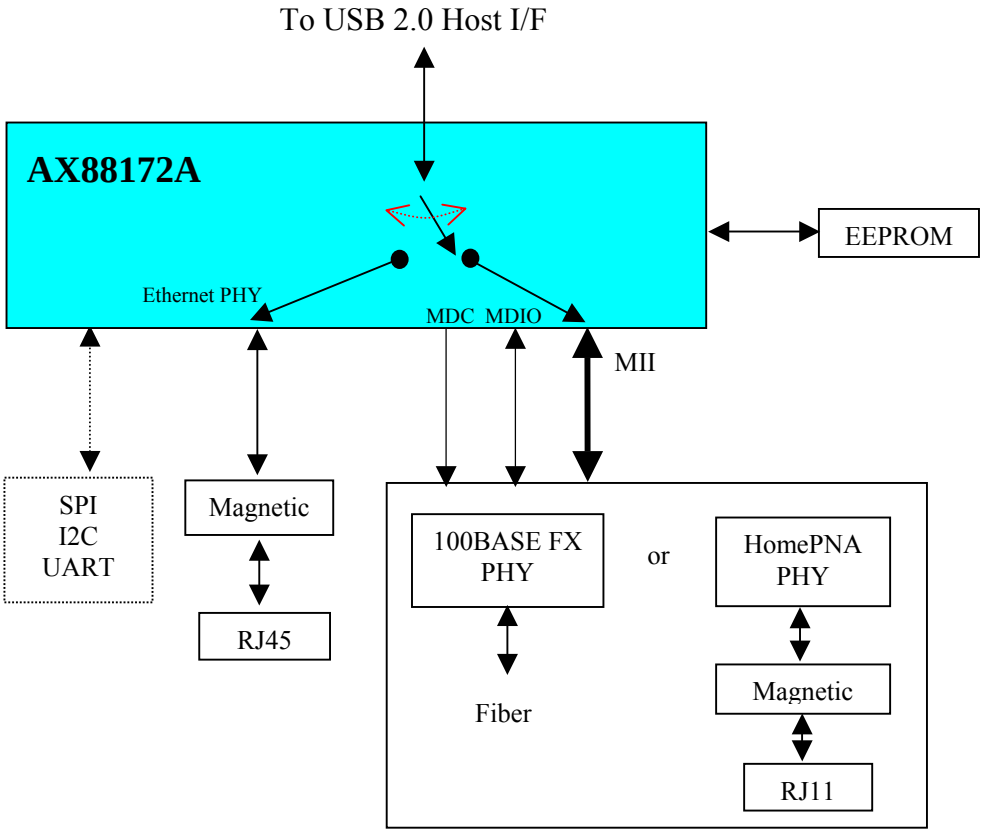

Figure 3 : USB 2.0 to Fast Ethernet and 100BASE-FX Fiber/HomePNA Combo (MAC mode)

- **Hosted by USB to operate with either internal Ethernet PHY (in MAC mode) or EMI (in PHY mode)**

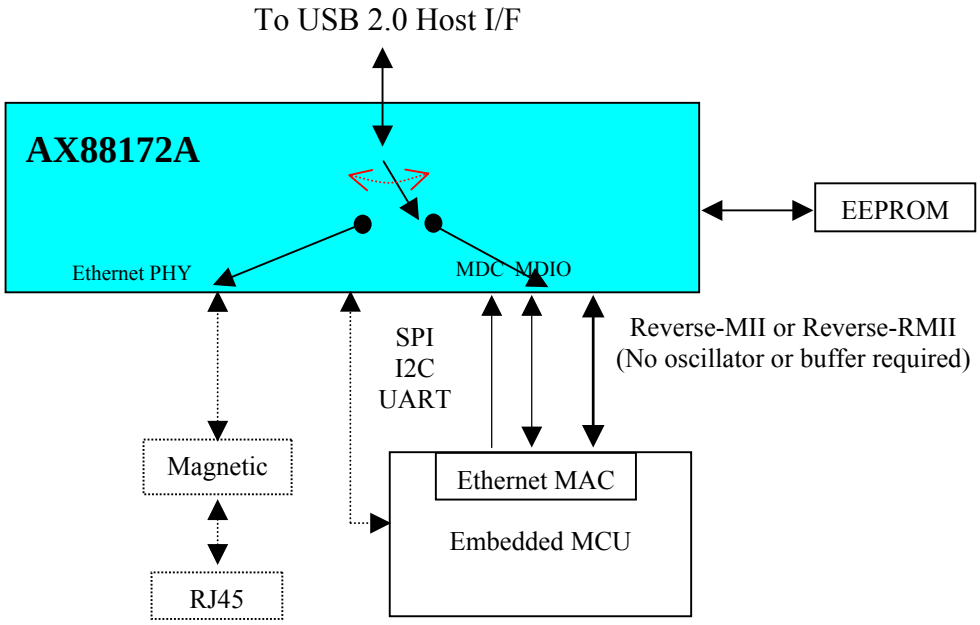

Figure 4 : Bridging Embedded MCU to USB 2.0 Host Interface (PHY mode)

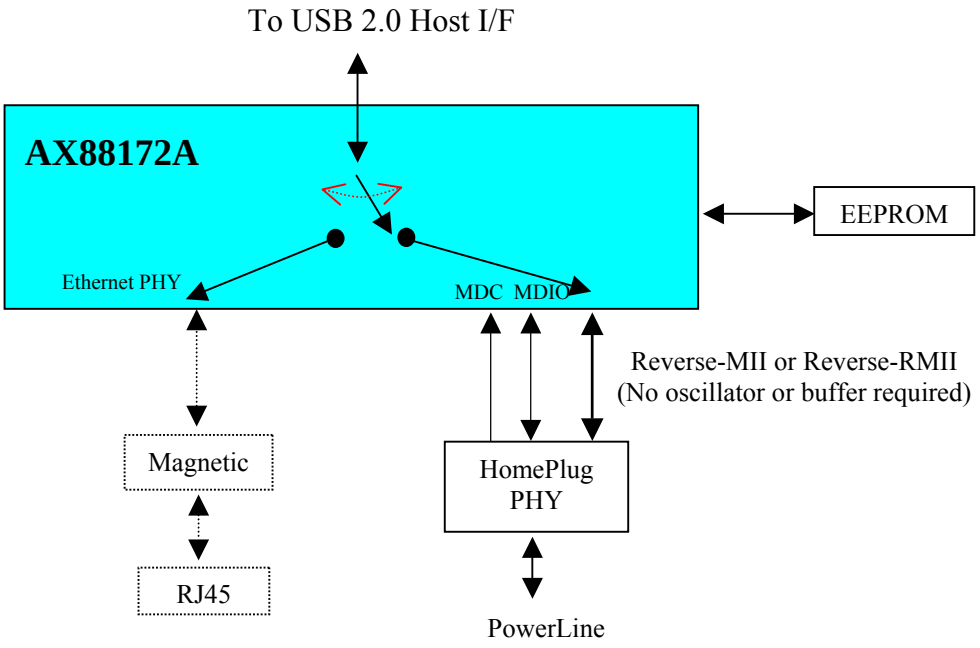

Figure 5 : USB 2.0 to HomePlug Adaptor (PHY mode)

- **Hosted by EMI to operate with either internal Ethernet PHY or USB PHY (in Dual-PHY mode)**

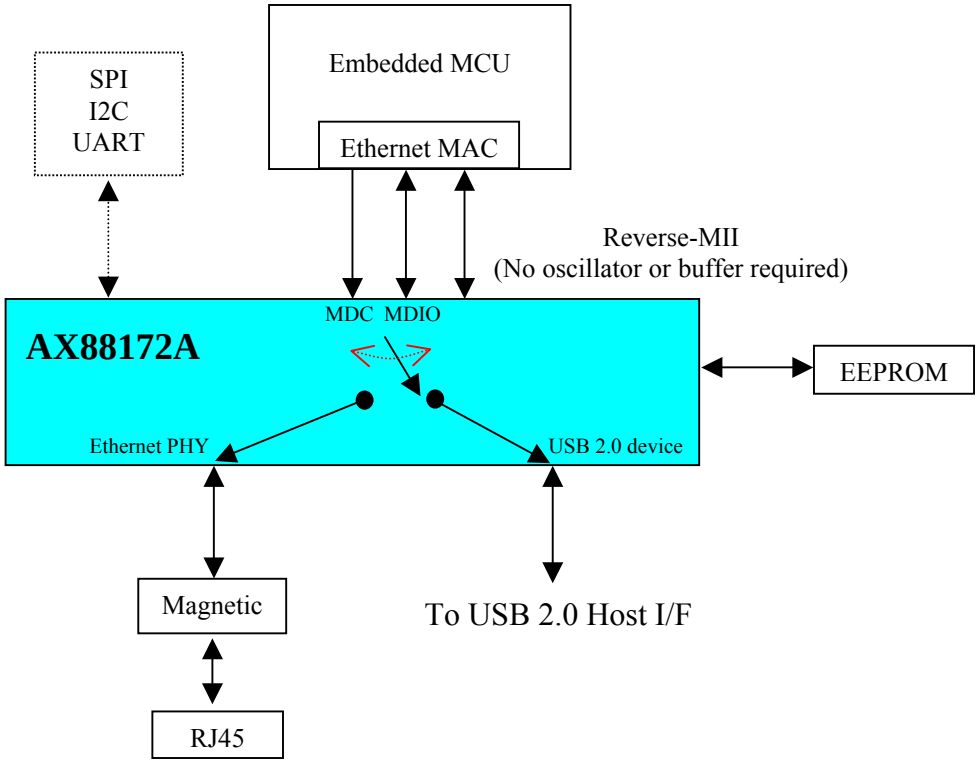

Figure 6 : Bridging Embedded MCU to either Ethernet PHY or USB 2.0 Interface

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1.0 Introduction

1.1 General Description

The AX88772A/AX88172A Low-pin-count USB 2.0 to 10/100M Fast Ethernet controller is a high performance and highly integrated ASIC which enables low cost, small form factor, and simple plug-and-play Fast Ethernet network connection capability for desktops, notebook PC's, Ultra-Mobile PC's, docking stations, game consoles, digital-home appliances, and any embedded system using a standard USB port.

The AX88772A/AX88172A features a USB interface to communicate with a USB Host Controller and is compliant with USB specification V1.1 and V2.0. The AX88772A/AX88172A implements a 10/100Mbps Ethernet LAN function based on IEEE802.3, and IEEE802.3u standards with 24KB of embedded SRAM for packet buffering. The AX88772A/AX88172A integrates an on-chip 10/100Mbps Ethernet PHY to simplify system design.

The AX88172A provides an optional External Media Interface (EMI) for external PHY or external MAC for different application purposes. The EMI can be a media-independent interface (MII) for implementing 100BASE-FX Ethernet or HomePNA functions. The EMI can also be a Reverse-MII or Reverse Reduced-MII (Reverse-RMII) for glueless MAC-to-MAC connections to any MCU with Ethernet MAC MII or RMII interface. In addition, the EMI can be configured to Dual-PHY mode allowing AX88172A to act as an Ethernet PHY or USB 2.0 PHY for external MAC device that needs Ethernet and USB interfaces in their system applications. The optional serial interface such as I2C, SPI, and UART are provided as a control channel from the USB Host Controller to communicate with the external MCU chip.

The AX88772A/AX88172A needs 12MHz clock for USB operation and 25Mhz clock for Fast Ethernet operation. The AX88772A is housed in the 64-pin LQFP and the AX88172A is housed in the 80-pin TQFP RoHS compliant package.

1.2 Block Diagram

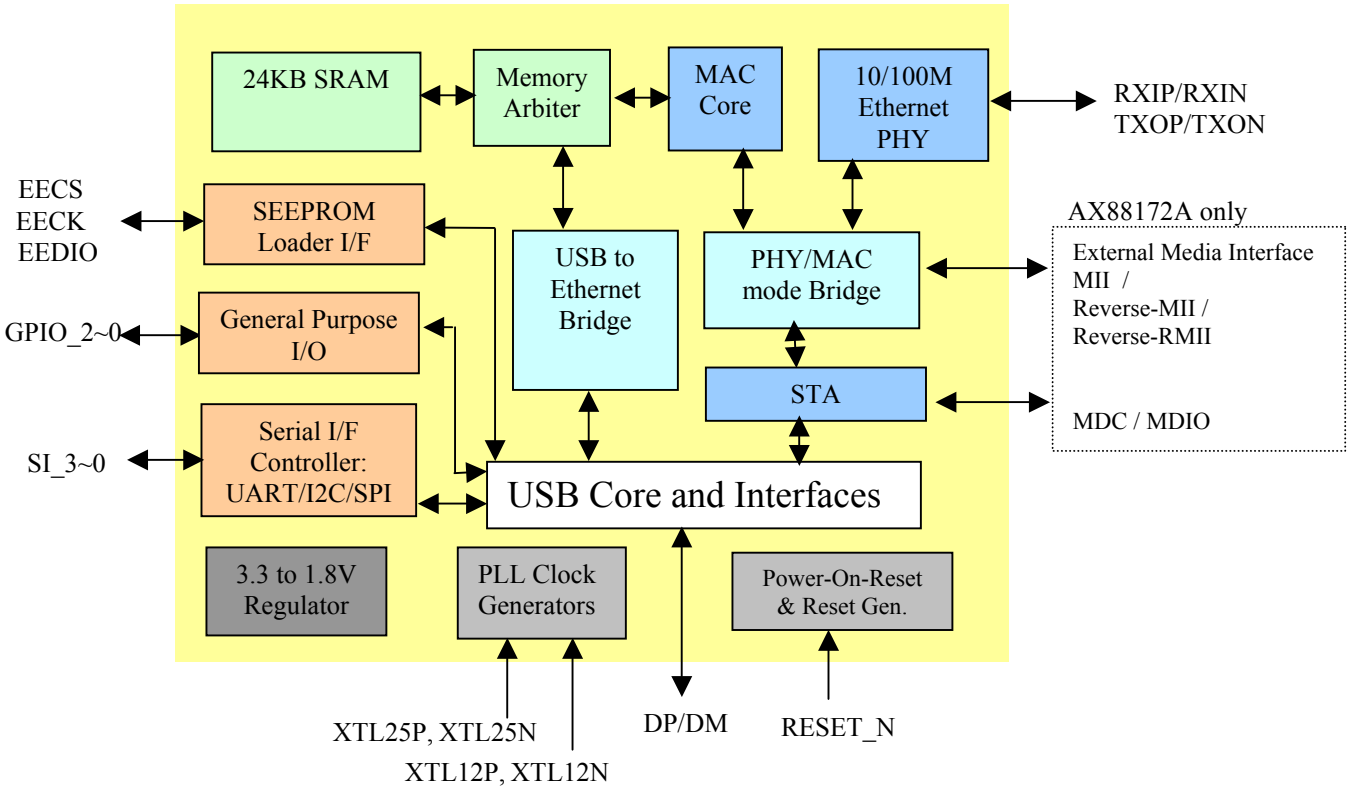


Figure 7 : AX88772A/AX88172A Block Diagram

1.3 Pinout Diagram

- AX88772A in 64-pin LQFP package

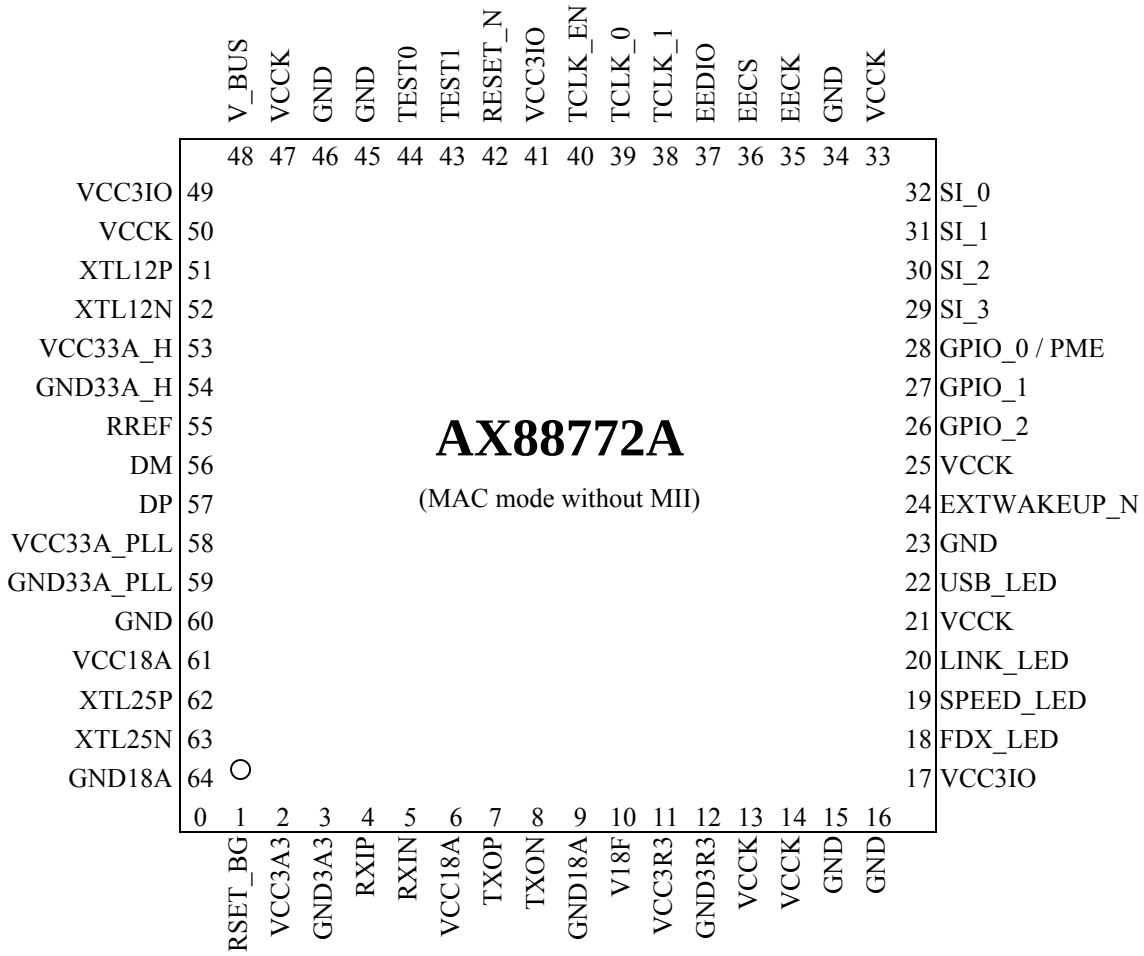


Figure 8 : AX88772A Pinout Diagram (MAC mode without MII)

- AX88172A in 80-pin TQFP package - MAC mode with MII

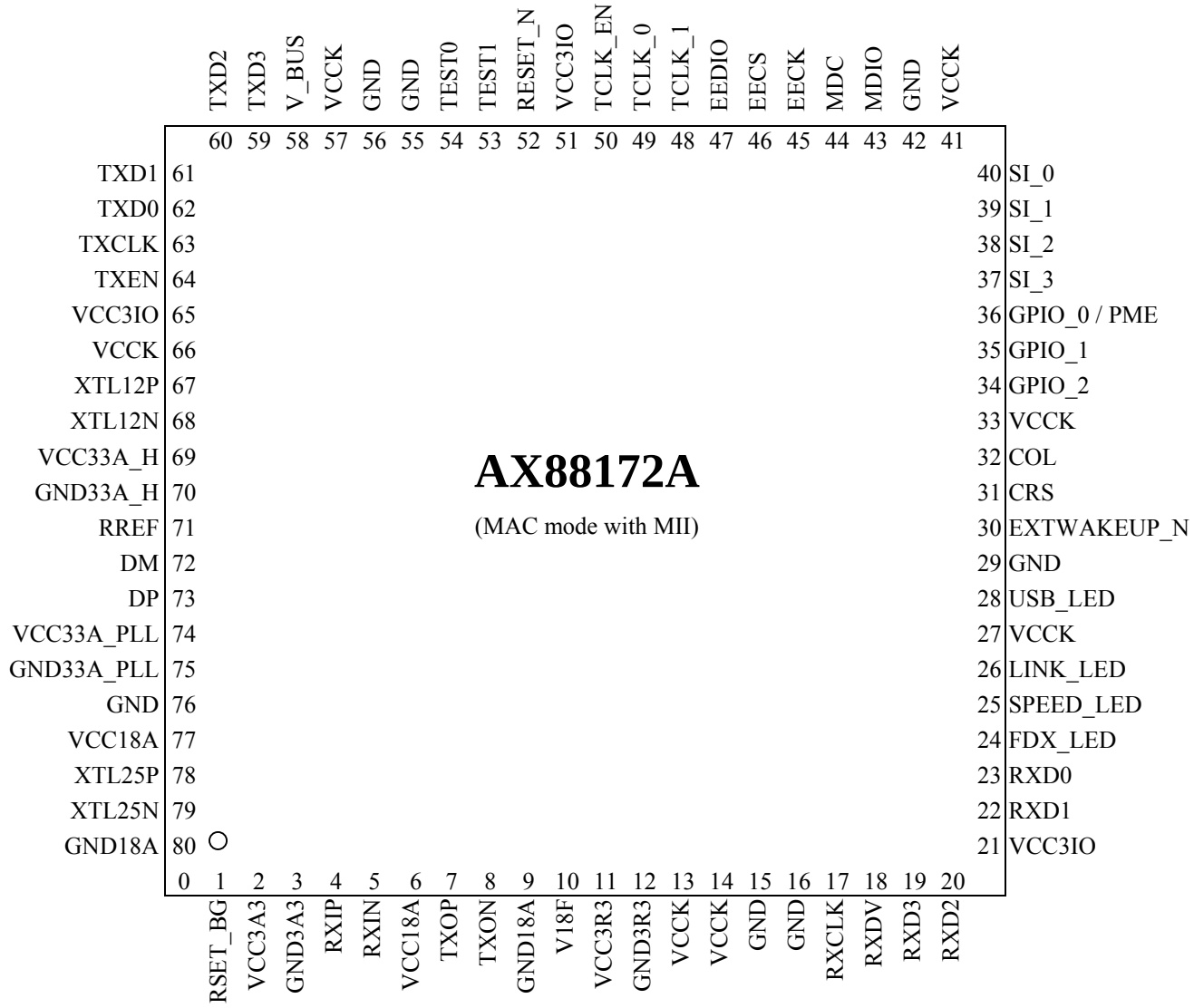


Figure 9 : AX88172A Pinout Diagram (MAC mode with MII)

- AX88172A in 80-pin TQFP package - PHY mode with Reverse-MII

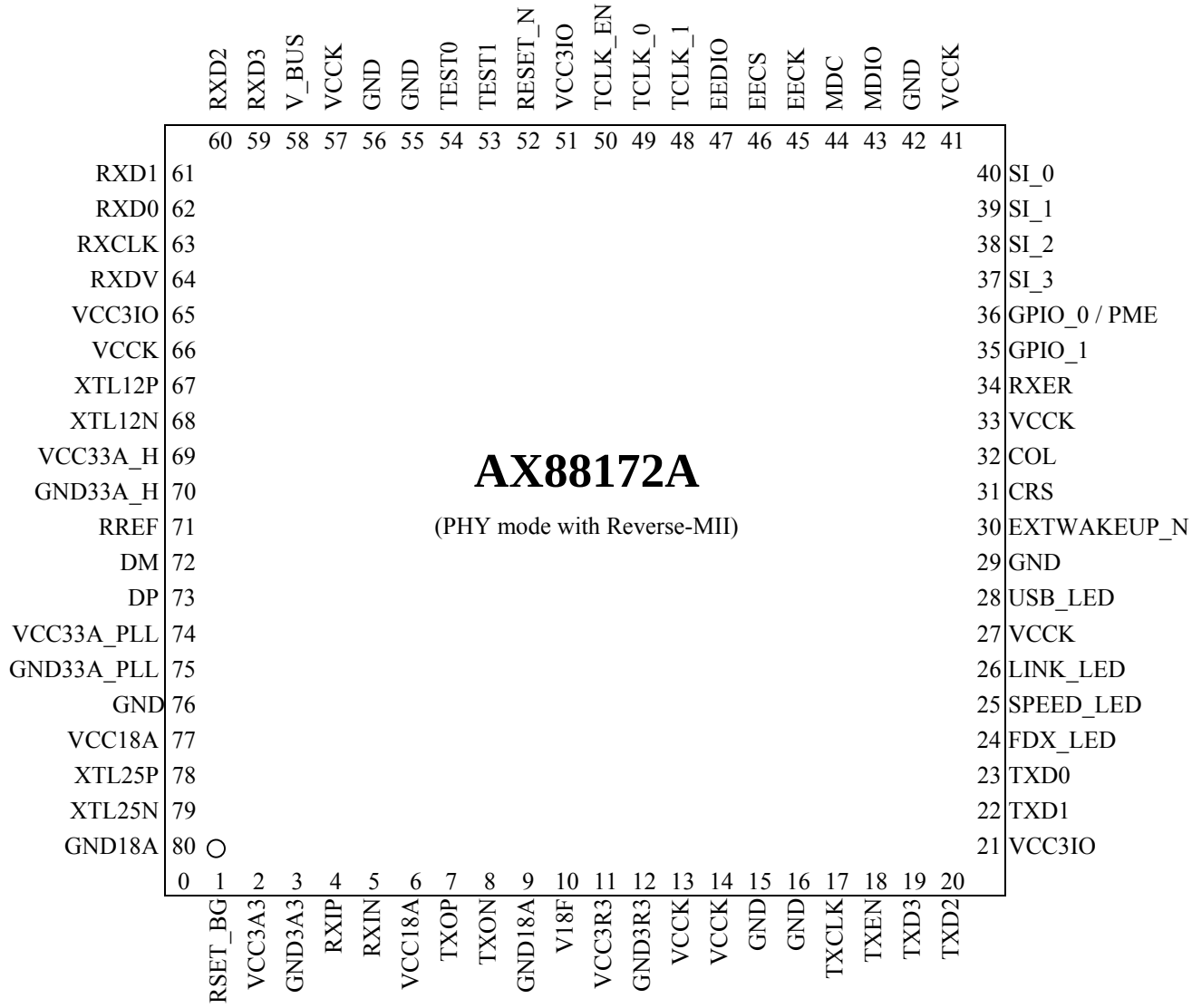


Figure 10 : AX88172A Pinout Diagram (PHY mode with Reverse-MII)

- AX88172A in 80-pin TQFP package - PHY mode with Reverse-RMII

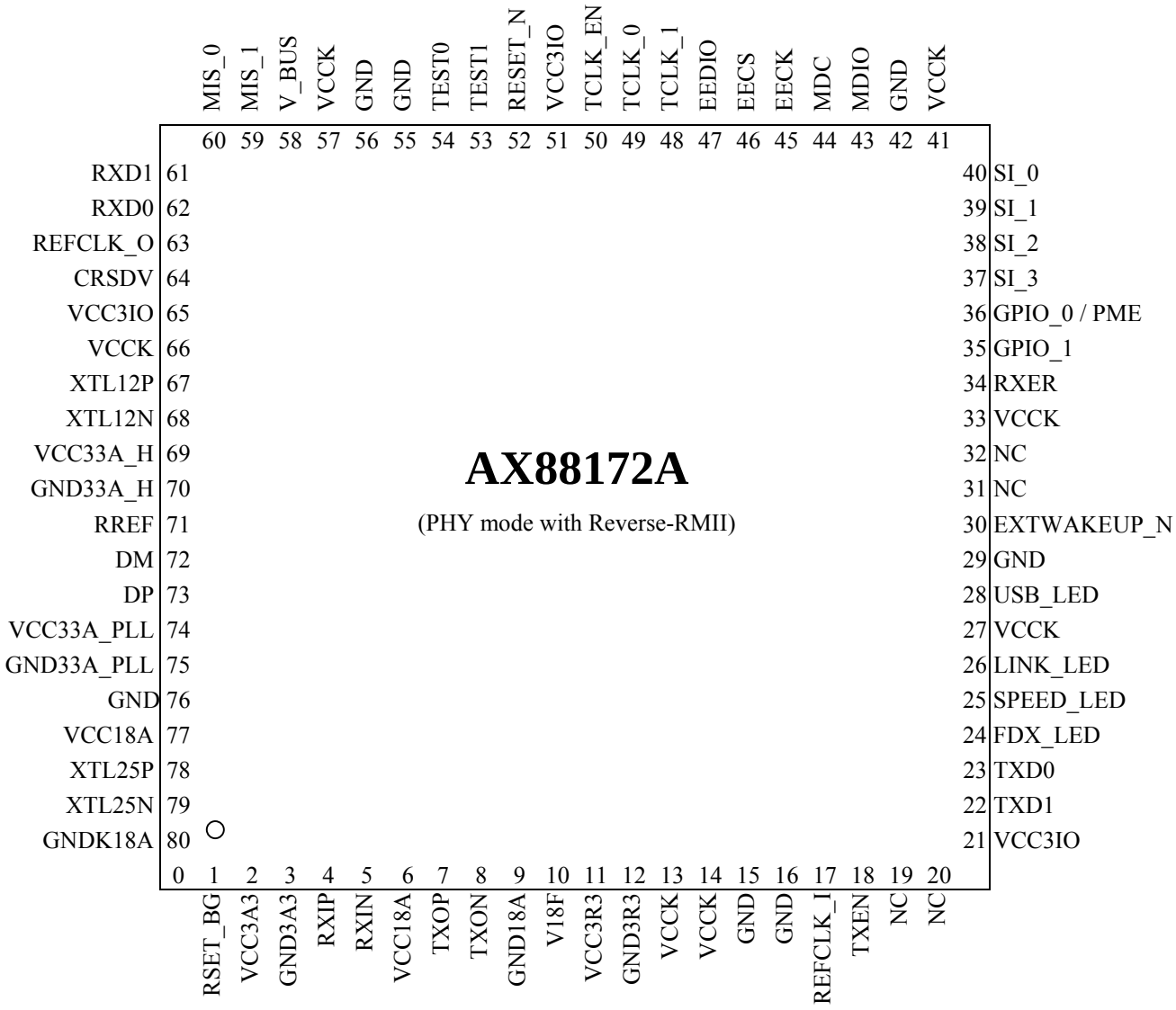


Figure 11 : AX88172A Pinout Diagram (PHY mode with Reverse-RMII)

2.0 Signal Description

The following abbreviations apply to the following pin description table.

I18	**Input, 1.8V**	**AO**	**Analog Output**
I3	**Input, 3.3V**	**AB**	**Analog Bi-directional I/O**
I5	**Input, 3.3V with 5V tolerant**	**PU**	**Internal Pull Up (75K)**
O3	**Output, 3.3V**	**PD**	**Internal Pull Down (75K)**
O5	**Output, 3.3V with 5V tolerant**	**P**	**Power Pin**
B5	**Bi-directional I/O, 3.3V with 5V tolerant**	**S**	**Schmitt Trigger**
		T	**Tri-stateable**
AI	**Analog Input**		

Note: Every output or bi-directional I/O pin is 8mA driving strength.

2.1 AX88772A 64-pin Pinout Description

Table 1 : AX88772A 64-pin Pinout Description

Pin Name	Type	Pin No	Pin Description
USB Interface			
DP	AB	57	USB 2.0 data positive pin.
DM	AB	56	USB 2.0 data negative pin.
VBUS	I5/PD/S	48	VBUS pin input. Please connect to USB bus power.
XTL12P	I3	51	12Mhz ±0.003%crystal or oscillator clock input. This clock is needed for USB PHY transceiver to operate.
XTL12N	O3	52	12Mhz crystal or oscillator clock output.
RREF	AI	55	For USB PHY's internal biasing. Please connect to analog GND through a resistor (12.1Kohm ±1%).
Serial EEPROM Interface			
EECK	B5/PD/T	35	EEPROM Clock. EECK is an output clock to EEPROM to provide timing reference for the transfer of EECS, and EEDIO signals. EECK only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down.
EECS	B5/PD/T	36	EEPROM Chip Select. EECS is asserted high synchronously with respect to rising edge of EECK as chip select signal. EECS only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down.
EEDIO	B5/PU/T	37	EEPROM Data In. EEDIO is the serial output data to EEPROM's data input pin and is synchronous with respect to the rising edge of EECK. EEDIO only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-up.
Ethernet PHY Interface			
XTL25P	I18	62	25Mhz ± 0.005% crystal or oscillator clock input. This clock is needed for the embedded 10/100M Ethernet PHY to operate.
XTL25N	O18	63	25Mhz crystal or oscillator clock output.
RXIP	AB	4	Receive data input positive pin for both 10BASE-T and 100BASE-TX.
RXIN	AB	5	Receive data input negative pin for both 10BASE-T and 100BASE-TX.
TXOP	AB	7	Transmit data output positive pin for both 10BASE-T and 100 BASE-TX
TXON	AB	8	Transmit data output negative pin for both 10BASE-T and 100 BASE-TX
RSET_BG	AO	1	For Ethernet PHY's internal biasing. Please connect to GND through a 12.1Kohm ±1% resistor.
LINK_LED	O5	20	Link status LED indicator. This pin drives low continuously when the Ethernet link is up and drives low and high in turn (blinking) when Ethernet PHY is in receiving or transmitting state.

FDX_LED	O5	18	Full Duplex and collision detected LED indicator. This pin drives low when the Ethernet PHY is in full-duplex mode and drives high when in half duplex mode. When in half duplex mode and the Ethernet PHY detects collision, it will be driven low (or blinking).
SPEED_LED	O5	19	Ethernet speed LED indicator. This pin drives low when the Ethernet PHY is in 100BASE-TX mode and drives high when in 10BASE-T mode.
Misc. Pins			
RESET_N	I5/PU/S	42	Chip reset input. Active low. This is the external reset source used to reset this chip. This input feeds to the internal power-on reset circuitry, which provides the main reset source of this chip. After completing reset, EEPROM data will be loaded automatically.
EXTWAKEUP_N	I5/PU/S	24	Remote-wakeup trigger from external pin. EXTWAKEUP_N should be asserted low for more than 2 cycles of 12MHz clock to be effective.
GPIO_2	B5/PD	26	General Purpose Input/ Output Pin 2.
GPIO_1	B5/PD	27	General Purpose Input/ Output Pin 1. This pin is default as input pin after power-on reset. This pin is also for Default WOL Ready Mode setting; please refer to section 2.3 Settings.
GPIO_0/PME	B5/PD	28	General Purpose Input/ Output Pin 0 or PME (Power Management Event). This pin is default as input pin after power-on reset. GPIO_0 also can be defined as PME output to indicate wake up event detected. Please refer to section 2.3 Settings.
SI_3	B5/PU	29	UART_RX or SPI_MISO. This is a multi-function pin determined by EEPROM Flag [1] setting. Please refer to section 2.3 Settings.
SI_2	B5/PU	30	UART_TX or SPI_MOSI. This is a multi-function pin determined by EEPROM Flag [1] setting. Please refer to section 2.3 Settings.
SI_1	B5/PU	31	I2C_SDA or SPI_SS. This is a multi-function pin determined by EEPROM Flag [1] setting. Please refer to section 2.3 Settings.
SI_0	B5/PU	32	I2C_SCLK or SPI_SCLK. This is a multi-function pin determined by EEPROM Flag [1] setting. Please refer to section 2.3 Settings.
USB_LED	O5	22	USB Speed indicator: When USB bus is in Full speed, this pin drives high continuously. When USB bus is in High speed, this pin drives low continuously. This pin drives high and low in turn (blinking) to indicate TX data transfer going on whenever the host controller sends bulk out data transfer.
TEST0	I5/S	44	Test pin. For normal operation, user should connect to ground.
TEST1	I5/S	43	Test pin. For normal operation, user should connect to ground.
TCLK_EN	I5/PD/S	40	Test pin. For normal operation, user should keep this pin NC.
TCLK_0	I5/PD	39	Test pin. For normal operation, user should keep this pin NC.
TCLK_1	I5/PD	38	Test pin. For normal operation, user should keep this pin NC.
On-chip Regulator Pins			
VCC3R3	P	11	3.3V Power supply to on-chip 3.3V to 1.8V voltage regulator.
GND3R3	P	12	Ground pin of on-chip 3.3V to 1.8V voltage regulator.
V18F	P	10	1.8V voltage output of on-chip 3.3V to 1.8V voltage regulator.
Power and Ground Pins			
VCCK	P	13, 14, 21, 25, 33, 47, 50	Digital Core Power. 1.8V.
VCC3IO	P	17, 41, 49	Digital I/O Power. 3.3V.
GND	P	15, 16, 23, 34, 45, 46, 60	Digital Ground.
VCC33A_H	P	53	Analog Power for USB transceiver. 3.3V.
GND33A_H	P	54	Analog Ground for USB transceiver.
VCC33A_PLL	P	58	Analog Power for USB PLL. 3.3V.
GND33A_PLL	P	59	Analog Ground for USB PLL.
VCC3A3	P	2	Analog Power for Ethernet PHY bandgap. 3.3V.
GND3A3	P	3	Analog Ground for Ethernet PHY.
VCC18A	P	6, 61	Analog Power for Ethernet PHY and 25Mhz crystal oscillator. 1.8V.

GND18A	P	9, 64	Analog Ground for Ethernet PHY and 25Mhz crystal oscillator.

2.2 AX88172A 80-pin Pinout Description

Table 2 : AX88172A 80-pin Pinout Description

Pin Name	Type	Pin No	Pin Description
USB Interface			
DP	AB	73	USB 2.0 data positive pin.
DM	AB	72	USB 2.0 data negative pin.
VBUS	I5/PD/S	58	VBUS pin input. Please connect to USB bus power.
XTL12P	I3	67	12Mhz ±0.003%crystal or oscillator clock input. This clock is needed for USB PHY transceiver to operate.
XTL12N	O3	68	12Mhz crystal or oscillator clock output.
RREF	AI	71	For USB PHY's internal biasing. Please connect to analog GND through a resistor (12.1Kohm ±1%).
Serial EEPROM Interface			
EECK	B5/PD/T	45	EEPROM Clock. EECK is an output clock to EEPROM to provide timing reference for the transfer of EECS, and EEDIO signals. EECK only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down.
EECS	B5/PD/T	46	EEPROM Chip Select. EECS is asserted high synchronously with respect to rising edge of EECK as chip select signal. EECS only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down.
EEDIO	B5/PU/T	47	EEPROM Data In. EEDIO is the serial output data to EEPROM's data input pin and is synchronous with respect to the rising edge of EECK. EEDIO only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-up.
Ethernet PHY Interface			
XTL25P	I18	78	25Mhz ± 0.005% crystal or oscillator clock input. This clock is needed for the embedded 10/100M Ethernet PHY to operate.
XTL25N	O18	79	25Mhz crystal or oscillator clock output.
RXIP	AB	4	Receive data input positive pin for both 10BASE-T and 100BASE-TX.
RXIN	AB	5	Receive data input negative pin for both 10BASE-T and 100BASE-TX.
TXOP	AB	7	Transmit data output positive pin for both 10BASE-T and 100 BASE-TX
TXON	AB	8	Transmit data output negative pin for both 10BASE-T and 100 BASE-TX
RSET_BG	AO	1	For Ethernet PHY's internal biasing. Please connect to GND through a 12.1Kohm ±1% resistor.
LINK_LED	O5	26	Link status LED indicator. This pin drives low continuously when the Ethernet link is up and drives low and high in turn (blinking) when Ethernet PHY is in receiving or transmitting state.
FDX_LED	O5	24	Full Duplex and collision detected LED indicator. This pin drives low when the Ethernet PHY is in full-duplex mode and drives high when in half duplex mode. When in half duplex mode and the Ethernet PHY detects collision, it will be driven low (or blinking).
SPEED_LED	O5	25	Ethernet speed LED indicator. This pin drives low when the Ethernet PHY is in 100BASE-TX mode and drives high when in 10BASE-T mode.
Misc. Pins			
RESET_N	I5/PU/S	52	Chip Reset Input. RESET_N pin is active low. When asserted, it puts the entire chip into reset state immediately. After completing reset, EEPROM data will be loaded automatically.
EXTWAKEUP_N	I5/PU/S	30	Remote-wakeup trigger from external pin. EXTWAKEUP_N should be asserted low for more than 2 cycles of 12MHz clock to be effective.
GPIO_2 / RXER	B5/PD	34	General Purpose Input/ Output Pin 2. This pin is GPIO_2 in MAC mode, but it will be redefined as RXER (receive error) or GPIO_2 depending on EEPROM Flag [3] in PHY mode.

GPIO_1	B5/PD	35	General Purpose Input/ Output Pin 1. This pin is default as input pin after power-on reset. This pin is also for Default WOL Ready Mode setting; please refer to section 2.3 Settings.
GPIO_0 / PME	B5/PD	36	General Purpose Input/ Output Pin 0 or PME (Power Management Event). This pin is default as input pin after power-on reset. GPIO_0 also can be defined as PME output to indicate wake up event detected. Please refer to section 2.3 Settings.
SI_3	B5/PU	37	UART_RX or SPI_MISO. This is a multi-function pin determined by EEPROM Flag [1] setting. Please refer to section 2.3 Settings.
SI_2	B5/PU	38	UART_TX or SPI_MOSI. This is a multi-function pin determined by EEPROM Flag [1] setting. Please refer to section 2.3 Settings.
SI_1	B5/PU	39	I2C_SDA or SPI_SS. This is a multi-function pin determined by EEPROM Flag [1] setting. Please refer to section 2.3 Settings.
SI_0	B5/PU	40	I2C_SCLK or SPI_SCLK. This is a multi-function pin determined by EEPROM Flag [1] setting. Please refer to section 2.3 Settings.
USB_LED	O5	28	USB Speed indicator: When USB bus is in Full speed, this pin drives high continuously. When USB bus is in High speed, this pin drives low continuously. This pin drives high and low in turn (blinking) to indicate TX data transfer going on whenever the host controller sends bulk out data transfer.
TEST0	I5/S	54	Test pin. For normal operation, user should connect to ground.
TEST1	I5/S	53	Test pin. For normal operation, user should connect to ground.
TCLK_EN	I5/PD/S	50	Test pin. For normal operation, user should keep this pin NC.
TCLK_0	I5/PD	49	Test pin. For normal operation, user should keep this pin NC.
TCLK_1	I5/PD	48	Test pin. For normal operation, user should keep this pin NC.
On-chip Regulator Pins			
VCC3R3	P	11	3.3V Power supply to on-chip 3.3V-to-1.8V voltage regulator.
GND3R3	P	12	Ground pin of on-chip 3.3V-to-1.8V voltage regulator.
V18F	P	10	1.8V voltage output of on-chip 3.3V-to-1.8V voltage regulator.
Power and Ground Pins			
VCCK	P	13, 14, 27, 33, 41, 57, 66,	Digital Core Power. 1.8V.
VCC3IO	P	21, 51, 65	Digital I/O Power. 3.3V.
GND	P	15, 16, 29, 42, 55, 56, 76	Digital Ground.
VCC33A_H	P	69	Analog Power for USB transceiver. 3.3V.
GND33A_H	P	70	Analog Ground for USB transceiver.
VCC33A_PLL	P	74	Analog Power for USB PLL. 3.3V.
GND33A_PLL	P	75	Analog Ground for USB PLL.
VCC3A3	P	2	Analog Power for Ethernet PHY bandgap. 3.3V.
GND3A3	P	3	Analog Ground for Ethernet PHY.
VCC18A	P	6, 77	Analog Power for Ethernet PHY and 25Mhz crystal oscillator. 1.8V.
GND18A	P	9, 80	Analog Ground for Ethernet PHY and 25Mhz crystal oscillator.

External Media Interface: MAC Mode with MII Interface			
RXCLK	I5/PD	17	Receive Clock. RXCLK is received from PHY to provide timing reference for the transfer of RXD [3:0] and RXDV signals on receive direction of MII interface.
RXDV	I5/PD	18	Receive Data Valid. RXDV is asserted high when valid data is present on RXD [3:0]. It is driven synchronously with respect to RXCLK by PHY.
RXD [3:0]	I5/PD	19, 20, 22, 23	Receive Data. RXD [3:0] is driven synchronously with respect to RXCLK by PHY.
CRS	I5/PD	31	Carrier Sense. CRS is asserted high asynchronously by the PHY when either transmit or receive medium is non-idle.
COL	I5/PD	32	Collision. COL is driven high by PHY when the collision is detected.

TXCLK	I5/PD	63	Transmit Clock. TXCLK is received from PHY to provide timing reference for the transfer of TXD [3:0] and TXEN signals on transmit direction of MII interface.
TXEN	O3	64	Transmit Enable. TXEN is asserted high to indicate a valid TXD [3:0]. It is transitioned synchronously with respect to the rising edge of TXCLK.
TXD [3:0]	O3	59, 60, 61, 62	Transmit Data. TXD [3:0] is transitioned synchronously with respect to the rising edge of TXCLK. Note TXD [3:2] are also used as Chip Operation Mode selection pins; please refer to section 2.3 Settings.
MDC	O3/PD	44	Station management clock output to PHY. All data transferred on MDIO are synchronized to the rising edge of this clock. The frequency of MDC is 1.5MHz.
MDIO	B5/PU	43	Station management data input/output. Serial data input/output transferred from/to the PHYs. The transfer protocol conforms to the IEEE 802.3u MII spec.

External Media Interface: PHY Mode with Reverse-MII Interface			
TXCLK	O3/T	17	Transmit Clock. This clock is provided to supply to the TX_CLK of externally connected Ethernet MAC device with MII. This pin is tri-stated in isolate mode.
TXEN	I5/PD	18	Transmit enable. TXEN is asserted high to indicate a valid TXD [3:0]. It should be driven synchronously with respect to the rising edge of TXCLK by the externally connected Ethernet MAC device with MII.
TXD [3:0]	I5/PD	19, 20, 22, 23	Transmit Data. TXD [3:0] should be driven synchronously with respect to the rising edge of TXCLK by the externally connected Ethernet MAC device with MII.
CRS	O3/PD/T	31	Carrier Sense. CRS is asserted high by AX88172A when RXDV is asserted high in Reverse-MII mode. This pin is tri-stated in isolate mode.
COL	O3/PD/T	32	Collision. COL is always driven low because AX88172A is operating in 100M/full-duplex mode internally in Reverse-MII mode. This pin is tri-stated in isolate mode.
RXER	O3/PD/T	34	Receive Error. RXER is always driven low by AX88172A in Reverse-MII mode. This pin is tri-stated in isolate mode.
RXCLK	O3/T	63	Receive clock. This clock is provided to supply to the RX_CLK of externally connected Ethernet MAC device with MII. This pin is tri-stated in isolate mode.
RXDV	O3/T	64	Receive Data Valid. RXDV is asserted high when valid data is present on RXD [3:0]. It is transitioned synchronously with respect to RXCLK from AX88172A to the externally connected Ethernet MAC device with MII. This pin is tri-stated in isolate mode.
RXD [3:0]	O3/T	59, 60, 61, 62	Receive Data. RXD [3:0] is transitioned synchronously with respect to RXCLK from AX88172A to the externally connected Ethernet MAC device with MII. Note that RXD [3:2] are also used as Chip Operation Mode selection pins. Please refer to section 2.3 Settings. These pins are tri-stated in isolate mode.
MDC	I5/PD	44	Station Management clock input from the externally connected Ethernet MAC device. All data transferred on MDIO are synchronized to the rising edge of this clock.
MDIO	B5/PU	43	Station Management Data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.

External Media Interface: PHY Mode with Reverse-RMII Interface			
REFCLK_I	I5	17	50Mhz +/-50ppm Reference clock input for RMII receive, transmit and control signals. If externally connected Ethernet MAC device with RMII can't provide 50Mhz Reference clock to AX88172A, then user can connect this pin to REFCLK_O and use REFCLK_O to supply clock to the externally connected Ethernet MAC device at the same time.

TXEN	I5/PD	18	Transmit Enable from the externally connected Ethernet MAC device with RMII.
TXD [1:0]	I5/PD	22, 23	Transmit Data from the externally connected Ethernet MAC device with RMII.
NC	I5/PD	19, 20	NC
NC	O3/PD	31, 32	NC
RXER	O3/PD/T	34	Receive Error. RXER is always driven low by AX88172A in Reverse-RMII mode. This pin is tri-stated in isolate mode.
MIS_1	I5/PD	59	External Media Interface Select 1. This is used as Chip Operation Mode selection pin; please refer to section 2.3 Settings.
MIS_0	I5/PD	60	External Media Interface Select 0. This is used as Chip Operation Mode selection pin; please refer to section 2.3 Settings.
REFCLK_O	O3	63	50Mhz Reference clock output. If the externally connected Ethernet MAC device can't supply 50Mhz reference clock, this clock can be used to supply to the REF_CLK of externally connected Ethernet MAC device with RMII and the REFCLK_I of this chip.
CRSDV	O3/T	64	Carrier Sense and Receive Data Valid to the externally connected Ethernet MAC device with RMII. This pin is tri-stated in isolate mode.
RXD [1:0]	O3/T	61, 62	Receive Data to the externally connected Ethernet MAC device with RMII. These pins are tri-stated in isolate mode.
MDC	I5/PD	44	Station Management clock input from the externally connected Ethernet MAC device. All data transferred on MDIO are synchronized to the rising edge of this clock.
MDIO	B5/PU	43	Station Management Data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.

2.3 Hardware Setting For Operation Mode And Multi-Function Pins

Please contact ASIX for receiving “AX88x72A Full Datasheet” which contains detailed description of section 2.3 and section 3, 4, 5, 6, 7, 8.

3.0 Function Description

3.1 USB Core and Interface
3.2 10/100M Ethernet PHY
3.3 MAC Core
3.4 Operation Mode
3.5 Station Management (STA)
3.6 Memory Arbiter
3.7 USB to Ethernet Bridge
3.8 Serial EEPROM Loader
3.9 General Purpose I/O
3.10 Serial Interface Controller
3.11 Clock Generation
3.12 Reset Generation
3.13 Voltage Regulator

4.0 Serial EEPROM Memory Map

4.1 Detailed Description

5.0 USB Configuration Structure

5.1 USB Configuration
5.2 USB Interface
5.3 USB Endpoints

6.0 USB Commands

6.1 USB Standard Commands
6.2 USB Vendor Commands
6.2.1 Detailed Register Description
6.2.2 Command Block Wrapper for Serial Interface
6.2.2.1 UART controller

6.2.2.2 I2C controller
6.2.2.3 SPI controller

6.3 Interrupt Endpoint

7.0 Embedded Ethernet PHY Register Description

7.1 PHY Register Detailed Description
7.1.1 Basic Mode Control Register (BMCR)
7.1.2 Basic Mode Status Register (BMSR)
7.1.3 PHY Identifier Register 1
7.1.4 PHY Identifier Register 2
7.1.5 Auto Negotiation Advertisement Register (ANAR)
7.1.6 Auto Negotiation Link Partner Ability Register (ANLPAR)
7.1.7 Auto Negotiation Expansion Register (ANER)

8.0 Station Management Registers in PHY/Dual-PHY Mode

8.1 PHY/Dual-PHY Mode Detailed Register Description
8.1.1 PHY Mode Basic Mode Control Register (PM_BMCR)
8.1.2 PHY Mode Basic Mode Status Register (PM_BMSR)
8.1.3 PHY Mode PHY Identifier Register 1
8.1.4 PHY Mode PHY Identifier Register 2
8.1.5 PHY Mode Auto Negotiation Advertisement Register (PM_ANAR)
8.1.6 PHY Mode Auto Negotiation Link Partner Ability Register (PM_ANLPAR)
8.1.7 PHY Mode Auto Negotiation Expansion Register (PM_ANER)
8.1.8 PHY Mode Control Register (PM_Control)

9.0 Electrical Specifications

9.1 DC Characteristics

9.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VCCK	Digital core power supply	- 0.3 to 2.16	V
VCC18A	Analog Power. 1.8V	- 0.3 to 2.16	V
VCC3IO	Power supply of 3.3V I/O	- 0.3 to 4	V
VCC3R3	Power supply of on-chip voltage regulator	- 0.3 to 4	V
VCC3A3	Analog Power 3.3V for Ethernet PHY bandgap	- 0.3 to 3.8	V
VCC33A_PLL	Analog Power 3.3V for USB PLL.	- 0.3 to 4	V
VCC33A_H	Analog Power 3.3V for USB TX and RX	- 0.3 to 4	V
V_{IN18}	Input voltage of 1.8V I/O	- 0.3 to 2.16	V
V_{IN3}	Input voltage of 3.3V I/O	- 0.3 to 4.0	V
	Input voltage of 3.3V I/O with 5V tolerant	- 0.3 to 5.8	V
T_{STG}	Storage temperature	- 40 to 150	℃
I_{IN}	DC input current	20	mA
I_{OUT}	Output short circuit current	20	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the optional sections of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

9.1.2 Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
VCCK	Digital core power supply	1.62	1.8	1.98	V
VCC18A	Analog core power supply	1.62	1.8	1.98	V
VCC3R3	Power supply of on-chip voltage regulator	2.97	3.3	3.63	V
VCC3IO	Power supply of 3.3V I/O	2.97	3.3	3.63	V
VCC33A_H	Analog Power 3.3V for USB TX and RX	2.97	3.3	3.63	V
VCC33A_PLL	Analog Power 3.3V for USB PLL.	2.97	3.3	3.63	V
VCC3A3	Analog power supply for bandgap	2.97	3.3	3.63	V
V_{IN18}	Input voltage of 1.8 V I/O	0	1.8	1.98	V
V_{IN3}	Input voltage of 3.3 V I/O	0	3.3	3.63	V
	Input voltage of 3.3 V I/O with 5V tolerance	0	3.3	5.25	V
T_j	Commercial junction operating temperature	0	25	125	℃
T_a	Commercial operating temperature	0	-	70	℃

- Thermal Characteristics

Symbol	Parameter		Rating	Unit
Θ_{JC}	Thermal resistance of junction to case	LQFP 64(AX88772A)	13.1	°C/W
		TQFP 80(AX88172A)	27.5	°C/W
Θ_{JA}	Thermal resistance of junction to ambient	Still air,LQFP 64(AX88772A)	45.1	°C/W
		Still air,TQFP 80(AX88172A)	55.2	°C/W

9.1.3 Leakage Current and Capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance		-	2.2	-	pF
C_{OUT}	Output capacitance		-	2.2	-	pF
C_{BID}	Bi-directional buffer capacitance		-	2.2	-	pF

Note: The capacitance listed above does not include pad capacitance and package capacitance. One can estimate pin capacitance by adding a pad capacitance of about 0.5pF to the package capacitance.

9.1.4 DC Characteristics of 3.3V I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 3.3V I/O	3.3V I/O	2.97	3.3	3.63	V
Tj	Junction temperature		0	25	125	℃
Vil	Input low voltage	LVTTL	-	-	0.8	V
Vih	Input high voltage		2.0	-	-	V
Vt	Switching threshold			1.5		V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage	Iol = 8mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -8mA	2.4	-	-	V
Rpu	Input pull-up resistance	V_{in} = 0	40	75	190	KΩ
Rpd	Input pull-down resistance	V_{in} = VCC3IO	40	75	190	KΩ
Iin	Input leakage current	Vin = VCC3IO or 0	-10	±1	10	μA
	Input leakage current with pull-up resistance	Vin = 0	-15	-45	-85	μA
	Input leakage current with pull-down resistance	Vin = VCC3IO	15	45	85	μA
I_{OZ}	Tri-state output leakage current		-10	±1	10	μA

9.1.5 DC Characteristics of 3.3V with 5V Tolerance I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 3.3V I/O	3.3V I/O	2.97	3.3	3.63	V
Tj	Junction temperature		0	25	125	℃
Vil	Input low voltage	LVTTL	-	-	0.8	V
Vih	Input high voltage		2.0	-	-	V
Vt	Switching threshold			1.5		V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage	Iol = 8mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -8mA	2.4	-	-	V
Rpu	Input pull-up resistance	V_{in} = 0	40	75	190	KΩ
Rpd	Input pull-down resistance	V_{in} = VCC3IO	40	75	190	KΩ
Iin	Input leakage current	Vin = 5.5V or 0		±5		μA
	Input leakage current with pull-up resistance	Vin = 0	-15	-45	-85	μA
	Input leakage current with pull-down resistance	Vin = VCC3IO	15	45	85	μA
I_{OZ}	Tri-state output leakage current	V_{in} = 5.5V or 0		±10		μA

9.1.6 DC Characteristics of Voltage Regulator

Symbol	Description	Conditions	Min	Typ	Max	Unit
VCC3R3	Power supply of on-chip voltage regulator.		3.0	3.3	3.6	V
Tj	Operating junction temperature.		0	25	125	℃
Iload	Driving current.	Normal operation	-	-	240	mA
		Standby mode enabled	-	-	30	mA
V18F	Output voltage of on-chip voltage regulator.	VCC3R3 = 3.3V	1.71	1.8	1.89	V
Vdrop	Dropout voltage.	△V18F = -1%, Iload = 10mA	-	0.1	0.2	V
$\frac{\triangle V18F}{(\triangle VCC3R3 \times V18F)}$	Line regulation.	VCC3R3 = 3.3V, Iload = 50mA	-	0.2	0.4	%/V
$\frac{\triangle V18F}{(\triangle Iload \times V18F)}$	Load regulation.	VCC3R3 = 3.3V, 1mA ≦ Iload ≦ 240mA	-	0.02	0.05	%/mA
$\frac{\triangle V18F}{\triangle Tj}$	Temperature coefficient.	VCC3R3 = 3.3V,-40℃ ≦ Tj ≦ 125℃	-	+/-0.2	+/-0.5	mV/℃
Iq_25℃	Quiescent current at 25 ℃.	VCC3R3 = 3.3V	-	70	100	μA
		VCC3R3 = 3.3V	-	100	125	μA
Iq_125℃	Quiescent current at 125 ℃.	VCC3R3 = 3.3V	-	85	115	μA
		VCC3R3 = 3.3V	-	125	170	μA
Cout	Output external capacitor.		0.1	1	-	μF
ESR	Allowable effective series resistance of external capacitor.		-	0.5	1	Ω

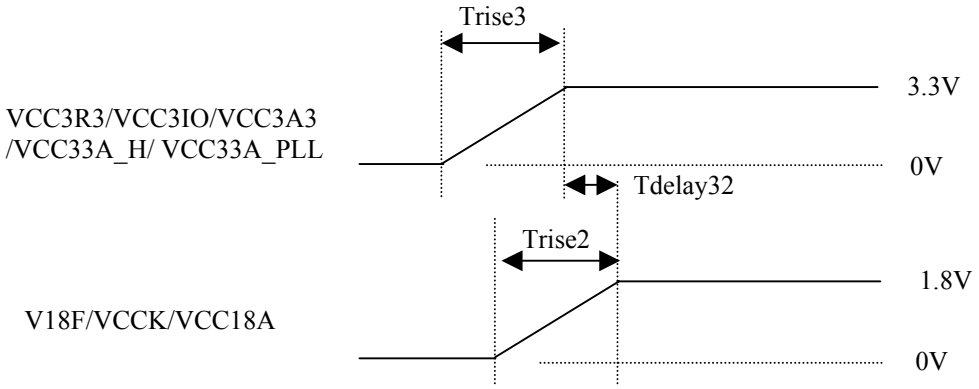
9.2 Power Consumption

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_{VCCK}	Current Consumption of VCCK	Operating at Ethernet 100Mbps full duplex mode and USB High speed mode		47.5		mA
I_{VCC18A}	Current Consumption of VCC18A			39.3		mA
I_{VCC3IO}	Current Consumption of VCC3IO			16.6		mA
I_{VCC33A}	Current Consumption of VCC33A_H + VCC33A_PLL + VCC33A_PLL			35.4		mA
I_{VCCK}	Current Consumption of VCCK	Operating at Ethernet 100Mbps full duplex mode and USB Full speed mode		44.3		mA
I_{VCC18A}	Current Consumption of VCC18A			39.3		mA
I_{VCC3IO}	Current Consumption of VCC3IO			12.9		mA
I_{VCC33A}	Current Consumption of VCC33A_H + VCC33A_PLL + VCC33A_PLL			28.7		mA
I_{VCCK}	Current Consumption of VCCK	Operating at Ethernet 10Mbps full duplex mode and USB High speed mode		19.3		mA
I_{VCC18A}	Current Consumption of VCC18A			6.3		mA
I_{VCC3IO}	Current Consumption of VCC3IO			8.3		mA
I_{VCC33A}	Current Consumption of VCC33A_H + VCC33A_PLL + VCC33A_PLL			38.8		mA
I_{VCCK}	Current Consumption of VCCK	Operating at Ethernet 10Mbps full duplex mode and USB Full speed mode		14.9		mA
VCC18A	Current Consumption of VCC18A			6.2		mA
I_{VCC3IO}	Current Consumption of VCC3IO			4.9		mA
I_{VCC33A}	Current Consumption of VCC33A_H + VCC33A_PLL + VCC33A_PLL			32.3		mA
I_{VCCK}	Current Consumption of VCCK	Suspend (the embedded Ethernet PHY is powered down)		2.0		µA
I_{VCC18A}	Current Consumption of VCC18A			49.3		µA
I_{VCC3IO}	Current Consumption of VCC3IO			0.7		mA
I_{VCC33A}	Current Consumption of VCC33A_H + VCC33A_PLL + VCC33A_PLL			0.2		mA
I_{VCCK}	Current Consumption of VCCK	AX88172A in USB Full speed, Rev-MII operation and internal PHY power save (BMCR[11] bit = 1)		19		mA
I_{VCC18A}	Current Consumption of VCC18A			3.4		mA
I_{VCC3IO}	Current Consumption of VCC3IO			8.5		mA
I_{VCC33A}	Current Consumption of VCC33A_H + VCC33A_PLL + VCC33A_PLL			30.9		mA
I_{VCCK}	Current Consumption of VCCK	AX88172A in USB High speed, Rev-MII operation and internal PHY power save (BMCR[11] bit = 1)		22		mA
I_{VCC18A}	Current Consumption of VCC18A			3.4		mA
I_{VCC3IO}	Current Consumption of VCC3IO			11.5		mA
I_{VCC33A}	Current Consumption of VCC33A_H + VCC33A_PLL + VCC33A_PLL			36.9		mA
I_{DEVICE}	Power consumption of AX88772A/AX88172A chip only	1.8V			100	mA
		3.3V (Excluding VCC3R3)			70	mA
I_{SYSTEM}	Power consumption of AX88x72A demo board	Total of 3.3V (Including VCC3R3 regulator supplies 1.8V to VCCK and VCC18A)			220	mA

Table 3 : Power consumption

9.3 Power-up Sequence

At power-up, the AX88772A/AX88172A requires the VCC3R3/VCC3IO/VCC3A3/VCC33A_H/ VCC33A_PLL power supply to rise to nominal operating voltage within Trise3 and the V18F/VCCK/VCC18A power supply to rise to nominal operating voltage within Trise2.



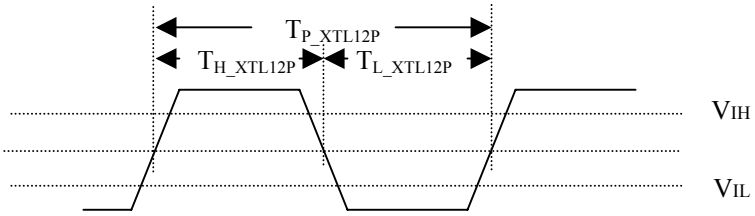
Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{rise3}	3.3V power supply rise time	From 0V to 3.3V	0.5	-	10	ms
T_{rise2}	1.8V power supply rise time	From 0V to 1.8V	-	-	10	ms
$T_{delay32}$	3.3V rise to 1.8V rise time delay		-5	-	5	ms

9.4 AC Timing Characteristics

Notice that the following AC timing specifications for output pins are based on C_L (Output load)=50pF.

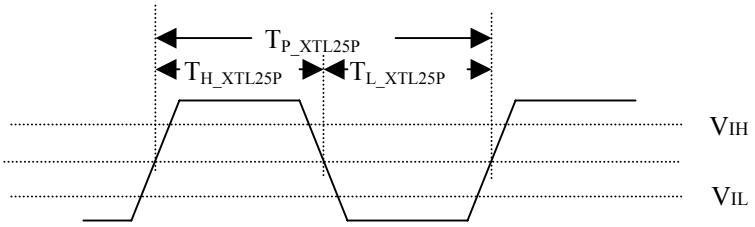
9.4.1 Clock Timing

XTL12P



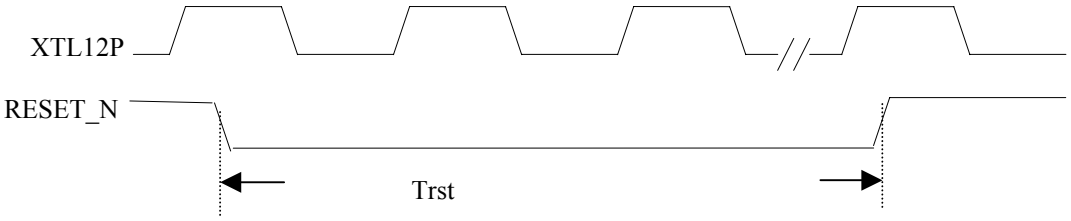
Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_XTL12P}	XTL12P clock cycle time		-	83.33	-	ns
T_{H_XTL12P}	XTL12P clock high time		-	41.6	-	ns
T_{L_XTL12P}	XTL12P clock low time		-	41.6	-	ns

XTL25P



Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_XTL25P}	XTL25P clock cycle time		-	40.0	-	ns
T_{H_XTL25P}	XTL25P clock high time		-	20.0	-	ns
T_{L_XTL25P}	XTL25P clock low time		-	20.0	-	ns

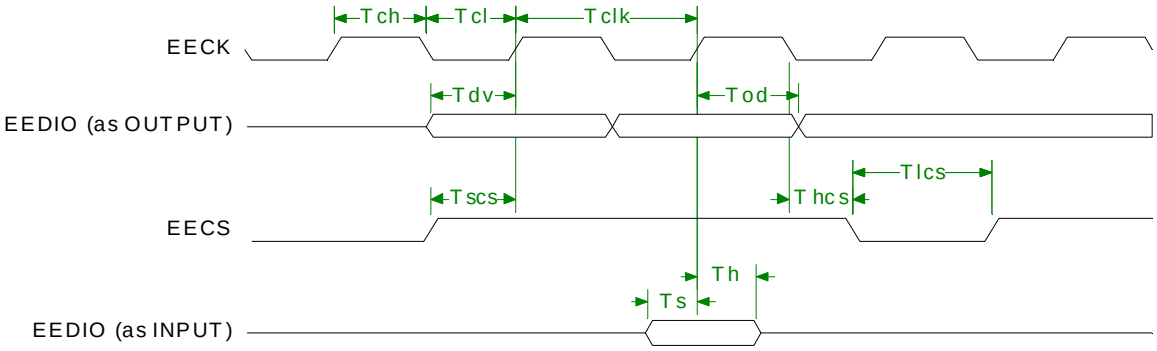
9.4.2 Reset Timing



Symbol	Description	Min	Typ	Max	Unit
Trst	Reset pulse width after XTL12P is running	60	-	120000	XTL12P clock cycle*

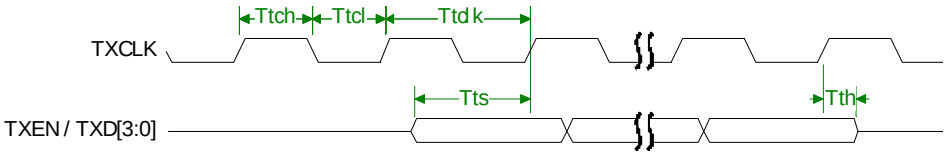
*: If the system applications require using hardware reset pin, RESET_N, to reset AX88772A/AX88172A during device initialization or normal operation after VBUS pin is asserted, the above timing spec (Min=5 μs, Max=10ms) of RESET_N should be met.

9.4.3 Serial EEPROM Timing

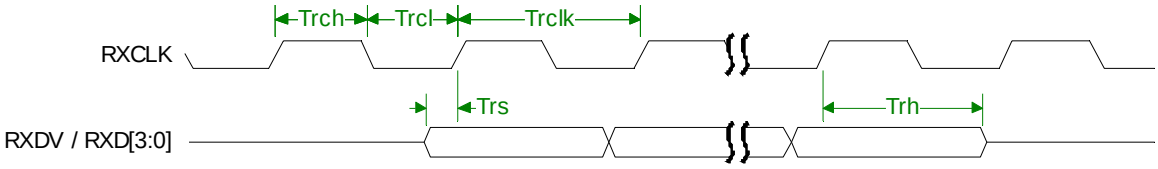


Symbol	Description	Min	Typ	Max	Unit
Tclk	EECK clock cycle time	-	5120	-	ns
Tch	EECK clock high time	-	2560	-	ns
Tcl	EECK clock low time	-	2560	-	ns
Tdv	EEDIO output valid to EECK rising edge time	2560	-	-	ns
Tod	EECK rising edge to EEDIO output delay time	2562	-	-	ns
Tscs	EECS output valid to EECK rising edge time	2560	-	-	ns
Thcs	EECK falling edge to EECS invalid time	7680	-	-	ns
Tlcs	Minimum EECS low time	23039	-	-	ns
Ts	EEDIO input setup time	20	-	-	ns
Th	EEDIO input hold time	0	-	-	ns

9.4.4 MII Timing



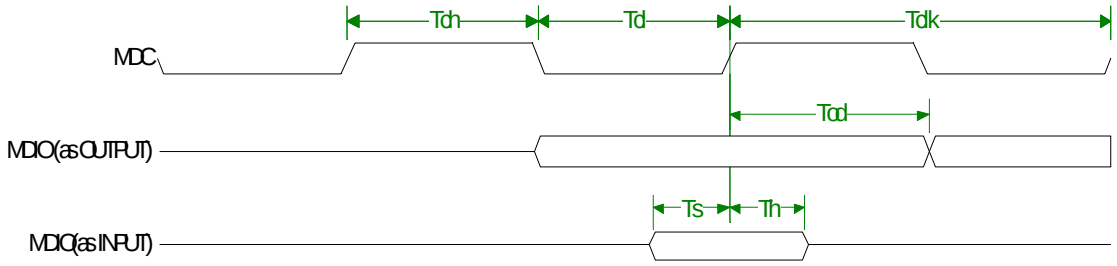
Symbol	Description	Min	Typ	Max	Unit
Ttclk	TXCLK clock cycle time *1	-	40.0	-	ns
Ttch	TXCLK clock high time *2	-	20.0	-	ns
Ttcl	TXCLK clock low time *2	-	20.0	-	ns
Tts	TXD [3:0], TXEN setup to rising TXCLK	23.0	-	-	ns
Tth	TXD [3:0], TXEN hold from rising TXCLK	7.0	-	-	ns



Symbol	Description	Min	Typ	Max	Unit
Trclk	RXCLK clock cycle time *1	-	40.0	-	ns
Trch	RXCLK clock high time *2	-	20.0	-	ns
Trcl	RXCLK clock low time *2	-	20.0	-	ns
Trs	RXD [3:0], RXDV setup to rising RXCLK	5.0	-	-	ns
Trh	RXD [3:0], RXDV hold from rising TXCLK	3.5	-	-	ns

*1: For 10Mbps, the typical value of Ttclk and Trclk shall scale to 400ns.
*2: For 10Mbps, the typical value of Ttch, Ttcl, Trch, and Trcl shall scale to 200ns.

9.4.5 Station Management Timing



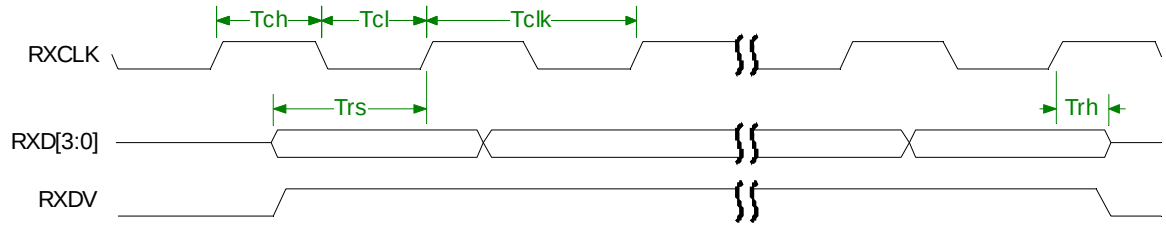
MAC mode with MII: MDC=Output

Symbol	Description	Min	Typ	Max	Unit
Tclk	MDC clock cycle time	-	640	-	ns
Tch	MDC clock high time	-	320	-	ns
Tcl	MDC clock low time	-	320	-	ns
Tod	MDC clock rising edge to MDIO output delay	0.5	-	-	Tclk
Ts	MDIO data input setup time	125	-	-	ns
Th	MDIO data input hold time	0	-	-	ns

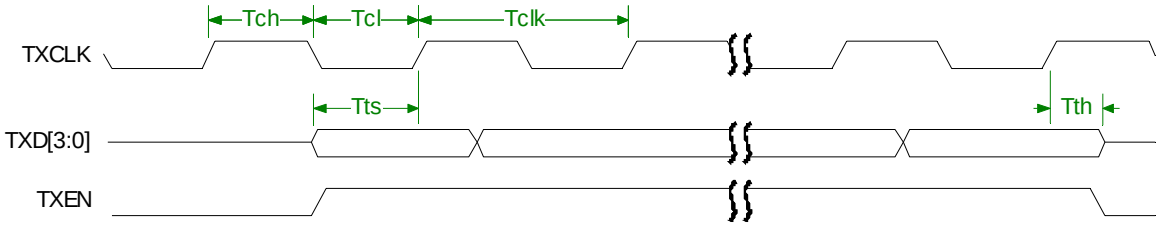
PHY/Dual-PHY mode with Reverse-MII/RMII: MDC=Input

Symbol	Description	Min	Typ	Max	Unit
Tclk	MDC clock cycle time	-	320	-	ns
Tch	MDC clock high time	-	160	-	ns
Tcl	MDC clock low time	-	160	-	ns
Tod	MDC clock rising edge to MDIO output delay	0	-	300	ns
Ts	MDIO data input setup time	10	-	-	ns
Th	MDIO data input hold time	10	-	-	ns

9.4.6 Reverse-MII Timing

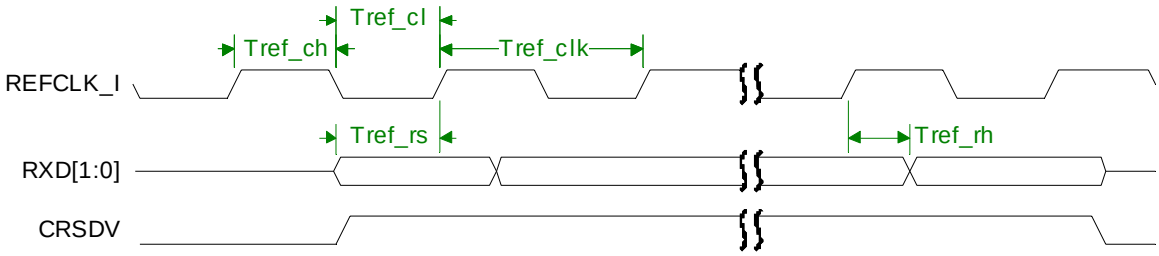


Symbol	Description	Min	Typ	Max	Unit
Tclk	Clock cycle time	-	40.0	-	ns
Tch	Clock high time	-	20.0	-	ns
Tcl	Clock low time	-	20.0	-	ns
Trs	RXD [3:0], RXDV setup to rising RXCLK	10.0	-	-	ns
Trh	RXD [3:0], RXDV hold from rising RXCLK	10.0	-	-	ns

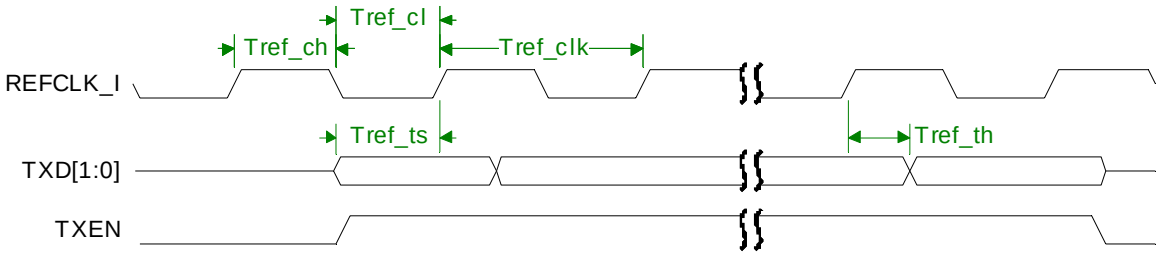


Symbol	Description	Min	Typ	Max	Unit
Tts	TXD [3:0], TXEN setup to rising TXCLK	11.0	-	-	ns
Tth	TXD [3:0], TXEN hold from rising TXCLK	2.0	-	-	ns

9.4.7 Reverse-RMII Timing

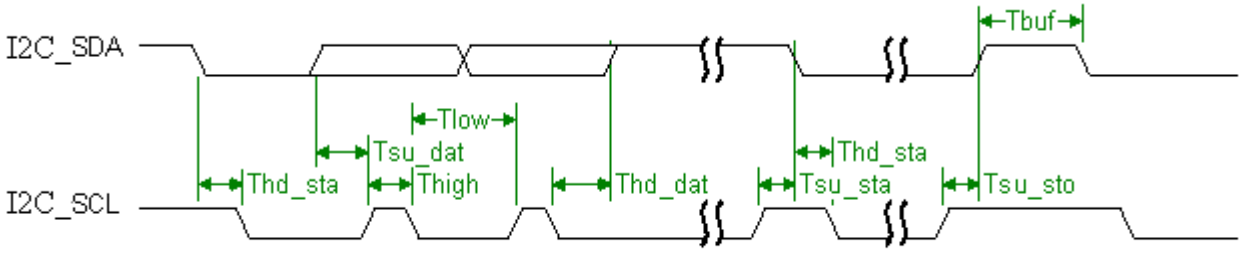


Symbol	Description	Min	Typ	Max	Unit
Tref_clk	Clock cycle time	-	20.0	-	ns
Tref_ch	Clock high time	-	10.0	-	ns
Tref_cl	Clock low time	-	10.0	-	ns
Tref_rs	RXD [1:0], CRSDV setup to rising REFCLK_I	4.0	-	-	ns
Tref_rh	RXD [1:0], CRSDV hold from rising REFCLK_I	2.0	-	-	ns



Symbol	Description	Min	Typ	Max	Unit
Tref_ts	TXD [1:0], TXEN setup to rising REFCLK_I	4.0	-	-	ns
Tref_th	TXD [1:0], TXEN hold from rising REFCLK_I	2.0	-	-	ns

9.4.8 I2C Interface Timing



I2C Master Controller Timing table:

Symbol	Parameter	Standard mode (Typ)	Fast mode (Typ)	Unit
Fclk	I2C_SCL clock frequency.	100	400	KHz
Thigh	High period of the I2C_SCL clock.	4.0	1.0	µs
Tlow	Low period of the I2C_SCL clock.	6.0	1.5	µs
Tsu_sta	Setup time for a repeated START (Sr) condition.	4.0	1.0	µs
Thd_sta	Hold time of (repeated) START (S) condition. After this period, the first clock pulse is generated	4.0	1.0	µs
Tsu_dat	Data Setup time.	2.0	0.5	µs
Thd_dat	Data Hold time.	4.0	1.0	µs
Tsu_sto	Data Setup time for STOP (P) condition.	4.0	1.0	µs
Tbuf	Bus free time between a STOP and START condition.	Note 1		

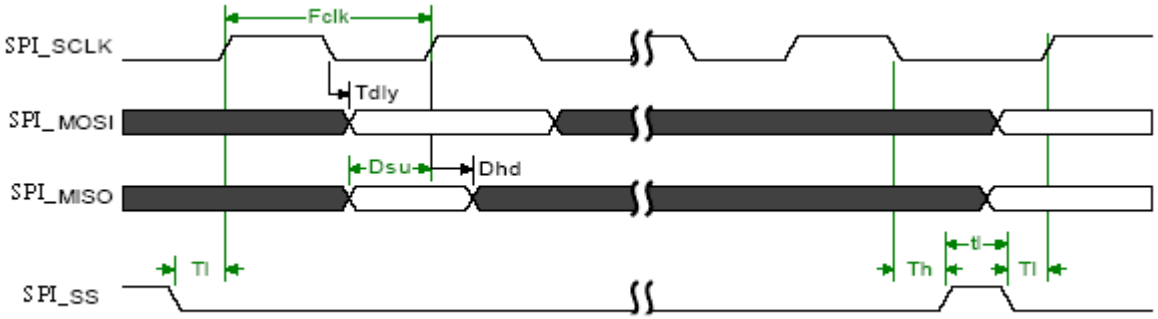
Note 1: It will be much greater than 22us because several factors can influence this parameter such as USB system utilization, the CBW structure, and High/Full speed, etc.

I2C Slave Controller Timing Table:

Symbol	Parameter	Min	Typ	Max	Unit
Fclk	I2C_SCL clock frequency.	-	-	390	KHz
Thigh	High period of the I2C_SCL clock in Fast mode.	0.6	-	-	µs
	High period of the I2C_SCL clock in Standard mode.	4.0	-	-	µs
Tlow	Low period of the I2C_SCL clock.	0.4	-	-	µs
Tsu_sta	Setup time for a repeated START (Sr) condition.	1	-	-	Tsys_clk (Note 2)
Thd_sta	Hold time of (repeated) START (S) condition. After this period, the first clock pulse is generated	3	-	-	Tsys_clk
Tsu_dat	Data Setup time.	3	-	-	Tsys_clk
Thd_dat	Data Hold time.	0.4	-	-	µs
Tsu_sto	Data Setup time for STOP (P) condition.	1	-	-	Tsys_clk
Tbuf	Bus free time between a STOP and START condition.	-	-	-	

Note 2: Tsys_clk =33.33ns for 30MHz operating system clock.

9.4.9 SPI Interface Timing

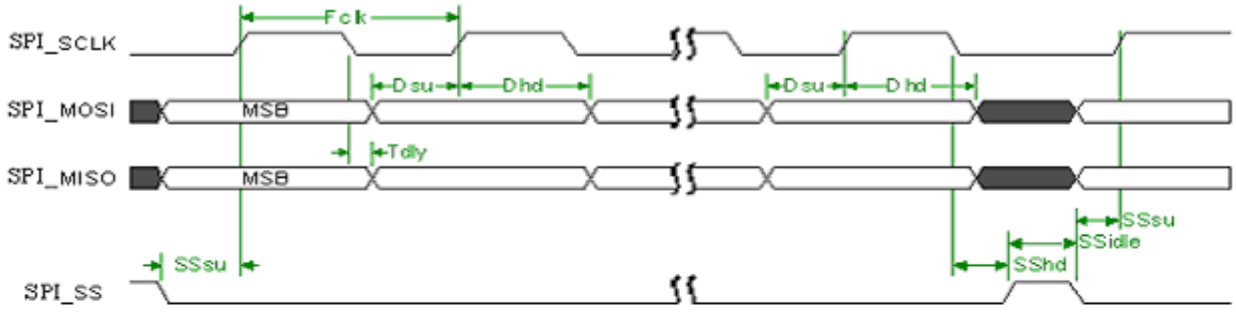


Note: Above diagram only shows setup and hold time relationship of SPI pins in Mode 0. For the remaining 3 modes, clock polarity is reversed.

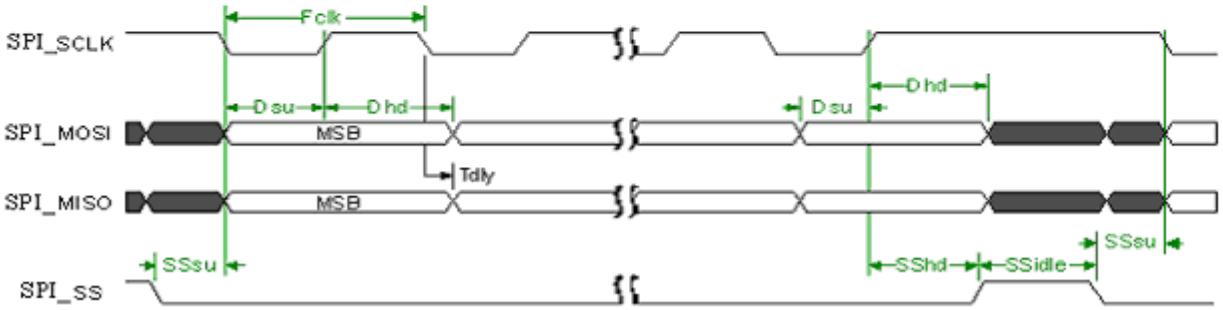
SPI Master Controller Timing Table:

Symbol	Description	Min	Typ	Max	Unit
Fclk	SPI_SCLK clock frequency.	-	Fsys_clk/ (SPIBRR+1)*2	5	MHz (Note 3)
Tl	Setup time of SPI_SS to the first SPI_SCLK edge.	-	0.5	-	Tclk (Note 3)
Th	Hold time of SPI_SS after the last SPI_SCLK edge.	-	0.5	-	Tclk
Tdly	SPI_MOSI data valid time after SPI_SCLK edge.	-	-	1	Tsys_clk (Note 4)
Dsu	SPI_MISO data setup time before SPI_SCLK edge.	2	-	-	Tsys_clk
Dhd	SPI_MISO data hold time after SPI_SCLK edge.	4	-	-	Tsys_clk
tl	Minimum idle time between transfers (minimum SPI_SS high time).	Note 5			
	Internal time base period.	-	0.5	-	Tclk

Note 3: Fsys_clk is the operating system clock frequency 30Mhz. The SPIBRR is SPI Baud Rate Register. Tclk = 1/Fclk.
Note 4: Tsys_clk =1/ Fsys_clk =33.33 ns.
Note 5: It will be much greater than 22us because several factors can influence this parameter, such as USB system utilization, the CBW structure, and High/Full speed ,etc.



SPI Slave Mode Timing Diagram in Mode 0

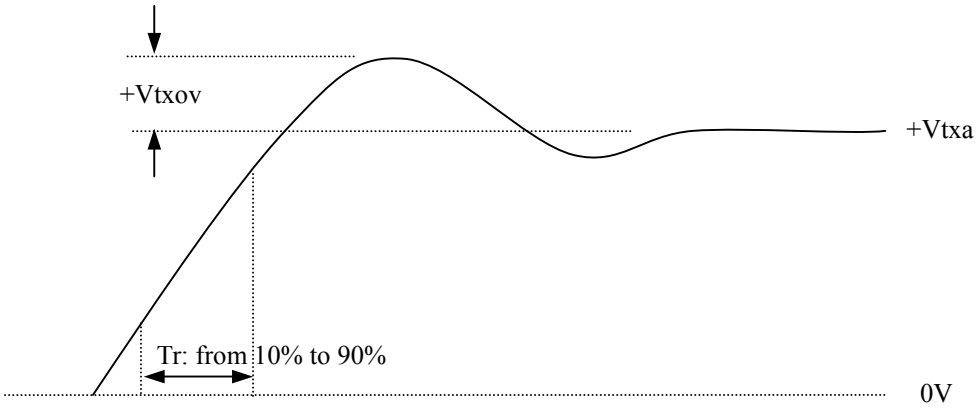


SPI Slave Mode Timing Diagram in Mode 3

SPI Slave Controller Timing Table:

Symbol	Description	Min	Typ	Max	Unit
Fclk	SPI_SCLK clock frequency.	-	-	2	MHz
Tdly	SPI_MISO data valid time after SPI_SCLK edge.	-	-	3	Tsys_clk
Dsu	SPI_MOSI data setup time before SPI_SCLK edge.	1	-	-	Tsys_clk
Dhd	SPI_MOSI data hold time after SPI_SCLK edge.	3	-	-	Tsys_clk
SSsu	SPI_SS setup time before SPI_SCLK edge.	2	-	-	Tsys_clk
SShd	SPI_SS hold time after SPI_SCLK edge.	4	-	-	Tsys_clk
SSidle	SPI_SS negation to next SPI_SS active time	2	-	-	Tsys_clk

9.4.10 10/100M Ethernet PHY Interface Timing



10/100M Ethernet PHY Transmitter Waveform and Spec:

Symbol	Description	Condition	Min	Typ	Max	Units
	Peak-to-peak differential output voltage	10BASE-T mode	4.4	5	5.6	V
Vtxa *2	Peak-to-peak differential output voltage	100BASE-TX mode	1.9	2	2.1	V
Tr / Tf	Signal rise / fall time	100BASE-TX mode	3	4	5	ns
	Output jitter	100BASE-TX mode, scrambled idle signal	-	-	1.4	ns
Vtxov	Overshoot	100BASE-TX mode	-	-	5	%

10/100M Ethernet PHY Receiver Spec:

Symbol	Description	Condition	Min	Typ	Max	Units
	Receiver input impedance		10	-	-	KΩ
	Differential squelch voltage	10BASE-T mode	300	400	500	mV
	Common mode input voltage		2.97	3.3	3.63	V
	Maximum error-free cable length		100	-	-	meter

9.4.11 USB Transceiver Interface Timing

VCC33A_H/ VCC33A_PLL= 3.0 ~ 3.6 V.

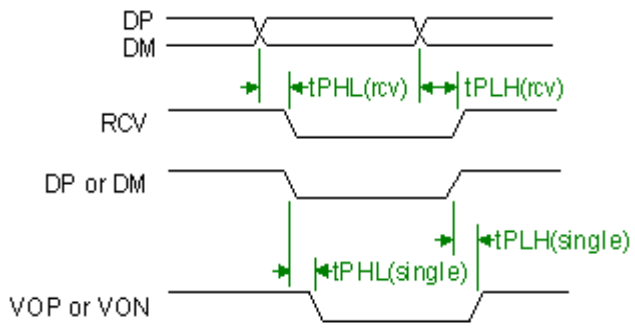
Static Characteristic for Analog I/O Pins (DP/DM):

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
USB 2.0 Transceiver (HS)						
Input Levels (Differential Receiver)						
V_{HSDIFF}	High speed differential input sensitivity	$\lvert V_{I(DP)} - V_{I(DM)} \rvert$ Measured at the connection as an application circuit.	300	-	-	mV
V_{HSCM}	High speed data signaling common mode voltage range		-50	-	500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected	-	-	100	mV
		No squelch detected	200	-	-	mV
Output levels (differential)						
V_{HSOI}	High speed idle level output voltage		-10	-	10	mV
V_{HSOL}	High speed low level output voltage		-10	-	10	mV
V_{HSOH}	High speed high level output voltage		-360	-	400	mV
V_{CHIRPJ}	Chirp-J output voltage		700	-	1100	mV
V_{CHIRPK}	Chirp-K output voltage		-900	-	-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip	40.5	45	49.5	Ohm
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0	-	3.6	V
USB 1.1 Transceiver (FS/LS)						
Input Levels (Differential Receiver)						
V_{DI}	Differential input sensitivity	$\lvert V_{I(DP)} - V_{I(DM)} \rvert$	0.2	-	-	V
V_{CM}	Differential common mode voltage		0.8	-	2.5	V
Input Levels (Single-Ended Receiver)						
V_{SE}	Single ended receiver threshold		0.8	-	2.0	V
Output levels						
V_{OL}	Low-level output voltage		0	-	0.3	V
V_{OH}	High-level output voltage		2.8	-	3.6	V

Dynamic Characteristic for Analog I/O Pins (DP/DM):

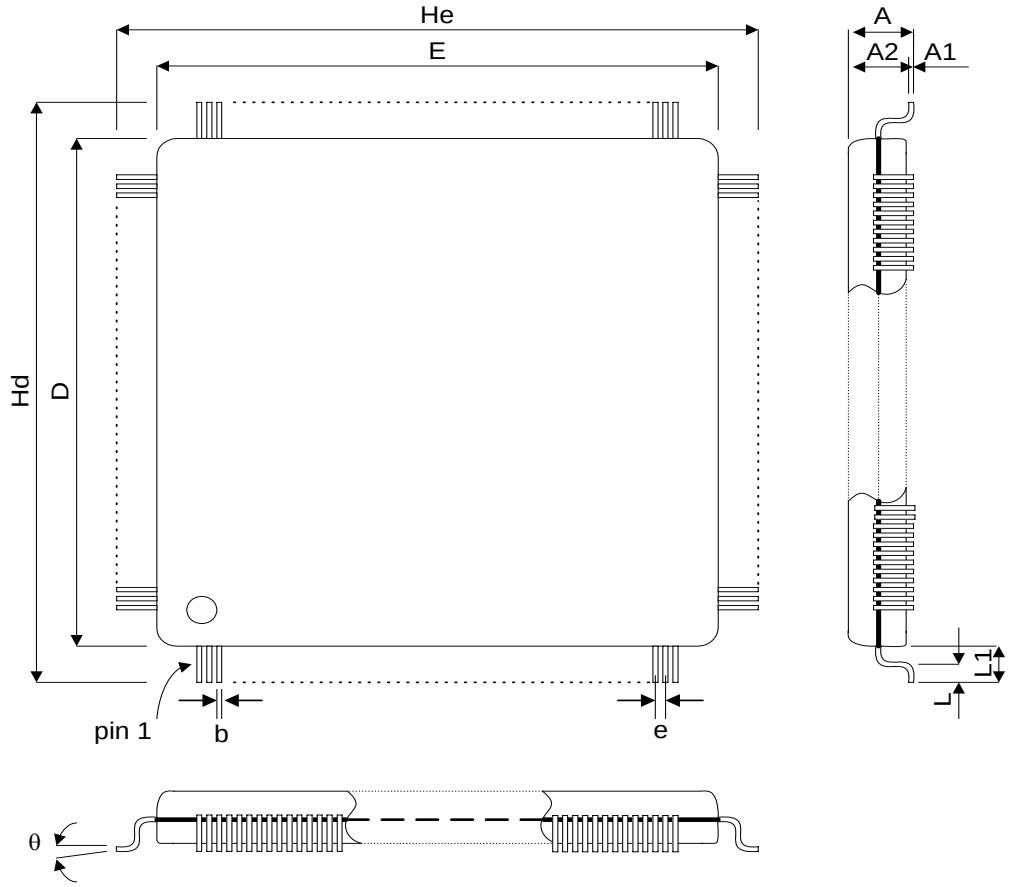
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver Characteristic						
High-Speed Mode						
t_{HSR}	High-speed differential rise time	-	500	-	-	ps
t_{HSF}	High-speed differential fall time	-	500	-	-	ps
Full-Speed Mode						
t_{FR}	Rise time of DP/DM	C_L=50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	Fall time of DP/DM	C_L=50pF; 90 to 10% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR} / t_{FF})	Excluding the first transition from idle mode	90	-	110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3	-	2.0	V
Driver Timing						
High-Speed Mode						
	Driver waveform requirement	See eye pattern of template 1	Follow template 1 described in USB rev 2.0 spec. (http://www.usb.org/developers/docs)			
Full-Speed Mode						
	VI, FSE 0, OE to DP, DN Propagation delay	For detailed description of VI, FSE 0 and OE, please refer to USB rev 1.1specification.	-	-	15	ns
Receiver Timing						
High-Speed Mode						
	Data source jitter and receiver jitter tolerance	See eye pattern of template 4	Follow template 4 described in USB rev 2.0 spec. (http://www.usb.org/developers/docs)			
Full-Speed Mode						
$t_{PLH(rcv)}$ $t_{PHL\ (rcv)}$	Receiver propagation delay (DP; DM to RCV)	For detailed description of RCV, please refer to USB rev 1.1specification.	-	-	15 (Note)	ns
$t_{PLH(single)}$ $t_{PHL(single)}$	Receiver propagation delay (DP; DM to VOP, VON)	-	-	-	15 (Note)	ns

Note: **Full-Speed Timing diagram**



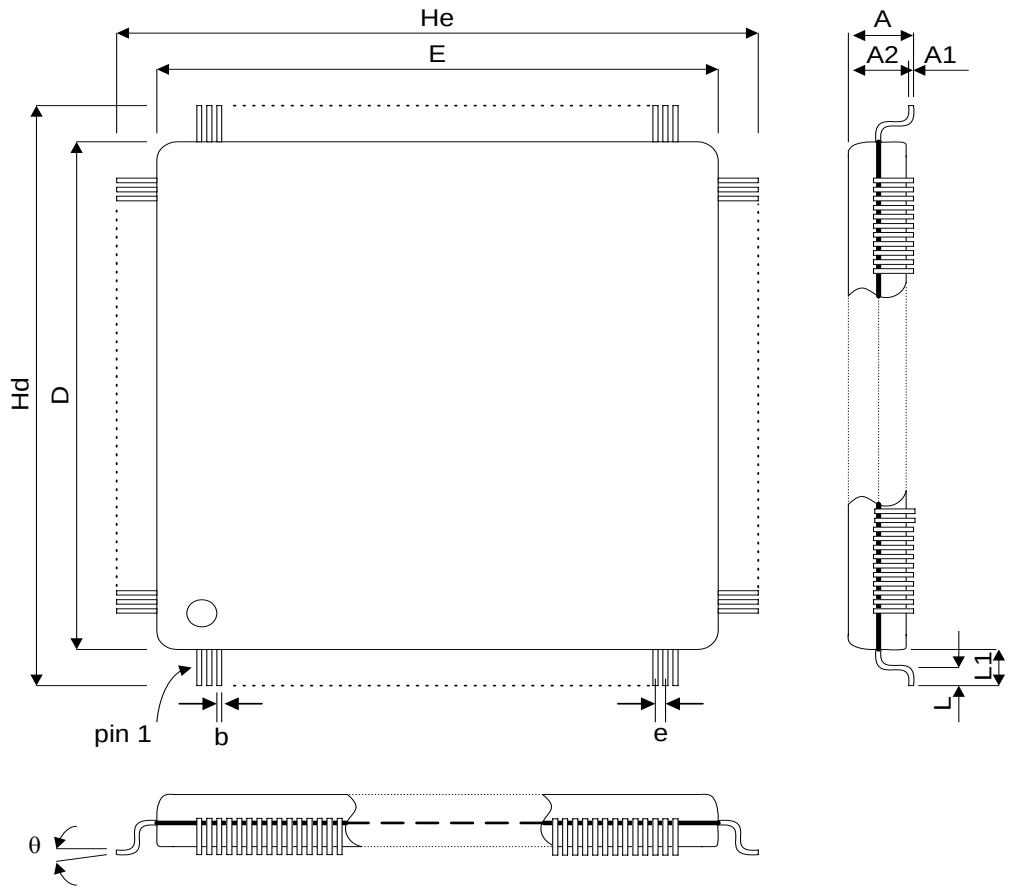
10.0 Package Information

10.1 AX88772A 64-pin LQFP package



Symbol	Millimeter		
	Min	Typ	Max
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A	-	-	1.60
b	0.13	0.18	0.23
D		7.00	
E		7.00	
e	-	0.40	-
Hd		9.00	
He		9.00	
L	0.45	0.60	0.75
L1	-	1.00 REF	-
θ	0°	3.5°	7°

10.2 AX88172A 80-pin TQFP package



Symbol	Millimeter		
	Min	Typ	Max
A1	0.05	-	0.15
A2	0.95	1.00	1.05
A	-	-	1.20
b	0.13	0.16	0.23
D		10.00	
E		10.00	
e	-	0.4 BSC	-
Hd		12.00	
He		12.00	
L	0.45	0.60	0.75
L1	-	1.00 REF	-
θ	0°	3.5°	7°

11.0 Ordering Information

Part Number	Description
AX88772ALF	AX88772A: Product Name (64 pin). L: LQFP Package. F: Lead Free.
AX88172ATF	AX88172A: Product Name (80 pin). T: TQFP Package. F: Lead Free.

12.0 Revision History

Revision	Date	Comment
V0.7	2007/8/13	Initial Release.
V1.0	2007/11/21	1. Update the power consumption information and add I_{DEVICE} and I_{SYSTEM} in Section 9.2. 2. Move the Thermal Characteristics information from Section 9.2 to Section 9.1.2 and update the Thermal Characteristics information. 3. Update the Tj junction operating temperature information in Section 9.1.2, 9.1.4, 9.1.5 and 9.1.6. 4. Update the Reset Timing information in Section 9.4.2.
V1.1	2007/12/24	1. Update some information in Section 9.1.6.

APPENDIX A. Default WOL Ready Mode

Please contact ASIX for receiving “AX88x72A Full Datasheet” which contains detailed description of Appendix A.

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