VD6725

2 megapixel, 1/5 inch system-on-chip imaging sensor

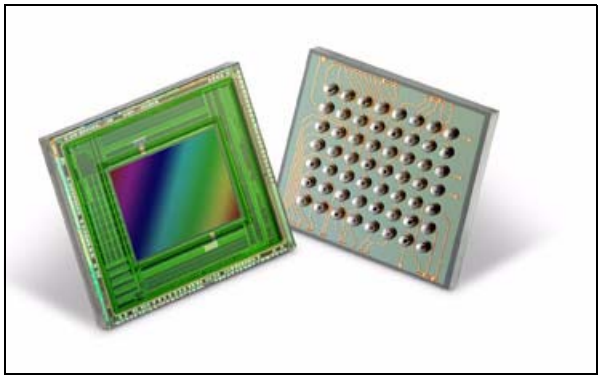
Data Brief

Features

- UXGA (2 megapixel) sensor array
- 1/5” optical format, 1.75 µm pixel size
- SNR max > 36 dB
- 10-bit continuous-time single-end ADC
- Selectable 8-bit parallel or CSI2 serial output
- Integrated high-performance image signal processor and camera controller
  - 4-channel radial anti-vignetting
  - dynamic singlet/couplet correction
  - adaptive noise reduction
  - high-quality scaler: any size scaling down from SXGA
  - electronic zoom
- 15 frames per second (fps) at full resolution, 30 fps in VGA with fast context switching feature for quicker still image capture
- Programmable I2C chip address
- Low power consumption and ultra-low standby current
- 1 Kbit OTP memory fully available to user
- Integrated 1.2 V regulator
- TSV wafer level package option

Benefits

- Compatible with camera modules with Z height below 4 mm
- Compatible with camera modules < 6 x 6 mm^2
- Flexible applications (//ITU, MIPI) using the same die
- Creative special effects
- Qualified for reflowable camera modules



Applications

- Mobile phones
- PDAs
- PC cameras and peripherals
- Gaming platforms

Description

VD6725 is an ultra-small, ultra-competitive and ultra-smart 2 megapixel 1/5” SOC imaging sensor with a high-performance image signal processor.

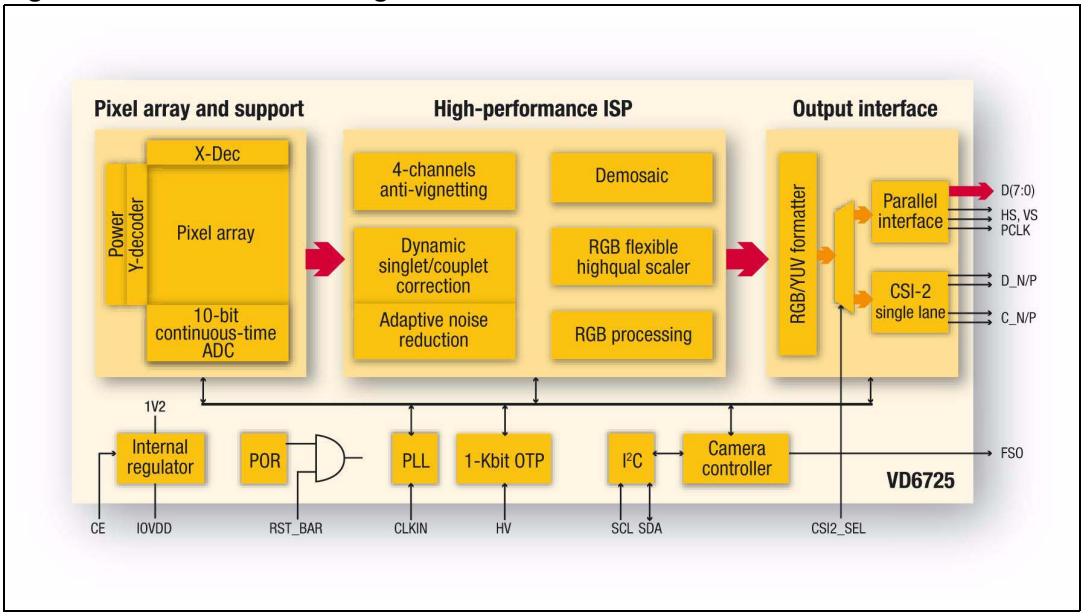
VD6725 imaging sensor allows design of ultra-low height camera modules, thanks to ST’s pixel ultra-low optical stack height that provides high quantum efficiency, better light sensitivity and improved relative illumination.

This cost competitive solution resulting from an ultra-small sensor die size is based on ST’s innovative sensor architecture and ST’s latest imaging patents, combined to our new imaging process.

ST’s new high performance imaging process provides 1.75 µm pixel size, very high logic density, excellent SNR and low light performance. It is qualified in our 8” and 12” world-leading manufacturing infrastructures.

1 Overview

Figure 1. VD6725 block diagram



Wafer level package: TSV (through-silicon via)

The wafer-level package, TSV (through-silicon via) technology, is used to design smaller camera modules, improve the assembly yield and lower costs. The VD6725 is available in ST's revolutionary TSV package:

- Ultra-scaled down camera module size
- No wire bonding inside the camera module: save up to 1.6 mm in X and Y
- No substrate in the module: directly reflowable, on phone mother board or flex-attach
- Up to 400 µm saved in module Z height
- No leads on the package sides for an increased reliability and ESD protection

2 Ordering information

Table 1. Ordering information

Order code	Description
VD6725/SW	Tested, sawn dice on reconstructed wafer.

3 Revision history

Table 2. Document revision history

Date	Revision	Changes
25-Jan-2008	1	Initial release.
31-Jan-2008	2	Clarified the feature on OTP memory in the *Features*.

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