8-Channel, Ultra-Low Power Variable Gain Amplifier with Low-Noise Pre-Amp

FEATURES

- **Ultra-low Power: 63mW/Channel**
- **Low Noise: 0.8nV/√Hz**
- **Low-Noise Pre-amp (LNP):**
  - **20dB Fixed Gain**
  - **250mV$_{PP}$ Linear Input Range**
- **Variable Gain Amplifier:**
  - **Gain Control Range: 45dB**
  - **Selectable PGA Gain: 20dB, 25dB, 27dB, 30dB**
  - **Fast Overload Recovery**
  - **Output Clamping Control**
- **Integrated Low-Pass Filter:**
  - **Second-Order, Linear Phase**
  - **Bandwidth: 10MHz, 15MHz**
- **High Accuracy:**
  - **Low Gain Error: ±0.25 dB**
  - **Excellent Channel Matching: ±0.5dB**
- **Distortion, HD2: –50dBc at 5MHz**
- **Integrated CW Switch Matrix:**
  - **Easy Current Summing**
- **Serial Control Interface**
- **Small Package: QFN-64, 9×9 mm**

APPLICATIONS

- **Medical Imaging, Ultrasound Systems**
  - **Portable Systems**
  - **Low-, Mid-Range Systems**

DESCRIPTION

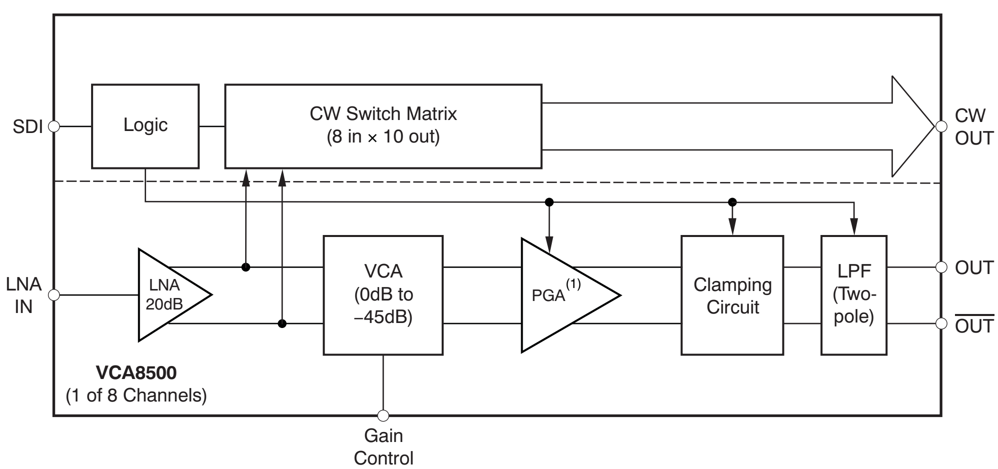
The VCA8500 is an 8-channel variable gain amplifier consisting of a Low-Noise Pre-amplifier (LNP) and a Variable-Gain Amplifier (VGA). This combination, along with the device features, makes it ideal for a variety of ultrasound systems.

The LNP gain is fixed at 20dB, and has excellent noise and signal handling characteristics. The gain of the voltage-controlled attenuator can vary over a 45-dB range with a 0V to 1.2V control voltage common to all channels of the VCA8500.

The Post-Gain Amplifier (PGA) can be programmed for four gain settings: 20dB, 25dB, 27dB, or 30dB gain. As a means to improve system overload recovery time, the VCA8500 provides an internal clamping function. The PGA settings as well the clamp levels are controlled through the serial interface.

The VCA8500 is built on TI's BiCOM process and is available in a small, 64-pin QFN PowerPAD™ package.

PRODUCT PREVIEW



NOTE (1): 20dB, 25dB, 27dB, or 30dB gain setting.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY	ECO STATUS(2)
VCA8500	QFN-64	RGC	–40°C to +85°C	VCA8500	Tape and Reel, 250	Pb-Free, Green
					Tape and Reel, 2500	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) **Eco-Status information:** Additional details including specific material content can be accessed at www.ti.com/leadfree
GREEN: Ti defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1% of total product weight.
N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go towww.ti.com/leadfree.
Pb-FREE: Ti defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

NOTE

These packages conform to Lead-Free and Green Manufacturing Specifications.

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ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	VCA8500	UNIT
Input voltage range(2)	–0.3 to AVDD to +0.3	V
	–0.3 to AVDD to +0.3	V
	–0.3 to DVDD to +0.3	V
Voltage range at (tbd)	TBD	V
Voltage on outputs	–0.3 to AVDD to +0.3	V
	–0.3 to DVDD to +0.3	V
Peak output current	Internally limited	
ESD rating, HBM	2k	V
ESD rating, CDM	500	V
Operating virtual junction temperature range, T_J	–40 to +150	°C
Operating ambient temperature range, T_A	–40 to +85	°C
Storage temperature range, T_{stg}	–65 to +150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (≤ 1μF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, VCA output is $2V_{PP}$ differential, R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VCA8500 MIN	VCA8500 TYP	VCA8500 MAX	UNIT	TEST LEVEL (1)
PREAMPLIFIER (LNA)							
	LNA gain	Single-ended input to differential output		20		dB	
	Accuracy			±0.5		dB	
Z_{IN}	Input resistance	At f = 4MHz		8		kΩ	
C_{IN}	Input capacitance	Including internal ESD and clamping diodes		30	35	pF	
V_{IN}	Input voltage	Linear operation (THD ≤ –40dBc)		250		mV_{PP}	
	Maximum input voltage (2)	Internal diode limited		600		mV_{PP}	
e_N, RTI	Input voltage noise	At f = 2MHz (calculated)		0.75		$nV/\sqrt{Hz}$	
I_N, RTI	Input current noise	At f = 2MHz		3.0		$pA/\sqrt{Hz}$	
V_{CMI}	Common-mode voltage, inputs	Internally generated		2.4		V	
BW	Bandwidth	Small-signal, –3dB		70		MHz	
SR	Slew rate			TBD		V/μs	
TGC SIGNAL PATH (LNA, VCA, PGA)							
e_N, RTI	Input voltage noise	PGA = 30dB, R_S = 0Ω, f = 2MHz		0.8		$nV/\sqrt{Hz}$	
		PGA = 20dB		0.9		$nV/\sqrt{Hz}$	
Z_{OUT}	Output impedance	dc to 10MHz, Single-Ended, Either Output		<1		Ω	
I_{OUT-SC}	Output short-circuit current			TBD		mA	
	Overload distortion (second-harmonic)	V_{IN} = $250mV_{PP}$	–40	< –35		dBc	
	Crosstalk, channel-to-channel	Worst case; Gain = TBDdB	TBD	–55		dBc	
		Gain = max (50dB)		–50		dBc	
NF	Noise figure	R_S = R_{IN} = 50Ω (TBDdB max gain)		TBD		dB	
	Group delay variation	1MHz to TBDMHz, full gain range		±2	±3	ns	
	Delay matching	Between channels		TBD		ns	
	Overload recovery time	To within 1% of $2V_{PP}$ output at 40dB gain (V_{CNTL} = TBDV + 30dB PGA)		1		μs	
C_L	Maximum capacitive output loading	50Ω series R in each output		TBD		pF	
V_{OUT}	Output voltage range (2)	Differential, non-clipped		2		V_{PP}	
V_{CMO}	Output common-mode voltage			1.65		V_{DC}	
HD2	Second-harmonic distortion	f_{IN} = 5MHz, V_{CNTL} = TBDV; Gain = TBD, V_{OUT} = $1V_{PP}$	–50	TBD		dBc	
		f_{IN} = 5MHz, V_{CNTL} = TBDV; Max gain, V_{OUT} = $2V_{PP}$	–42	–50		dBc	
HD3	Third-harmonic distortion	f_{IN} = 5MHz, V_{CNTL} = TBDV; Gain = TBD, V_{OUT} = $1V_{PP}$	–48	TBD		dBc	
		f_{IN} = 5MHz, V_{CNTL} = TBDV; Max gain, V_{OUT} = $2V_{PP}$	–40	–48		dBc	
IMD3	Two-tone intermodulation	f_1 = TBDMHz, f_2 = TBDMHz, V_{CNTL} = TBDV; V_{OUT} = $1V_{PP}$		–40		dBc	

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Second, third-harmonic distortion less than or equal to −TBDdB.

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ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (≤ 1μF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, VCA output is $2V_{PP}$ differential, R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VCA8500 MIN	VCA8500 TYP	VCA8500 MAX	UNIT	TEST LEVEL[1]
CW SIGNAL PATH							
	Output transconductance (V/I)			15		mA/V	
I_{OUT-CW}	Dynamic CW output current	Signal current		2.4 (±1.2)		mA_{PP}	
I_{OUT-DC}	Static CW output current			0.9		mA	
V_{CMO}	Output common-mode voltage			2.5		V_{DC}	
V_{Cout}	Output compliance range	Symmetric around V_{CMO}	TBD	±0.5	TBD	V	
C_{OUT}	Output capacitance			< 10		pF	
Z_{OUT}	Output impedance			50		kΩ	
THD_{CW}	Harmonic distortion	HD2		TBD		dBc	
		HD3		TBD		dBc	
e_N, RTI	Input voltage noise, CW mode	At f = 2MHz		1.1		nV/√Hz	
	Signal-dependent noise (RTO)	At 2kHz offset from 2MHz CW carrier		+2		dB	
		At 2kHz offset from 5MHz CW carrier		+2		dB	
	Output noise correlation factor	Summing of eight channels [compared to ideal 0dB (SNR)]		0.6		dB	
FILTER							
LPF	Low-pass filter (second-order)	–3dB point, V_{CNTL} = 1.2V		10		MHz	
	Tolerance			±10	±15	%	
	Group delay (variation)			TBD		ns	
	Gain flatness	–1dB point		TBD		MHz	
HPF	High-pass filter (first-order, due to internal ac coupling)	–3dB point, V_{CNTL} = 1.2V		150		kHz	
ACCURACY							
	Gain error (VCA)(3)	V_{CNTL} = 0V to 1.2V		±0.25	±0.5	dB	
	Gain range	V_{CNTL} = 0V to 1.2V	TBD	45	TBD	dB	
	Gain slope	V_{CNTL} = 0V to 1.2V		37.5		dB/V	
	Gain matching, channel-to-channel	V_{CNTL} = 0V to 1.2V		±0.5	±1.5	dB	
	Gain, PGA	Selectable through SDI		20, 25, 27, 30		dB	
V_{OS}	Output offset voltage						
	Differential		–25	±5	+25	mV	
	Common-mode		–50	±25	+50	mV	
GAIN CONTROL INTERFACE							
V_{CNTL}	Input voltage range	Gain range = 45dB		0 to 1.2		V	
	Input resistance			25		kΩ	
	Response time			0.75		μs	
	Gain control bandwidth	V_{CNTL}= 0V to 1.2V step; to 90% Signal Level		1.5		MHz	
DIGITAL INPUTS (SDI)(4)(5)		(PD, DIN, DOUT, CLK, RST)					
V_{IH}	V_{IH}, High-level input voltage		2.0		VD	V	
V_{IL}	V_{IL}, Low-level input voltage		0		0.8	V	
I_{IN}	Input current			±10		μA	
f_{CLK}	Clock frequency		10k		20M	Hz	
	Input resistance			1		MΩ	
	Input capacitance			5		pF	

(3) Compared to a standard curve. This is also Gain Error vs $V_{CONTROL}$.
(4) Parameters ensured by design; not production tested.
(5) Internal pull-up/pull-down resistors.

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ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, AVDD2 = 5.0V, AVDD1 = DVDD = 3.3V; single-ended, ac-coupled (≤ 1µF) input configuration to the preamp (LNA), f_{IN} = 5MHz, V_{CNTL} = 1.0V, VCA output is $2V_{PP}$ differential, R_{LOAD} = 1kΩ on each output to ground, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VCA8500 MIN	VCA8500 TYP	VCA8500 MAX	UNIT	TEST LEVEL(1)
POWER SUPPLY							
AVDD1	Analog aupply voltage	Specified	3.14	3.3	3.47	V	
		Operating	3.0	3.3	3.6	V	
DVDD	Digital supply voltage	Specified	3.14	3.3	3.47	V	
		Operating	3.0	3.3	3.6	V	
	AVDD1 + DVDD quiescent current			TBD		mA	
AVDD2	Analog supply voltage (VCA, CW)		4.75	5.0	5.25	V	
	AVDD2 quiescent current			8		mA	
I_Q	Total quiescent current	All channels, no signal		148		mA	
P_{Dtot}	Total power dissipation	TGC-mode		504	TBD	mW	
		CW-mode		450		mW	
PDT	Power-down dissipation, total	PD to Valid output (90% level)		5	10	mW	
I_{PD}	Total power-down current			1.5		mA	
	Power-up response time			50		µs	
	Power-down response time			10		µs	
PDF	Power-down dissipation, fast-mode	Power-down and power-up; PD to Valid output (90% level)		18		mW	
	Power-down, fast-mode			TBD	5	µs	
PSRR	Power-supply ripple rejection	Gain < max (TBD), f < 10kHz		TBD		dB	
THERMAL CHARACTERISTICS							
	Temperature range	Ambient, operating	–40		+85	°C	
	Thermal resistance, θ_{JA}	Soldered pad; four-layer PCB with thermal vias		22.5		°C/W	
	Thermal resistance, θ_{JC}			17.0		°C/W	

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DEVICE INFORMATION

RGC PACKAGE
QFN-64
(TOP VIEW)

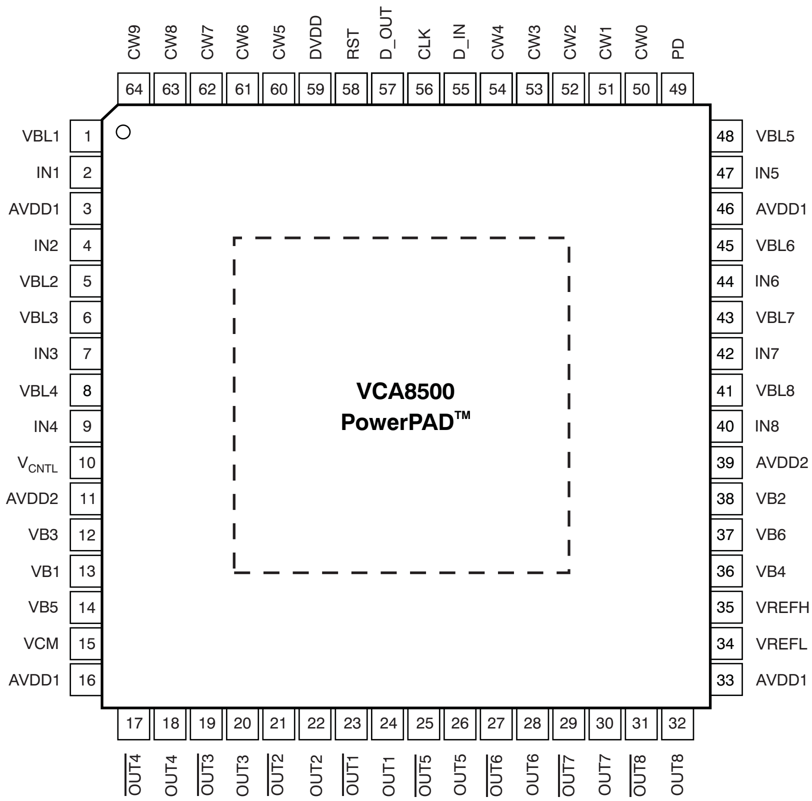

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Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
PIN NO.	NAME		
1	VBL1		Internal bias voltage; bypass with 0.1µF (min)
2	IN1	I	LNA input channel 1
3	AVDD1		+3.3V analog supply
4	IN2	I	LNA input channel 2
5	VBL2		Internal bias voltage; bypass with 0.1µF (min)
6	VBL3		Internal bias voltage; bypass with 0.1µF (min)
7	IN3	I	LNA input channel 3
8	VBL4		Internal bias voltage; bypass with 0.1µF (min)
9	IN4		LNA input channel 4
10	VCNTL	I	Attenuator control voltage input (all channels)
11	AVDD2		+5V Analog supply (VCA, CW)
12	VB3		Internal bias voltage; bypass with 0.1µF (min)
13	VB1		Internal bias voltage; bypass with 2.2µF (1.0µF min)
14	VB5		Internal bias voltage; bypass with 0.1µF (min)
15	VCM		Internal common-mode voltage; bypass with 0.1µF (min)
16	AVDD1		+3.3V analog supply
17	$\overline{\text{OUT4}}$	O	PGA output channel 4 (inverted)
18	OUT4	O	PGA output channel 4
19	$\overline{\text{OUT3}}$	O	PGA output channel 3 (inverted)
20	OUT3	O	PGA output channel 3

Table 1. TERMINAL FUNCTIONS (continued)

TERMINAL			
PIN NO.	NAME	I/O	DESCRIPTION
21	$\overline{\text{OUT2}}$	O	PGA output channel 2 (inverted)
22	OUT2	O	PGA output channel 2
23	$\overline{\text{OUT1}}$	O	PGA output channel 1 (inverted)
24	OUT1	O	PGA output channel 1
25	$\overline{\text{OUT5}}$	O	PGA output channel 5 (inverted)
26	OUT5	O	PGA output channel 5
27	$\overline{\text{OUT6}}$	O	PGA output channel 6 (inverted)
28	OUT6	O	PGA output channel 6
29	$\overline{\text{OUT7}}$	O	PGA output channel 7 (inverted)
30	OUT7	O	PGA output channel 7
31	$\overline{\text{OUT8}}$	O	PGA output channel 8 (inverted)
32	OUT8	O	PGA output channel 8
33	AVDD1		+3.3V analog supply
34	VREFL		Clamp level low, 2.0V; bypass with 0.1µF (min)
35	VREFH		Clamp level high, 2.7V; bypass with 0.1µF (min)
36	VB4		Internal bias voltage; bypass with 0.1µF (min)
37	VB6		Internal bias voltage; bypass with 0.1µF (min)
38	VB2		Internal bias voltage; bypass with 0.1µF (min)
39	AVDD2		+5V analog supply (VCA, CW)
40	IN8	I	LNA input channel 8
41	VBL8		Internal bias voltage; bypass with 0.1µF (min)
42	IN7	I	LNA input channel 7
43	VBL7		Internal bias voltage; bypass with 0.1µF (min)
44	IN6	I	LNA input channel 6
45	VBL6		Internal bias voltage; bypass with 0.1µF (min)
46	AVDD1		+3.3V analog supply
47	IN5	I	LNA input channel 5
48	VBL5		Internal bias voltage; bypass with 0.1µF (min)
49	PD	I	Power-down pin for fast mode; active high
50	CW0	O	CW channel 0 current output
51	CW1	O	CW channel 1 current output
52	CW2	O	CW channel 2 current output
53	CW3	O	CW channel 3 current output
54	CW4	O	CW channel 4 current output
55	D_IN	I	Serial data input
56	CLK	I	Clock input for serial interface
57	D_OUT	O	Serial data output
58	RST	I	Reset input; rising edge resets register to default values.
59	DVDD		+3.3V Digital supply; connect to analog supply plane (AVDD1)
60	CW5		CW channel 5 current output
61	CW6		CW channel 6 current output
62	CW7		CW channel 7 current output
63	CW8		CW channel 8 current output
64	CW9		CW channel 9 current output
—	GND		PowerPAD must be connected to the analog ground of the printed circuit board; use this ground for bypass cap return ground.

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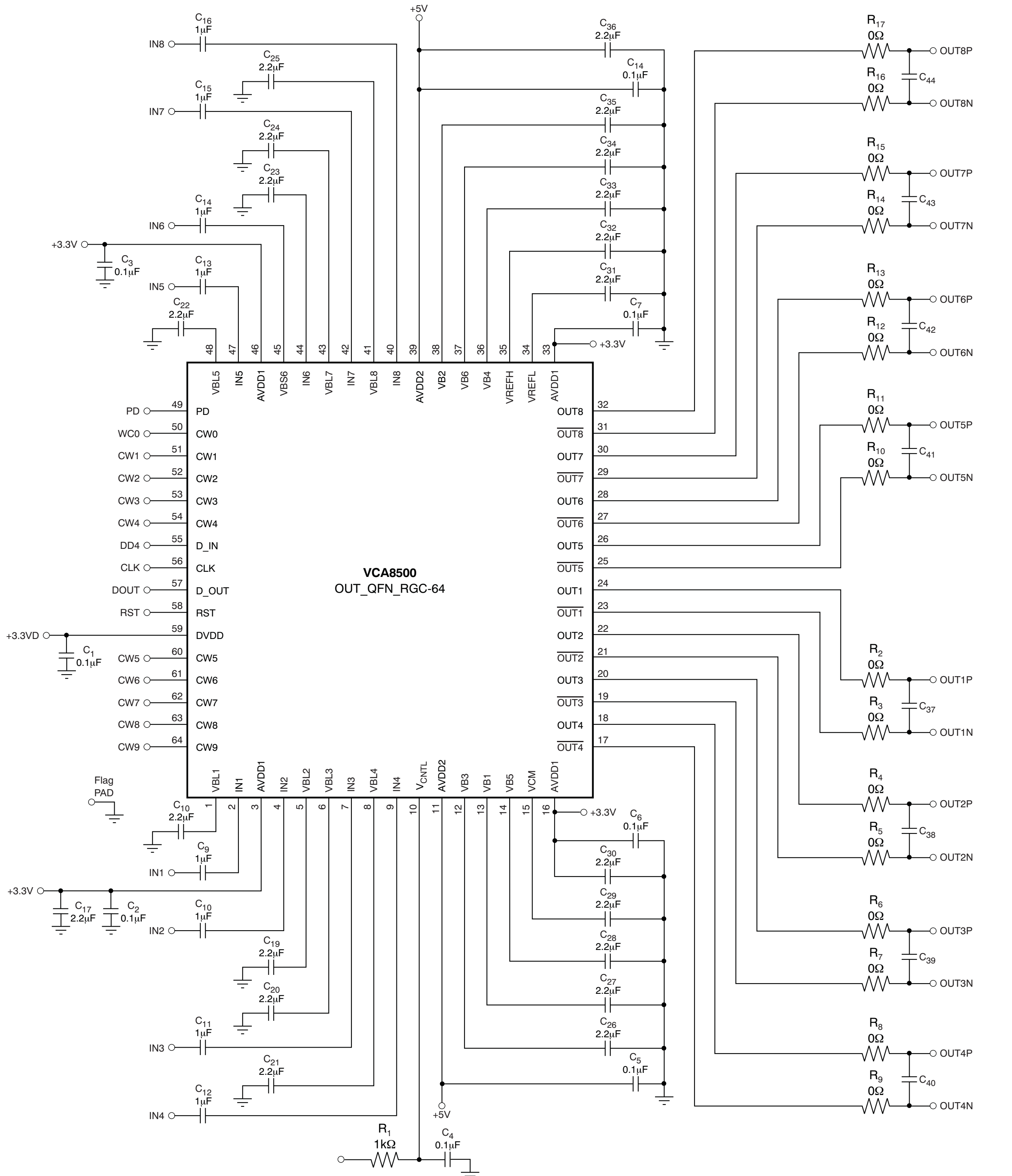
TYPICAL CONNECTION DIAGRAM



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NOTES:

(1) $V_{CONTROL}$: Values for R_1 and C_4 should be selected for a desired time constant.

(2) Outputs: Values for R_2 – R_{17} and C_{37} – C_{44} should be selected based on the analog-to-digital converter selected.

(3) The +3.3V supply connections for DVDD and AVDD1 should be joined to a low-noise +3.3V system supply. Consider filtering any supply noise with an LC filter.

INPUT REGISTER BIT MAPS

Register Map

BYTE #1	BYTE #2		BYTE #3		BYTE #4		BYTE #5	
D0:D7	D8:D11	D12:D15	D16:D19	D20:D23	D24:D27	D28:D31	D32:D35	D36:D39
Control	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8

Table 2. Byte 1—Control Byte Register Map

BIT #	NAME	DESCRIPTION
D0 (LSB)	1	Start bit; must be a '1' (high); 40-bit countdown starts with first falling clock edge.
D1	R/$\overline{W}$	1 = Write, 0 = Read; Read prevents latching of new data/bits. Control register remains latched with previously loaded data.
D2	PWR	1 = Power-down mode enabled.
D3	BW	Low-pass filter bandwidth setting (see Table 7)
D4	CL	Clamp level setting (see Table 7)
D5	Mode	1 = TGC Mode, 0 = CW Doppler Mode (TGC powered down)
D6	PG0	LSB of PGA Gain Control (see Table 8)
D7 (MSB)	PG1	MSB of PGA Gain Control

Table 3. Byte 2—First Data Byte

BIT #	NAME	DESCRIPTION
D8 (LSB)	DB1:1	Channel 1; LSB of Matrix Control
D9	DB1:2	Channel 1, Matrix Control
D10	DB1:3	Channel 1, Matrix Control
D11	DB1:4	Channel 1, MSB of Matrix Control
D12	DB2:1	Channel 2; LSB of Matrix Control
D13	DB2:2	Channel 2, Matrix Control
D14	DB2:3	Channel 2, Matrix Control
D15 (MSB)	DB2:4	Channel 2, MSB of Matrix Control

Table 4. Byte 3—Second Data Byte

BIT #	NAME	DESCRIPTION
D16 (LSB)	DB3:1	Channel 3; LSB of Matrix Control
D17	DB3:2	Channel 3, Matrix Control
D18	DB3:3	Channel 3, Matrix Control
D19	DB3:4	Channel 3, MSB of Matrix Control
D20	DB4:1	Channel 4; LSB of Matrix Control
D21	DB4:2	Channel 4, Matrix Control
D22	DB4:3	Channel 4, Matrix Control
D23 (MSB)	DB4:4	Channel 4, MSB of Matrix Control

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Table 5. Byte 4—Third Data Byte

BIT #	NAME	DESCRIPTION
D24 (LSB)	DB5:1	Channel 5; LSB of Matrix Control
D25	DB5:2	Channel 5, Matrix Control
D26	DB5:3	Channel 5, Matrix Control
D27	DB5:4	Channel 5, MSB of Matrix Control
D28	DB6:1	Channel 6; LSB of Matrix Control
D29	DB6:2	Channel 6, Matrix Control
D30	DB6:3	Channel 6, Matrix Control
D31 (MSB)	DB6:4	Channel 6, MSB of Matrix Control

Table 6. Byte 5—Fourth Data Byte

BIT #	NAME	DESCRIPTION
D32 (LSB)	DB7:1	Channel 7; LSB of Matrix Control
D33	DB7:2	Channel 7, Matrix Control
D34	DB7:3	Channel 7, Matrix Control
D35	DB7:4	Channel 7, MSB of Matrix Control
D36	DB8:1	Channel 8; LSB of Matrix Control
D37	DB8:2	Channel 8, Matrix Control
D38	DB8:3	Channel 8, Matrix Control
D39 (MSB)	DB8:4	Channel 8, MSB of Matrix Control

Table 7. Clamp Level and LPF Bandwidth Setting

NAME	SETTING	FUNCTION
BW	D3 = 0	Bandwidth set to 10 MHz
	D3 = 1	Bandwidth set to 15 MHz
CL	D4 = 0	Clamps the output signal at 2 dB below the full-scale of 2 V_{PP} (1.6 V_{PP}) on each PGA output channel
	D4 = 1	Clamp transparent (disabled)

Table 8. PGA Gain Setting

PG1	PG0	FUNCTION
0	0	Set PGA gain to 20dB
0	1	Set PGA gain to 25dB
1	0	Set PGA gain to 27dB
1	1	Set PGA gain to 30dB

Table 9. CW Switch Matrix Control for Each Channel

DBn:4 (MSB)	DBn:3	DBn:2	DBn:1 (LSB)	LNA Input Channel Directed To:
0	0	0	0	Output CW0
0	0	0	1	Output CW1
0	0	1	0	Output CW2
0	0	1	1	Output CW3
0	1	0	0	Output CW4
0	1	0	1	Output CW5
0	1	1	0	Output CW6
0	1	1	1	Output CW7
1	0	0	0	Output CW8
1	0	0	1	Output CW9
1	0	1	0	Connected to AVDD1
1	0	1	1	Connected to AVDD1
1	1	0	0	Connected to AVDD1
1	1	0	1	Connected to AVDD1
1	1	1	0	Connected to AVDD1
1	1	1	1	Connected to AVDD1

Table 10 shows the default register configuration at device power-up, or after a reset cycle.

Table 10. Default Register Configuration

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	1	1

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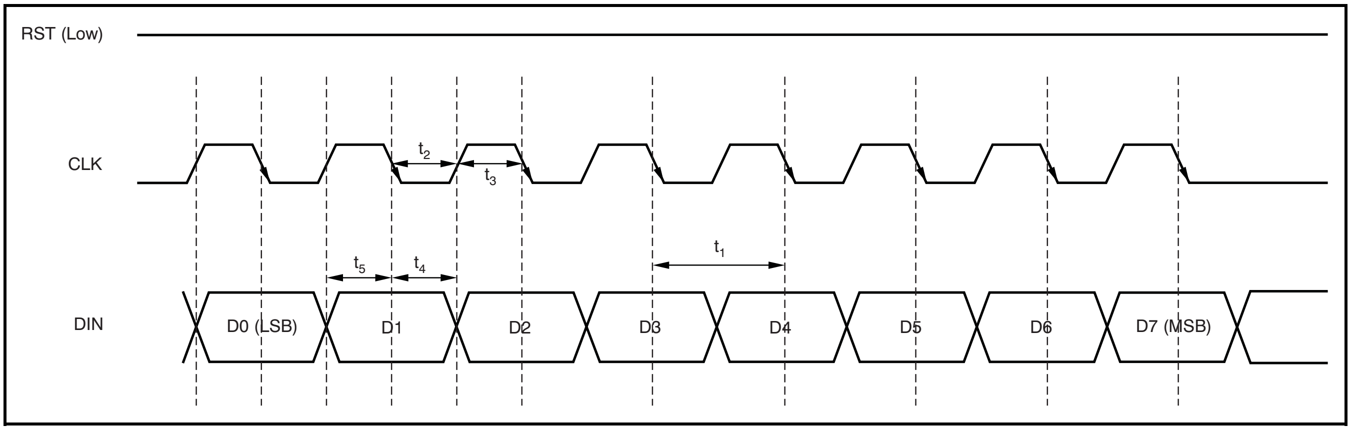
WRITE/READ TIMING

- All writes and reads are five bytes at a time. Each byte consists of 8 bits, for a total instruction set of 40 bits.
- Data are latched on the falling edge of CLK.
- Separate write (DIN) and read data (DOUT) lines.
- Reads follow the same bitstream pattern seen in the write cycle.
- Reads extract data from the FIFO buffer, not the latched register.
- DOUT data are continuously available and do not need to be enabled with a read cycle. Selecting a read cycle in the control register only prevents latching of data. The control register remains latched.
- The Reset pin (RS) must be low in order to allow the register to update with new data. RST can be held low permanently. To initiate a reset cycle, pull the RST pin high for at least 100ns.

WRITE CYCLE TIMING



NOTE: Figure shows timing example for one data byte. A full register update cycle requires all five bytes (that is, 40 bits).

SERIAL PORT TIMING TABLE

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	Serial CLK Period	100			ns
t_2	Serial CLK HIGH Time	40			ns
t_3	Serial CLK LOW Time	40			ns
t_4	Data Hold Time	5			ns
t_5	Data Setup Time	5			ns
	Reset Pulse (L - H - L)	100			ns

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
VCA8500IRGCR	PREVIEW	QFN	RGC	64	2000	TBD	Call TI	Call TI
VCA8500IRGCT	PREVIEW	QFN	RGC	64	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

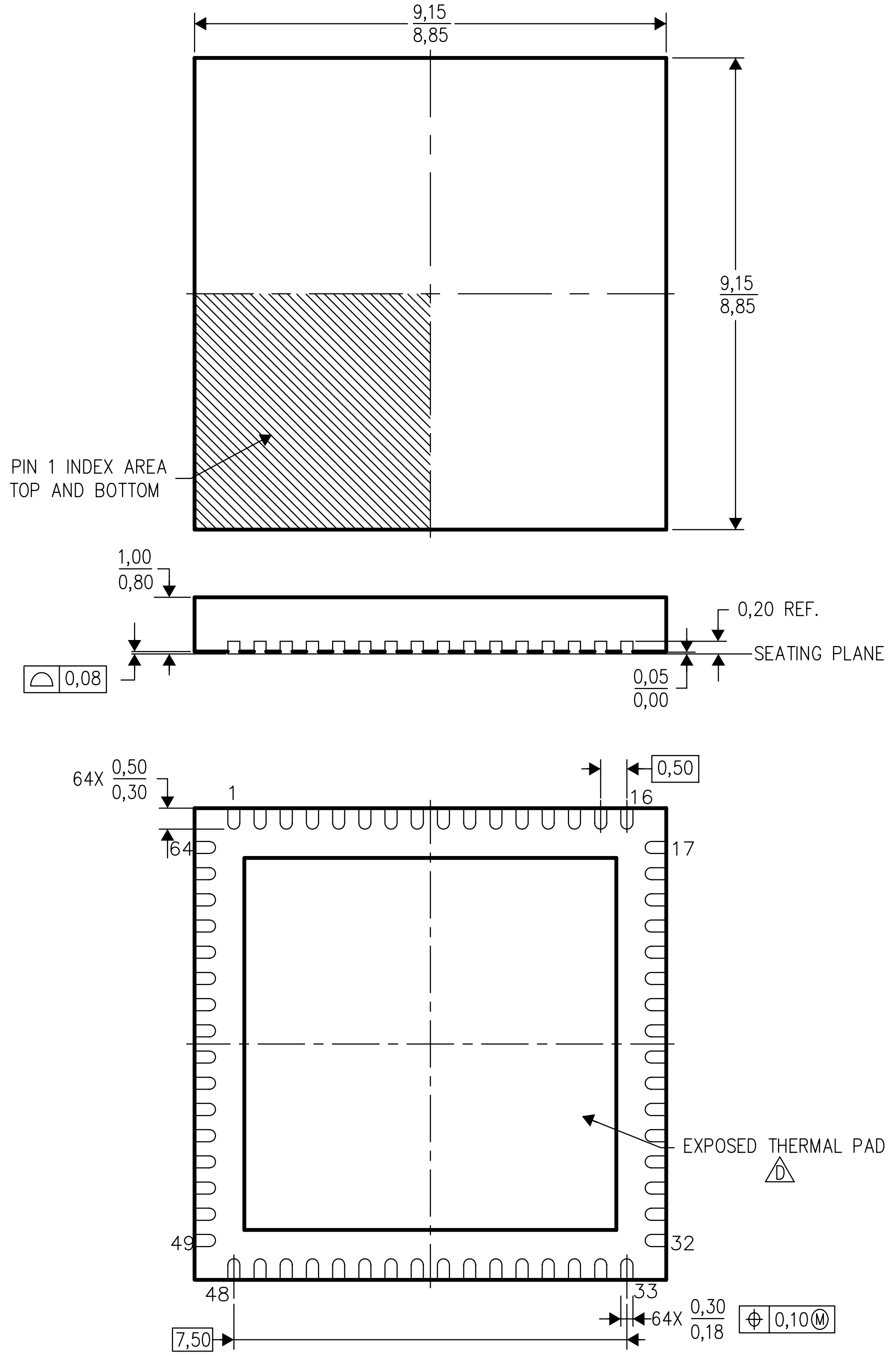
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGC (S-PQFP-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration .
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.