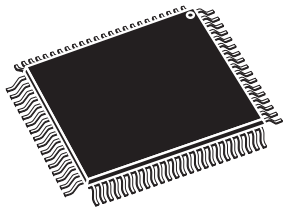
M58BW016DB M58BW016DT M58BW016FT M58BW016FB

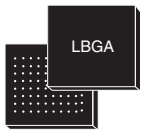
16 Mbit (512 Kbit x 32, boot block, burst) 3 V supply Flash memories

Features

- Supply voltage
  - V_{DD} = 2.7 V to 3.6 V for program, erase and read
  - V_{DDQ} = V_{DDQIN} = 2.4 V to 3.6 V for I/O buffers
  - V_{PP} = 12 V for fast program (optional)
- High performance
  - Access times: 70, 80 ns
  - 56 MHz effective zero wait-state burst read
  - Synchronous burst read
  - Asynchronous page read
- Hardware block protection
  - $\overline{WP}$ pin for write protect of the 4 outermost parameter blocks and all main blocks
  - $\overline{RP}$ pin for write protect of all blocks
- Optimized for FDI drivers
  - Fast program / erase suspend latency time < 6 µs
  - Common Flash interface
- Memory blocks
  - 8 parameters blocks (top or bottom)
  - 31 main blocks
- Low power consumption
  - 5 µA typical deep power-down
  - 60 µA typical standby for M58BW016DT/B 150 µA typical standby for M58BW016FT/B
  - Automatic standby after asynchronous read
- Electronic signature
  - Manufacturer code: 20h
  - Top device code: 8836h
  - Bottom device code: 8835h
- 100 K write/erase cycling + 20 years data retention (minimum)
- High reliability level with over 1 M write/erase cycling sustained
- ECOPACK® packages available



PQFP80 (T)



LBGA80 10 × 12 mm

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1 Description

The M58BW016DT, M58BW016DB, M58BW016FT and M58BW016FB are 16-Mbit non-volatile Flash memories that can be erased electrically at the block level and programmed in-system on a double-word basis using a 2.7 V to 3.6 V V_{DD} supply for the circuit and a V_{DDQ} supply down to 2.4 V for the input and output buffers. Optionally a 12 V V_{PP} supply can be used to provide fast program and erase for a limited time and number of program/erase cycles.

The devices support asynchronous (latch controlled and page read) and synchronous bus operations. The synchronous burst read interface allows a high data transfer rate controlled by the burst clock, K, signal. It is capable of bursting fixed or unlimited lengths of data. The burst type, latency and length can be configured and can be easily adapted to a large variety of system clock frequencies and microprocessors. All writes are asynchronous. On power-up the memory defaults to read mode with an asynchronous bus.

The devices have a boot block architecture with an array of 8 parameter blocks of 64 Kbits each and 31 main blocks of 512 Kbits each. In the M58BW016DT and M58BW016FT the parameter blocks are located at the top of the address space whereas in the M58BW016DB and M58BW016FB, they are located at the bottom.

Program and erase commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified in the status register. The command set required to control the memory is consistent with JEDEC standards.

Erase can be suspended in order to perform either read or program in any other block and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

All blocks are protected during power-up.

The M58BW016DT, M58BW016DB, M58BW016FT and M58BW016FB feature two different levels of block protection to avoid unwanted program/erase operations:

- The $\overline{WP}$ pin offers an hardware protection on two of the parameter blocks and all of the main blocks
- All program or erase operations are blocked when Reset, $\overline{RP}$, is held Low. A reset/power-down mode is entered when the $\overline{RP}$ input is Low. In this mode the power consumption is lower than in the normal standby mode, the device is write protected and both the status and the burst configuration registers are cleared. A recovery time is required when the $\overline{RP}$ input goes High.

The memory is offered in a PQFP80 (14 x 20 mm) and LBGA80 (10 × 12 mm) package.

The memories are supplied with all the bits erased (set to ’1’).

In the present document, M58BW016DT, M58BW016DB, M58BW016FT and M58BW016FB will be referred to as M58BW016 unless otherwise specified.

Figure 1. Logic diagram

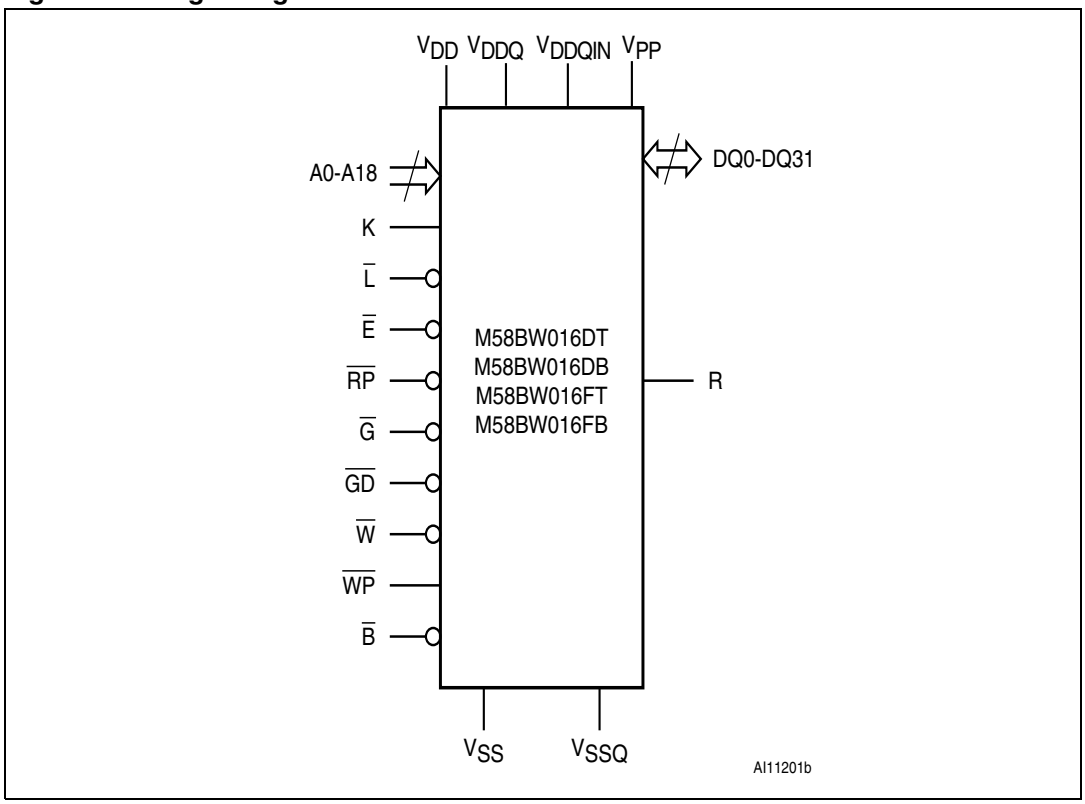


Table 1. Signal names

Signal	Description	Direction
A0-A18	Address inputs	Inputs
DQ0-DQ7	Data input/output, command input	I/O
DQ8-DQ15	Data input/output, Burst Configuration Register	I/O
DQ16-DQ31	Data input/output	I/O
$\overline{B}$	Burst Address Advance	Input
$\overline{E}$	Chip Enable	Input
$\overline{G}$	Output Enable	Input
K	Burst Clock	Input
$\overline{L}$	Latch Enable	Input
R	Valid Data Ready (open drain output)	Output
$\overline{RP}$	Reset/Power-down	Input
$\overline{W}$	Write Enable	Input
$\overline{GD}$	Output Disable	Input
$\overline{WP}$	Write Protect	Input
V_{DD}	Supply voltage	Supply
V_{DDQ}	Power supply for output buffers	Supply
V_{DDQIN}	Power supply for input buffers only	Supply
V_{PP}	Optional supply voltage for fast program and fast erase operations	Supply
V_{SS}	Ground	–
V_{SSQ}	Input/output ground	–
NC	Not connected internally	–
DU	Don’t use as internally connected	–

Figure 2. PQFP connections (top view through package)

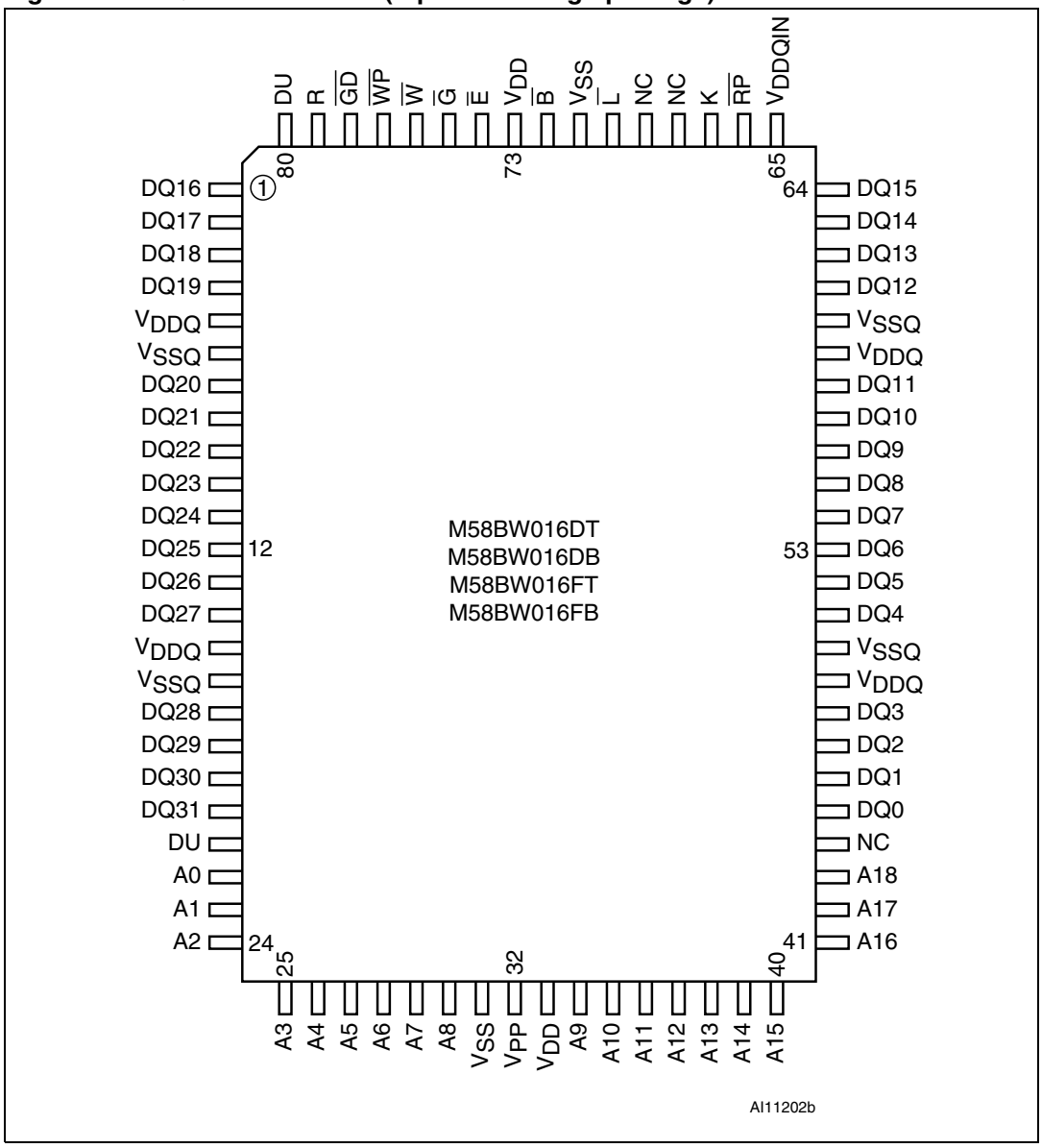
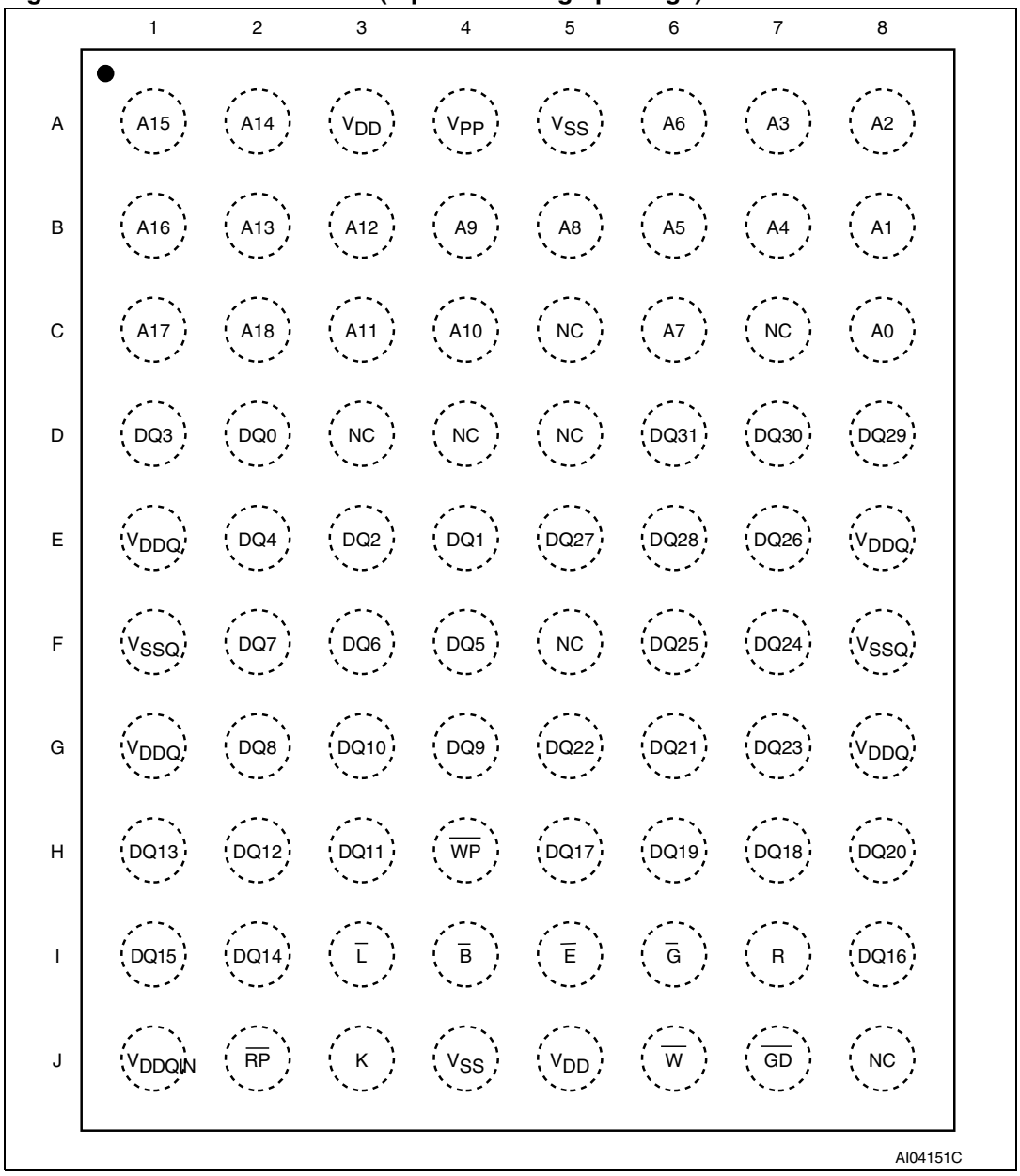


Figure 3. LBGA connections (top view through package)



1.1 Block protection

The M58BW016 feature two different levels of block protection.

- **Write protect pin, $\overline{WP}$ -** When $\overline{WP}$ is Low, V_{IL}, all the lockable parameter blocks (two upper (top) or lower (bottom)) and all the main blocks are protected. When $\overline{WP}$ is High (V_{IH}) all the lockable parameter blocks and all the main blocks are unprotected
- **Reset/power-down pin, $\overline{RP}$ -** If the device is held in reset mode ($\overline{RP}$ at V_{IL}), no program or erase operations can be performed on any block.

After a device reset the first two kinds of block protection ($\overline{WP}$, $\overline{RP}$) can be combined to give a flexible block protection.

Table 2. M58BW016DT and M58BW016FT top boot block addresses

#	Size (Kbit)	Address range
38	64	7F800h-7FFFFh
37	64	7F000h-7F7FFh
36	64	7E800h-7EFFFh
35	64	7E000h-7E7FFh
34	64	7D800h-7DFFFh
33	64	7D000h-7D7FFh
32	64	7C800h-7CFFFh
31	64	7C000h-7C7FFh
30	512	78000h-7BFFFh
29	512	74000h-77FFFh
28	512	70000h-73FFFh
27	512	6C000h-6FFFFh
26	512	68000h-6BFFFh
25	512	64000h-67FFFh
24	512	60000h-63FFFh
23	512	5C000h-5FFFFh
22	512	58000h-5BFFFh
21	512	54000h-57FFFh
20	512	50000h-53FFFh
19	512	4C000h-4FFFFh
18	512	48000h-4BFFFh
17	512	44000h-47FFFh
16	512	40000h-43FFFh
15	512	3C000h-3FFFFh
14	512	38000h-3BFFFh
13	512	34000h-37FFFh
12	512	30000h-33FFFh
11	512	2C000h-2FFFFh
10	512	28000h-2BFFFh
9	512	24000h-27FFFh
8	512	20000h-23FFFh
7	512	1C000h-1FFFFh
6	512	18000h-1BFFFh
5	512	14000h-17FFFh
4	512	10000h-13FFFh
3	512	0C000h-0FFFFh
2	512	08000h-0BFFFh
1	512	04000h-07FFFh
0	512	00000h-03FFFh

Table 3. M58BW016DB and M58BW016FB bottom boot block addresses

#	Size (Kbit)	Address range
38	512	7C000h-7FFFFh
37	512	78000h-7BFFFh
36	512	74000h-77FFFh
35	512	70000h-73FFFh
34	512	6C000h-6FFFFh
33	512	68000h-6BFFFh
32	512	64000h-67FFFh
31	512	60000h-63FFFh
30	512	5C000h-5FFFFh
29	512	58000h-5BFFFh
28	512	54000h-57FFFh
27	512	50000h-53FFFh
26	512	4C000h-4FFFFh
25	512	48000h-4BFFFh
24	512	44000h-47FFFh
23	512	40000h-43FFFh
22	512	3C000h-3FFFFh
21	512	38000h-3BFFFh
20	512	34000h-37FFFh
19	512	30000h-33FFFh
18	512	2C000h-2FFFFh
17	512	28000h-2BFFFh
16	512	24000h-27FFFh
15	512	20000h-23FFFh
14	512	1C000h-1FFFFh
13	512	18000h-1BFFFh
12	512	14000h-17FFFh
11	512	10000h-13FFFh
10	512	0C000h-0FFFFh
9	512	08000h-0BFFFh
8	512	04000h-07FFFh
7	64	03800h-03FFFh
6	64	03000h-037FFh
5	64	02800h-02FFFh
4	64	02000h-027FFh
3	64	01800h-01FFFh
2	64	01000h-017FFh
1	64	00800h-00FFFh
0	64	00000h-007FFh

2 Signal descriptions

See *Figure 1: Logic diagram*, and *Table 1: Signal names* for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-A18)

The address inputs are used to select the cells to access in the memory array during bus operations either to read or to program data. During bus write operations they control the commands sent to the command interface of the program/erase controller. Chip Enable must be Low when selecting the addresses.

The address inputs are latched on the rising edge of Latch Enable $\overline{L}$ or Burst Clock K, whichever occurs first, in a read operation.The address inputs are latched on the rising edge of Chip Enable, Write Enable or Latch Enable, whichever occurs first in a write operation. The address latch is transparent when Latch Enable is Low, V_{IL}. The address is internally latched in an erase or program operation.

2.2 Data inputs/outputs (DQ0-DQ31)

The data inputs/outputs output the data stored at the selected address during a bus read operation, or are used to input the data during a program operation. During bus write operations they represent the commands sent to the command interface of the program/erase controller. When used to input data or write commands they are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first.

When Chip Enable and Output Enable are both Low, V_{IL}, and Output Disable is at V_{IH}, the data bus outputs data from the memory array, the electronic signature, the CFI information or the contents of the status register. The data bus is high impedance when the device is deselected with Chip Enable at V_{IH}, Output Enable at V_{IH}, Output Disable at V_{IL} or Reset/Power-down at V_{IL}. The status register content is output on DQ0-DQ7 and DQ8-DQ31 are at V_{IL}.

2.3 Chip Enable ($\overline{E}$)

The Chip Enable, $\overline{E}$, input activates the memory control logic, input buffers, decoders and sense amplifiers. Chip Enable, $\overline{E}$, at V_{IH} deselects the memory and reduces the power consumption to the standby level.

2.4 Output Enable ($\overline{G}$)

The Output Enable, $\overline{G}$, gates the outputs through the data output buffers during a read operation, when Output Disable $\overline{GD}$ is at V_{IH}. When Output Enable $\overline{G}$ is at V_{IH}, the outputs are high impedance independently of Output Disable.

2.5 Output Disable ($\overline{GD}$)

The Output Disable, $\overline{GD}$, deactivates the data output buffers. When Output Disable, $\overline{GD}$, is at V_{IH}, the outputs are driven by the Output Enable. When Output Disable, $\overline{GD}$, is at V_{IL}, the outputs are high impedance independently of Output Enable. The Output Disable pin must be connected to an external pull-up resistor as there is no internal pull-up resistor to drive the pin.

2.6 Write Enable ($\overline{W}$)

The Write Enable, $\overline{W}$, input controls writing to the command interface, Address inputs and Data latches. Both addresses and data can be latched on the rising edge of Write Enable (also see Latch Enable, $\overline{L}$).

2.7 Reset/Power-down ($\overline{RP}$)

The Reset/Power-down, $\overline{RP}$, is used to apply a hardware reset to the memory. A hardware reset is achieved by holding Reset/Power-down Low, V_{IL}, for at least t_{PLPH}. Writing is inhibited to protect data, the command interface and the program/erase controller are reset. The status register information is cleared and power consumption is reduced to deep power-down level. The device acts as deselected, that is the data outputs are high impedance.

After Reset/Power-down goes High, V_{IH}, the memory will be ready for bus read operations after a delay of t_{PHEL} or bus write operations after t_{PHWL}.

If Reset/Power-down goes Low, V_{IL}, during a Block Erase, or a Program the operation is aborted, in a time of t_{PLRH} maximum, and data is altered and may be corrupted.

During power-up power should be applied simultaneously to V_{DD} and $V_{DDQ(IN)}$ with $\overline{RP}$ held at V_{IL}. When the supplies are stable $\overline{RP}$ is taken to V_{IH}. Output Enable, $\overline{G}$, Chip Enable, $\overline{E}$, and Write Enable, $\overline{W}$, should be held at V_{IH} during power-up.

In an application, it is recommended to associate reset/power-down pin, $\overline{RP}$, with the reset signal of the microprocessor. Otherwise, if a reset operation occurs while the memory is performing an erase or program operation, the memory may output the status register information instead of being initialized to the default asynchronous random read.

See *Table 22: Reset, power-down and power-up AC characteristics* and *Figure 17: Reset, power-down and power-up AC waveforms - control pins low*, for more details.

2.8 Latch Enable ($\overline{L}$)

The bus interface can be configured to latch the address inputs on the rising edge of Latch Enable, $\overline{L}$, for asynchronous latch enable controlled read or write or synchronous burst read operations. In synchronous burst read operations the address is latched on the active edge of the Clock when Latch Enable is Low, V_{IL}. Once latched, the addresses may change without affecting the address used by the memory. When Latch Enable is Low, V_{IL}, the latch is transparent. Latch Enable, $\overline{L}$, can remain at V_{IL} for asynchronous random read and write operations.

2.9 Burst Clock (K)

The Burst Clock, K, is used to synchronize the memory with the external bus during synchronous burst read operations. Bus signals are latched on the active edge of the Clock. The Clock can be configured to have an active rising or falling edge. In synchronous burst read mode the address is latched on the first active clock edge when Latch Enable is Low, V_{IL}, or on the rising edge of Latch Enable, whichever occurs first.

During asynchronous bus operations the Clock is not used.

2.10 Burst Address Advance ($\overline{B}$)

The Burst Address Advance, $\overline{B}$, controls the advancing of the address by the internal address counter during synchronous burst read operations.

Burst Address Advance, $\overline{B}$, is only sampled on the active clock edge of the Clock when the X-latency time has expired. If Burst Address Advance is Low, V_{IL}, the internal address counter advances. If Burst Address Advance is High, V_{IH}, the internal address counter does not change; the same data remains on the data inputs/outputs and Burst Address Advance is not sampled until the Y-latency expires.

The Burst Address Advance, $\overline{B}$, may be tied to V_{IL}.

2.11 Valid Data Ready (R)

The Valid Data Ready output, R, is an open drain output that can be used, during synchronous burst read operations, to identify if the memory is ready to output data or not. The Valid Data Ready output can be configured to be active on the clock edge of the invalid data read cycle or one cycle before. Valid Data Ready, at V_{IH}, indicates that new data is or will be available. When Valid Data Ready is Low, V_{IL}, the previous data outputs remain active.

In all asynchronous operations, Valid Data Ready is high impedance. It may be tied to other components with the same Valid Data Ready signal to create a unique system Ready signal. The Valid Data Ready output has an internal pull-up resistor of around 1 MΩ powered from V_{DDQ}, designers should use an external pull-up resistor of the correct value to meet the external timing requirements for Valid Data Ready going to V_{IH}.

2.12 Write Protect ($\overline{WP}$)

The Write Protect, $\overline{WP}$, provides protection against program or erase operations. When Write Protect, $\overline{WP}$, is at V_{IL} the first two (in the bottom configuration) or last two (in the top configuration) parameter blocks and all main blocks are locked. When Write Protect $\overline{WP}$ is at V_{IH} all the blocks can be programmed or erased, if no other protection is used.

2.13 Supply voltage (V_{DD})

The supply voltage, V_{DD}, is the core power supply. All internal circuits draw their current from the V_{DD} pin, including the program/erase controller.

2.14 Output supply voltage (V_{DDQ})

The output supply voltage, V_{DDQ}, is the output buffer power supply for all operations (read, program and erase) used for DQ0-DQ31 when used as outputs.

2.15 Input supply voltage (V_{DDQIN})

The input supply voltage, V_{DDIN}, is the power supply for all input signal. Input signals are: K, $\overline{B}$, $\overline{L}$, $\overline{W}$, $\overline{GD}$, $\overline{G}$, $\overline{E}$, A0-A18 and DQ0-DQ31, when used as inputs.

2.16 Program/erase supply voltage (V_{PP})

The program/erase supply voltage, V_{PP}, is used for program and erase operations. The memory normally executes program and erase operations at V_{PP1} voltage levels. In a manufacturing environment, programming may be speeded up by applying a higher voltage level, V_{PPH}, to the V_{PP} pin.

The voltage level V_{PPH} may be applied for a total of 80 hours over a maximum of 1000 cycles. Stressing the device beyond these limits could damage the device.

2.17 Ground (V_{SS} and V_{SSQ})

The ground V_{SS} is the reference for the internal supply voltage V_{DD}. The ground V_{SSQ} is the reference for the output and input supplies $V_{DDQ,}$ and V_{DDQIN}. It is essential to connect V_{SS} and V_{SSQ} together.

Note: A 0.1 µF capacitor should be connected between the supply voltages, V_{DD}, V_{DDQ} and V_{DDIN} and the grounds, V_{SS} and V_{SSQ} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during all operations of the parts, see Table 15: DC characteristics, for maximum current supply requirements.

2.18 Don't use (DU)

This pin should not be used as it is internally connected. Its voltage level can be between V_{SS} and V_{DDQ} or leave it unconnected.

2.19 Not connected (NC)

This pin is not physically connected to the device.

3 Bus operations

Each bus operation that controls the memory is described in this section, see *Table 4*, *Table 5* and *Table 6* Bus operations, for a summary. The bus operation is selected through the burst configuration register; the bits in this register are described at the end of this section.

On power-up or after a hardware reset the memory defaults to asynchronous bus read and asynchronous bus write, no other bus operation can be performed until the burst control register has been configured.

The electronic signature, CFI or status register will be read in asynchronous mode regardless of the burst control register settings.

Typically glitches of less than 5 ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

3.1 Asynchronous bus operations

For asynchronous bus operations refer to *Table 4* together with the following text.

3.1.1 Asynchronous bus read

Asynchronous bus read operations read from the memory cells, or specific registers (electronic signature, status register, CFI and burst configuration register) in the command interface. A valid bus operation involves setting the desired address on the address inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable and Output Disable High, V_{IH}. The data inputs/outputs will output the value, see *Figure 8: Asynchronous bus read AC waveforms*, and *Table 16: Asynchronous bus read AC characteristics*, for details of when the output becomes valid.

Asynchronous read is the default read mode which the device enters on power-up or on return from reset/power-down.

3.1.2 Asynchronous latch controlled bus read

Asynchronous latch controlled bus read operations read from the memory cells or specific registers in the command interface. The address is latched in the memory before the value is output on the data bus, allowing the address to change during the cycle without affecting the address that the memory uses.

A valid bus operation involves setting the desired address on the address inputs, setting Chip Enable and Latch Enable Low, V_{IL} and keeping Write Enable High, V_{IH}; the address is latched on the rising edge of Latch Enable. Once latched, the address inputs can change. Set Output Enable Low, V_{IL}, to read the data on the data inputs/outputs; see *Figure 9: Asynchronous latch controlled bus read AC waveforms*, and *Table 17: Asynchronous latch controlled bus read AC characteristics*, for details on when the output becomes valid.

Note that, since the Latch Enable input is transparent when set Low, V_{IL}, asynchronous bus read operations can be performed when the memory is configured for asynchronous latch enable bus operations by holding Latch Enable Low, V_{IL} throughout the bus operation.

3.1.3 Asynchronous page read

Asynchronous page read operations are used to read from several addresses within the same memory page. Each memory page is 4 double-words and is addressed by the address inputs A0 and A1.

Data is read internally and stored in the page buffer. Valid bus operations are the same as asynchronous bus read operations but with different timings. The first read operation within the page has identical timings, subsequent reads within the same page have much shorter access times. If the page changes then the normal, longer timings apply again. Page read does not support latched controlled read.

See *Figure 10: Asynchronous page read AC waveforms*, and *Table 18: Asynchronous page read AC characteristics*, for details on when the outputs become valid.

3.1.4 Asynchronous bus write

Asynchronous bus write operations write to the command interface to send commands to the memory or to latch addresses and input data to program. Bus write operations are asynchronous, the clock, K, is don't care during bus write operations.

A valid asynchronous bus write operation begins by setting the desired address on the address inputs, and setting Chip Enable, Write Enable and Latch Enable Low, V_{IL}, and Output Enable High, V_{IH}, or Output Disable Low, V_{IL}. The address inputs are latched by the command interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Commands and input data are latched on the rising edge of Chip Enable, $\overline{E}$, or Write Enable, $\overline{W}$, whichever occurs first. Output Enable must remain High, and Output Disable Low, during the whole asynchronous bus write operation.

See *Figure 11: Asynchronous write AC waveforms*, and *Table 19: Asynchronous write and latch controlled write AC characteristics*, for details of the timing requirements.

3.1.5 Asynchronous latch controlled bus write

Asynchronous latch controlled bus write operations write to the command interface to send commands to the memory or to latch addresses and input data to program. Bus write operations are asynchronous, the clock, K, is don't care during bus write operations.

A valid asynchronous latch controlled bus write operation begins by setting the desired address on the address inputs and pulsing Latch Enable Low, V_{IL}. The address inputs are latched by the command interface on the rising edge of Latch Enable, Write Enable or Chip Enable, whichever occurs first. Commands and input data are latched on the rising edge of Chip Enable, $\overline{E}$, or Write Enable, $\overline{W}$, whichever occurs first. Output Enable must remain High, and Output Disable Low, during the whole asynchronous bus write operation.

See *Figure 12: Asynchronous latch controlled write AC waveforms*, and *Table 19: Asynchronous write and latch controlled write AC characteristics*, for details of the timing requirements.

3.1.6 Output Disable

The data outputs are high impedance when the Output Enable, $\overline{G}$, is at V_{IH} or Output Disable, $\overline{GD}$, is at V_{IL}.

3.1.7 Standby mode

When Chip Enable is High, V_{IH}, and the Program/Erase controller is idle, the memory enters Standby mode, the power consumption is reduced to the standby level and the Data inputs/outputs pins are placed in the high impedance state regardless of Output Enable, Write Enable or Output Disable inputs.

3.1.8 Automatic low power mode

If there is no change in the state of the bus for a short period of time during asynchronous bus read operations the memory enters auto low power mode where the internal supply current is reduced to the auto-standby supply current. The data inputs/outputs will still output data if a bus read operation is in progress.

Automatic low power is only available in asynchronous read modes.

3.1.9 Power-down mode

The memory is in power-down when Reset/Power-down, $\overline{RP}$, is at V_{IL}. The power consumption is reduced to the power-down level and the outputs are high impedance, independent of the Chip Enable, $\overline{E}$, Output Enable, $\overline{G}$, Output Disable, $\overline{GD}$, or Write Enable, $\overline{W}$, inputs.

3.1.10 Electronic signature

Two codes identifying the manufacturer and the device can be read from the memory allowing programming equipment or applications to automatically match their interface to the characteristics of the memory. The electronic signature is output by giving the Read Electronic Signature command. The manufacturer code is output when all the address inputs are at V_{IL}. The device code is output when A1 is at V_{IH} and all the other address pins are at V_{IL} (see *Table 5: Asynchronous read electronic signature operation*). Issue a Read Memory Array command to return to read mode.

Table 4. Asynchronous bus operations(1)

Bus operation	Step	$\overline{E}$	$\overline{G}$	$\overline{GD}$	$\overline{W}$	$\overline{RP}$	$\overline{L}$	A0-A18	DQ0-DQ31
Asynchronous bus read		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Address	Data output
Asynchronous latch controlled bus read	Address Latch	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Address	High-Z
	Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	Data output
Asynchronous page read		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Address	Data output
Asynchronous bus write		V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	Address	Data input
Asynchronous latch controlled bus write	Address Latch	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Address	High-Z
	Write	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{IH}	X	Data input
Output Enable, $\overline{G}$		V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	High-Z
Output Disable, $\overline{GD}$		V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	High-Z
Standby		V_{IH}	X	X	X	V_{IH}	X	X	High-Z
Reset/power-down		X	X	X	X	V_{IL}	X	X	High-Z

1. X = don't care.

Table 5. Asynchronous read electronic signature operation

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{GD}$	$\overline{W}$	A18-A0	DQ31-DQ0
Manufacturer	All	V_{IL}	V_{IL}	V_{IH}	V_{IH}	00000h	00000020h
Device	M58BW016DT M58BW016FT	V_{IL}	V_{IL}	V_{IH}	V_{IH}	00001h	00008836h
	M58BW016DB M58BW016FB	V_{IL}	V_{IL}	V_{IH}	V_{IH}	00001h	00008835h
Burst configuration register		V_{IL}	V_{IL}	V_{IH}	V_{IH}	00005h	BCR(1)

1. BCR = Burst configuration register.

3.2 Synchronous bus operations

For synchronous bus operations refer to *Table 6* together with the following text.

3.2.1 Synchronous burst read

Synchronous burst read operations are used to read from the memory at specific times synchronized to an external reference clock.

In the M58BW016FT and M58BW016FB only, once the memory is configured in burst mode, it is mandatory to have an active clock signal since the switching of the output buffer data bus is synchronized to the active edge of the clock. In the absence of clock, no data is output.

Caution: The M58BW016DT and M58BW016DB are not concerned by the paragraph above.

The burst type, length and latency can be configured. The different configurations for synchronous burst read operations are described in *Section 3.3: Burst configuration register*. Refer to *Figure 4* and *Figure 5* for examples of synchronous burst operations.

In continuous burst read, one burst read operation can access the entire memory sequentially by keeping the Burst Address Advance $\overline{B}$ at V_{IL} for the appropriate number of clock cycles. At the end of the memory address space the burst read restarts from the beginning at address 000000h.

A valid synchronous burst read operation begins when the Burst Clock is active and Chip Enable and Latch Enable are Low, V_{IL}. The burst start address is latched and loaded into the internal burst address counter on the valid Burst Clock K edge (rising or falling depending on the value of M6) or on the rising edge of Latch Enable, whichever occurs first.

After an initial memory latency time, the memory outputs data each clock cycle (or two clock cycles depending on the value of M9). The Burst Address Advance $\overline{B}$ input controls the memory burst output. The second burst output is on the next clock valid edge after the Burst Address Advance $\overline{B}$ has been pulled Low.

Valid Data Ready, R, monitors if the memory burst boundary is exceeded and the burst controller of the microprocessor needs to insert wait states. When Valid Data Ready is Low on the active clock edge, no new data is available and the memory does not increment the internal address counter at the active clock edge even if Burst Address Advance, $\overline{B}$, is Low.

Valid Data Ready may be configured (by bit M8 of burst configuration register) to be valid immediately at the valid clock edge or one data cycle before the valid clock edge.

Synchronous burst read will be suspended if Burst Address Advance, $\overline{B}$, goes High, V_{IH}.

If Output Enable is at V_{IL} and Output Disable is at V_{IH}, the last data is still valid.

If Output Enable, $\overline{G}$, is at V_{IH} or Output Disable, $\overline{GD}$, is at V_{IL}, but the Burst Address Advance, $\overline{B}$, is at V_{IL} the internal Burst Address counter is incremented at each Burst Clock K valid edge.

The synchronous burst read timing diagrams and AC characteristics are described in the AC and DC parameters section. See *Figure 13*, *Figure 14*, *Figure 15* and *Figure 16*, and *Table 20*.

3.2.2 Synchronous burst read suspend

During a synchronous burst read operation it is possible to suspend the operation, freeing the data bus for other higher priority devices.

A valid synchronous burst read operation is suspended when both Output Enable and Burst Address Advance are High, V_{IH}. The Burst Address Advance going High, V_{IH}, stops the burst counter and the Output Enable going High, V_{IH}, inhibits the data outputs. The synchronous burst read operation can be resumed by setting Output Enable Low.

Table 6. Synchronous burst read bus operations(1)(2)

Bus operation	Step	$\overline{E}$	$\overline{G}$	$\overline{GD}$	$\overline{RP}$	K(3)	$\overline{L}$	$\overline{B}$	A0-A18 DQ0-DQ31
Synchronous burst read	Address Latch	V_{IL}	V_{IH}	X	V_{IH}	T	V_{IL}	X	Address input
	Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	T	V_{IH}	V_{IL}	Data output
	Read Suspend	V_{IL}	V_{IH}	X	V_{IH}	X	V_{IH}	V_{IH}	High-Z
	Read Resume	V_{IL}	V_{IL}	V_{IH}	V_{IH}	T	V_{IH}	V_{IL}	Data output
	Burst Address Advance	V_{IL}	V_{IH}	X	V_{IH}	T	V_{IH}	V_{IL}	High-Z
	Read Abort, $\overline{E}$	V_{IH}	X	X	V_{IH}	X	X	X	High-Z
	Read Abort, $\overline{RP}$	X	X	X	V_{IL}	X	X	X	High-Z

1. X = don't care, V_{IL} or V_{IH}.
2. M15 = 0, bit M15 is in the burst configuration register.
3. T = transition, see M6 in the burst configuration register for details on the active edge of K.

3.3 Burst configuration register

The burst configuration register is used to configure the type of bus access that the memory will perform.

The burst configuration register is set through the command interface and will retain its information until it is re-configured, the device is reset, or the device goes into reset/power-down mode. The burst configuration register bits are described in *Table 7*. They specify the selection of the burst length, burst type, burst X and Y latencies and the read operation. Refer to *Figure 4* and *Figure 5* for examples of synchronous burst configurations.

3.3.1 Read select bit (M15)

The read select bit, M15, is used to switch between asynchronous and synchronous bus read operations. When the read select bit is set to '1', bus read operations are asynchronous; when the read select bit is set to '0', bus read operations are synchronous.

On reset or power-up the read select bit is set to'1' for asynchronous accesses.

3.3.2 X-Latency bits (M14-M11)

The X-Latency bits are used during synchronous bus read operations to set the number of clock cycles between the address being latched and the first data becoming available. For correct operation the X-Latency bits can only assume the values in *Table 7: Burst configuration register*. The X-Latency bits should also be selected in conjunction with *Table 8: Burst type definition* to ensure valid settings.

3.3.3 Y-Latency bit (M9)

The Y-Latency bit is used during synchronous bus read operations to set the number of clock cycles between consecutive reads. The Y-Latency value depends on both the X-Latency value and the setting in M9.

When the Y-Latency is '1' the data changes each clock cycle; when the Y-Latency is '2' the data changes every second clock cycle. See *Table 7: Burst configuration register*, and *Table 8: Burst type definition* for valid combinations of the Y-Latency, the X-Latency and the clock frequency.

3.3.4 Valid data ready bit (M8)

The valid data ready bit controls the timing of the valid data ready output pin, R. When the valid data ready bit is '0' the valid data ready output pin is driven Low for the active clock edge when invalid data is output on the bus. When the valid data ready bit is '1' the valid data ready output pin is driven Low one clock cycle prior to invalid data being output on the bus.

3.3.5 Burst type bit (M7)

The burst type bit is used to configure the sequence of addresses read as sequential or interleaved. When the burst type bit is '0' the memory outputs from interleaved addresses; when the burst type bit is '1' the memory outputs from sequential addresses. See *Table 8: Burst type definition*, for the sequence of addresses output from a given starting address in each mode.

3.3.6 Valid clock edge bit (M6)

The valid clock edge bit, M6, is used to configure the active edge of the Clock, K, during synchronous burst read operations. When the valid clock edge bit is ’0’ the falling edge of the clock is the active edge; when the valid clock edge bit is ’1’ the rising edge of the clock is active.

3.3.7 Wrap burst bit (M3)

The burst reads can be confined inside the 4 or 8 double-word boundary (wrap) or overcome the boundary (no wrap). The wrap burst bit is used to select between wrap and no wrap. When the wrap burst bit is set to ‘0’ the burst read wraps; when it is set to ‘1’ the burst read does not wrap.

3.3.8 Burst length bit (M2-M0)

The burst length bits set the maximum number of double-words that can be output during a synchronous burst read operation before the address wraps. Burst lengths of 4 or 8 are available for both the sequential and interleaved burst types, and a continuous burst is available for the sequential type.

Table 7: Burst configuration register gives the valid combinations of the burst length bits that the memory accepts; *Table 8: Burst type definition*, gives the sequence of addresses output from a given starting address for each length.

If either a continuous or a no wrap burst read has been initiated the device will output data synchronously. Depending on the starting address, the device activates the valid data ready output to indicate that a delay is necessary before the data is output. If the starting address is aligned to an 8 double-word boundary, the continuous burst mode will run without activating the valid data ready output. If the starting address is not aligned to an 8 double-word boundary, valid data ready is activated to indicate that the device needs an internal delay to read the successive words in the array.

M10, M5 and M4 are reserved for future use.

Table 7. Burst configuration register

Bit	Description	Value	Description
M15	Read select	0	Synchronous burst read
		1	Asynchronous read (default at power-on)
M14		0	Reserved (default value)
M13-M11	X-Latency(1)	000	Reserved (default value)
		001	Reserved
		010	4, 4-1-1-1(2)
		011	5(3), 5-1-1-1, 5-2-2-2
		100	6(3), 6-1-1-1, 6-2-2-2
		101	7(3), 7-1-1-1, 7-2-2-2
		110	8(3), 8-1-1-1, 8-2-2-2
		111	Reserved
M10		0	Reserved (default value)
M9	Y-Latency(4)	0	One burst clock cycle (default value)
		1	Two burst clock cycles
M8	Valid data ready	0	R valid Low during valid burst clock edge (default value)
		1	R valid Low 1 data cycle before valid burst clock edge
M7	Burst type	0	Interleaved (default value)
		1	Sequential
M6	Valid clock edge	0	Falling burst clock edge (default value)
		1	Rising burst clock edge
M5-M4		00	Reserved (default value)
		01	Reserved
		10	Reserved
		11	Reserved
M3	Wrapping	0	Wrap (default value)
		1	No wrap
M2-M0	Burst length	000	Reserved (default value)
		001	4 double-words
		010	8 double-words
		011	Reserved
		100	Reserved
		101	Reserved
		110	Reserved
		111	Continuous

1. X latencies can be calculated as: $(t_{AVQV} - t_{LLKH} + t_{QVKH}) + t_{SYSTEM\ MARGIN} < (X - 1)\ t_K$. (X is an integer number from 4 to 8, t_K is the clock period and $t_{SYSTEM\ MARGIN}$ is the time margin required for the calculation).
2. This feature is available for the M58BW016F version up to the full operative frequency of 56 MHz, and for the M58BW016D version only if the operative frequency is below 45 MHz.
3. The M58BW016F version has a maximum operative frequency of 66 MHz, fully factory tested.
4. Y latencies can be calculated as: $t_{KHQV} + t_{SYSTEM\ MARGIN} + t_{QVKH} < Y\ t_K$.

Table 8. Burst type definition

M 3	Starting address	x 4 sequential	x 4 interleaved	x 8 sequential	x 8 interleaved	Continuous
0	0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10..
0	1	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4-5-6-7-8-9-10-11..
0	2	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4-5-6-7-8-9-10-11-12..
0	3	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5-6-7-8-9-10-11-12-13..
0	4	–	–	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-2-13-14..
0	5	–	–	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2	5-6-7-8-9-10-11-12-13-14..
0	6	–	–	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	6-7-8-9-10-11-12-13-14-15..
0	7	–	–	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9-10-11-12-13-14-15-16..
0	8	–	–	–	–	8-9-10-11-12-13-14-15-16-17..
1	0	0-1-2-3	–	0-1-2-3-4-5-6-7	–	0-1-2-3-4-5-6-7-8-9-10..
1	1	1-2-3-4	–	1-2-3-4-5-6-7-8	–	1-2-3-4-5-6-7-8-9-10-11..
1	2	2-3-4-5	–	2-3-4-5-6-7-8-9	–	2-3-4-5-6-7-8-9-10-11-12..
1	3	3-4-5-6	–	3-4-5-6-7-8-9-10	–	3-4-5-6-7-8-9-10-11-12-13..
1	4	4-5-6-7	–	4-5-6-7-8-9-10-11	–	4-5-6-7-8-9-10-11-12-13-14..
1	5	5-6-7-8	–	5-6-7-8-9-10-11-12	–	5-6-7-8-9-10-11-12-13-14..
1	6	6-7-8-9	–	6-7-8-9-10-11-12-13	–	6-7-8-9-10-11-12-13-14-15..
1	7	7-8-9-10	–	7-8-9-10-11-12-13-14	–	7-8-9-10-11-12-13-14-15-16..
1	8	8-9-10-11	–	8-9-10-11-12-13-14-15	–	8-9-10-11-12-13-14-15-16-17..

Figure 4. Example burst configuration X-1-1-1

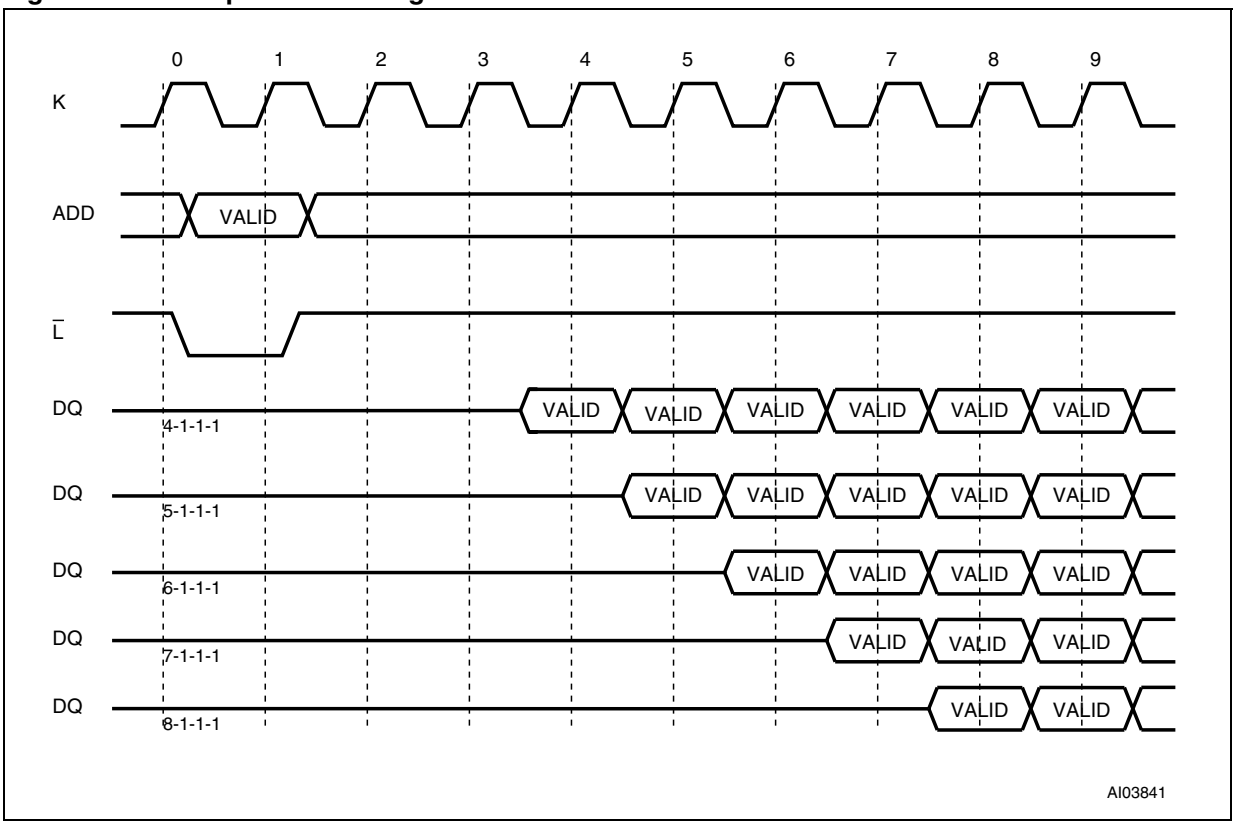
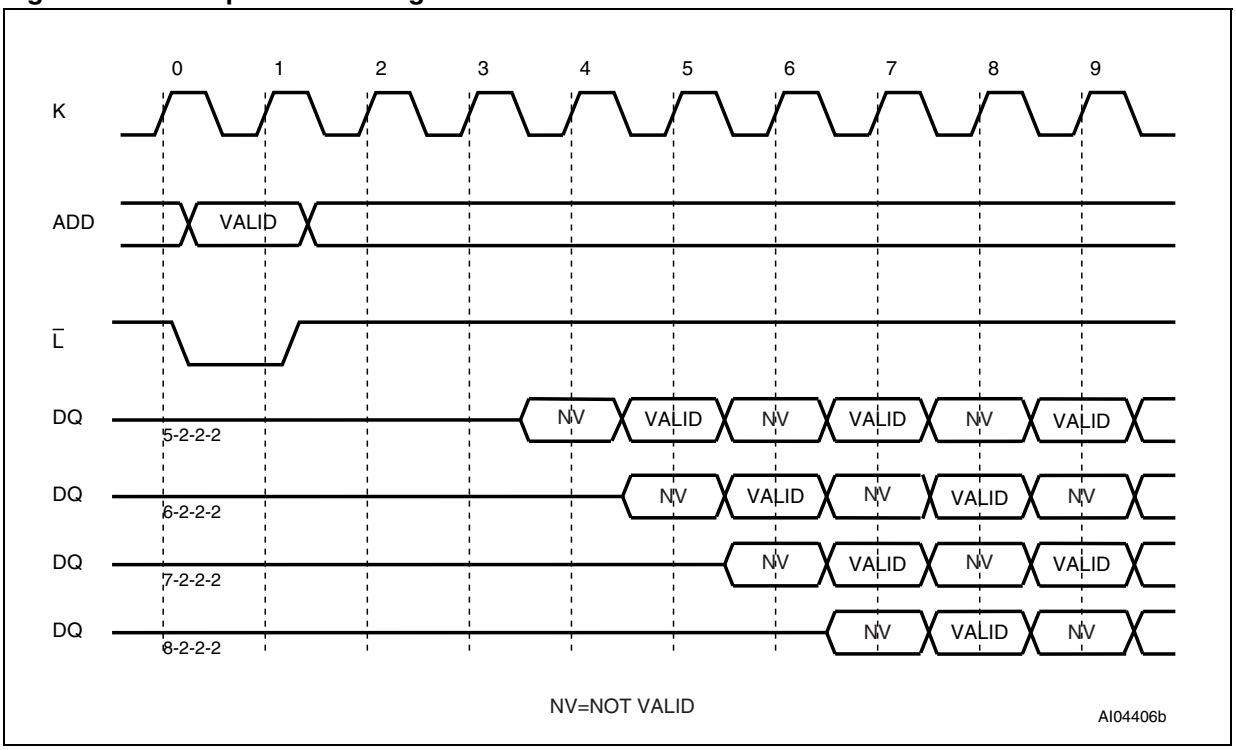


Figure 5. Example burst configuration X-2-2-2



4 Command interface

All bus write operations to the memory are interpreted by the command interface. Commands consist of one or more sequential bus write operations. The commands are summarized in *Table 9: Commands*. Refer to *Table 9* in conjunction with the text descriptions below.

4.1 Read Memory Array command

The Read Memory Array command returns the memory to read mode. One bus write cycle is required to issue the Read Memory Array command and return the memory to read mode. Subsequent read operations will output the addressed memory array data. Once the command is issued the memory remains in read mode until another command is issued. From read mode bus read commands will access the memory array.

4.2 Read Electronic Signature command

The Read Electronic Signature command is used to read the manufacturer code, the device code or the burst configuration register. One bus write cycle is required to issue the Read Electronic Signature command. Once the command is issued subsequent bus read operations, depending on the address specified, read the manufacturer code, the device code or the burst configuration register until another command is issued; see *Table 5: Asynchronous read electronic signature operation*.

4.3 Read Query command

The Read Query command is used to read data from the common Flash interface (CFI) memory area. One bus write cycle is required to issue the Read Query command. Once the command is issued subsequent bus read operations, depending on the address specified, read from the common Flash interface memory area. See *Appendix A: Common Flash interface (CFI)*, *Table 26*, *Table 27*, *Table 28*, *Table 29* and *Table 30* for details on the information contained in the common Flash interface (CFI) memory area.

4.4 Read Status Register command

The Read Status Register command is used to read the status register. One bus write cycle is required to issue the Read Status Register command. Once the command is issued subsequent bus read operations read the status register until another command is issued.

The status register information is present on the output data bus (DQ1-DQ7) when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are at V_{IL} and Output Disable is at V_{IH}.

An interactive update of the status register bits is possible by toggling Output Enable or Output Disable. It is also possible during a program or erase operation, by deactivating the device with Chip Enable at V_{IH} and then reactivating it with Chip Enable and Output Enable at V_{IL} and Output Disable at V_{IH}.

The content of the status register may also be read at the completion of a program, erase or suspend operation. During a Block Erase or Program command, DQ7 indicates the program/erase controller status. It is valid until the operation is completed or suspended.

See the section on the status register and *Table 11* for details on the definitions of the status register bits.

4.5 Clear Status Register command

The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the status register to ‘0’. One bus write is required to issue the Clear Status Register command. Once the command is issued the memory returns to its previous mode, subsequent bus read operations continue to output the same data.

The bits in the status register are sticky and do not automatically return to ‘0’ when a new Program or Erase command is issued. If any error occurs then it is essential to clear any error bits in the status register by issuing the Clear Status Register command before attempting a new Program, Erase or Resume command.

4.6 Block Erase command

The Block Erase command can be used to erase a block. It sets all of the bits in the block to '1'. All previous data in the block is lost. If the block is protected then the erase operation will abort, the data in the block will not be changed and the status register will output the error.

Two bus write operations are required to issue the command; the first write cycle sets up the Block Erase command, the second write cycle confirms the Block Erase command and latches the block address in the program/erase controller and starts it. The sequence is aborted if the Confirm command is not given and the device will output the status register data with bits 4 and 5 set to '1'.

Once the command is issued subsequent bus read operations read the status register. See the section on the status register for details on the definitions of the status register bits. During the erase operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored. The command can be executed using either V_{DD} (for a normal erase operation) or V_{PP} (for a fast erase operation). If V_{PP} is in the V_{PPH} range when the command is issued then a fast erase operation will be executed, otherwise the operation will use V_{DD}. If V_{PP} goes below the V_{PP} lockout voltage, V_{PPLK}, during a fast erase the operation aborts, the status register V_{PP} status bit is set to '1' and the command must be re-issued.

Typical erase times are given in *Table 10*.

See *Appendix B: Flowcharts*, *Figure 24: Block erase flowchart and pseudocode*, for a suggested flowchart on using the Block Erase command.

4.7 Program command

The Program command is used to program the memory array. Two bus write operations are required to issue the command; the first write cycle sets up the Program command, the second write cycle latches the address and data to be programmed in the program/erase controller and starts it. A program operation can be aborted by writing FFFFFFFFh to any address after the program set-up command has been given.

Once the command is issued subsequent bus read operations read the status register. See the section on the status register for details on the definitions of the status register bits. During the program operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored.

If Reset/Power-down, $\overline{RP}$, falls to V_{IL} during programming the operation will be aborted.

The command can be executed using either V_{DD} (for a normal program operation) or V_{PP} (for a fast program operation). If V_{PP} is in the V_{PPH} range when the command is issued then a fast program operation will be executed, otherwise the operation will use V_{DD}. If V_{PP} goes below the V_{PP} lockout voltage, V_{PPLK}, during a fast program the operation aborts and the status register V_{PP} status bit is set to '1'. As data integrity cannot be guaranteed when the program operation is aborted, the memory block must be erased and reprogrammed.

See *Appendix B: Flowcharts on page 59*, *Figure 22: Program flowchart and pseudocode*, for a suggested flowchart on using the Program command.

4.8 Program/Erase Suspend command

The Program/Erase Suspend command is used to pause a program or erase operation. The command will only be accepted during a program or erase operation. It can be issued at any time during a program or erase operation. The command is ignored if the device is already in suspend mode.

One bus write cycle is required to issue the Program/Erase Suspend command and pause the program/erase controller. Once the command is issued it is necessary to poll the program/erase controller status bit (bit 7) to find out when the program/erase controller has paused; no other commands will be accepted until the program/erase controller has paused. After the program/erase controller has paused, the memory will continue to output the status register until another command is issued.

During the polling period between issuing the Program/Erase Suspend command and the program/erase controller pausing it is possible for the operation to complete. Once the program/erase controller status bit (bit 7) indicates that the program/erase controller is no longer active, the program suspend status bit (bit 2) or the erase suspend status bit (bit 6) can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the Program/Erase Suspend command and the program/erase controller pausing see *Table 10*.

During Program/Erase Suspend the Read Memory Array, Read Status Register, Read Electronic Signature, Read Query and Program/Erase Resume commands will be accepted by the command interface. Additionally, if the suspended operation was erase then the Program and the Program Suspend commands will also be accepted. When a program operation is completed inside a Block Erase Suspend the Read Memory Array command must be issued to reset the device in read mode, then the Erase Resume command can be issued to complete the whole sequence. Only the blocks not being erased may be read or programmed correctly.

See *Appendix B: Flowcharts*, *Figure 23: Program suspend & resume flowchart and pseudocode*, and *Figure 25: Erase suspend & resume flowchart and pseudocode*, for suggested flowcharts on using the Program/Erase Suspend command.

4.9 Program/Erase Resume command

The Program/Erase Resume command can be used to restart the program/erase controller after a program/erase suspend operation has paused it. One bus write cycle is required to issue the Program/Erase Resume command.

See *Appendix B: Flowcharts*, *Figure 23: Program suspend & resume flowchart and pseudocode*, and *Figure 25: Erase suspend & resume flowchart and pseudocode*, for suggested flowcharts on using the Program/Erase Resume command.

4.10 Set Burst Configuration Register command

The Set Burst Configuration Register command is used to write a new value to the burst configuration control register which defines the burst length, type, X and Y latencies, synchronous/asynchronous read mode and the valid clock edge configuration.

Two bus write cycles are required to issue the Set Burst Configuration Register command. The first cycle writes the setup command and the address corresponding to the set burst configuration register content. The second cycle writes the burst configuration register data and the confirm command. Once the command is issued the memory returns to read mode as if a Read Memory Array command had been issued.

The value for the burst configuration register is always presented on A0-A15. M0 is on A0, M1 on A1, etc.; the other address bits are ignored.

Table 9. Commands(1)

Command	Cycles	Bus operations					
		1st cycle			2nd cycle		
		Op.	Addr.	Data	Op.	Addr.	Data
Read Memory Array	≥ 2	Write	X	FFh	Read	RA	RD
Read Electronic Signature (manufacturer code)	≥ 2	Write	X	90h	Read	00000h	20h
Read Electronic Signature (device code)	≥ 2	Write	X	90h	Read	00001h	IDh
Read Electronic Signature (burst configuration register)	≥ 2	Write	X	90h	Read	00005h	BCRh
Read Status Register	2	Write	X	70h	Read	X	SRDh
Read Query	≥ 2	Write	X	98h	Read	QAh	QDh
Clear Status Register	1	Write	X	50h			
Block Erase	2	Write	X	20h	Write	BAh	D0h
Program	2	Write	X	40h 10h	Write	PA	PD
Program/Erase Suspend	1	Write	X	B0h			
Program/Erase Resume	1	Write	X	D0h			
Set Burst Configuration Register	2	Write	X	60h	Write	BCRh	03h

1. X = Don't care; RA = Read Address, RD = Read Data, ID = Device Code, SRD = Status Register Data, PA = Program Address; PD = Program Data, QA = Query Address, QD = Query Data, BA = Any address in the Block, BCR = Burst Configuration Register value.

Table 10. Program, erase times and program, erase endurance cycles(1)

Parameters	M58BW016					Unit
	Min	Typ		Max		
		$V_{PP} = V_{DD}$	V_{PP} = 12 V	$V_{PP} = V_{DD}$	V_{PP} = 12 V	
Parameter Block (64 Kbits) Program		0.030	0.016	0.060	0.032	s
Main Block (512 Kbits) Program		0.23	0.13	0.46	0.26	s
Parameter Block Erase		0.8	0.64	1.8	1.5	s
Main Block Erase		1.5	0.9	3	1.8	s
Program Suspend Latency time		3		10		µs
Erase Suspend Latency time		10		30		µs
Program/Erase cycles (per block)	100,000					cycles

1. T_A = –40 to 125 °C, V_{DD} = 2.7 V to 3.6 V, V_{DDQ} = 2.4 V to V_{DD}.

5 Status register

The Status register provides information on the current or previous program or erase operation. The various bits in the status register convey information and errors on the operation. They are output on DQ7-DQ0.

To read the status register the Read Status Register command can be issued. The status register is automatically read after Program, Erase or Program/Erase Resume commands. The status register can be read from any address.

The contents of the status register can be updated during an erase or program operation by toggling the Output Enable or Output Disable pins or by deactivating (Chip Enable, V_{IH}) and then reactivating (Chip Enable and Output Enable, V_{IL}, and Output Disable, V_{IH}.) the device.

The status register bits are summarized in *Table 11: Status register bits*. Refer to *Table 11* in conjunction with the following text descriptions.

5.1 Program/erase controller status (bit 7)

The Program/erase controller status bit indicates whether the program/erase controller is active or inactive. When the program/erase controller status bit is set to ‘0’, the program/erase controller is active; when bit7 is set to ‘1’, the program/erase controller is inactive.

The program/erase controller status is set to ‘0’ immediately after a Program/Erase Suspend command is issued until the program/erase controller pauses. After the program/erase controller pauses the bit is set to ‘1’.

During program and erase operations the program/erase controller status bit can be polled to find the end of the operation. The other bits in the status register should not be tested until the program/erase controller completes the operation and the bit is set to ‘1’.

After the program/erase controller completes its operation the erase status (bit5), program status bits should be tested for errors.

5.2 Erase suspend status (bit 6)

The erase suspend status bit indicates that an erase operation has been suspended and is waiting to be resumed. The erase suspend status should only be considered valid when the program/erase controller status bit is set to ‘1’ (program/erase controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the suspend mode.

When the erase suspend status bit is set to ‘0’, the program/erase controller is active or has completed its operation; when the bit is set to ‘1’, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the erase suspend status bit returns to ‘0’.

5.3 Erase status (bit 5)

The erase status bit can be used to identify if the memory has failed to verify that the block has erased correctly. The erase status bit should be read once the program/erase controller status bit is High (program/erase controller inactive).

When the erase status bit is set to ‘0’, the memory has successfully verified that the block has erased correctly. When the erase status bit is set to ‘1’, the program/erase controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly.

Once set to ‘1’, the erase status bit can only be reset to ‘0’ by a Clear Status Register command or a hardware reset. If set to ‘1’ it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

5.4 Program status (bit 4)

The program status bit is used to identify a program failure. Bit4 should be read once the program/erase controller status bit is High (program/erase controller inactive).

When bit4 is set to ‘0’ the memory has successfully verified that the device has programmed correctly. When bit4 is set to ‘1’ the device has failed to verify that the data has been programmed correctly.

Once set to 1’, the program status bit can only be reset to ‘0’ by a Clear Status Register command or a hardware reset. If set to ‘1’ it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

5.5 V_{PP} status (bit 3)

The V_{PP} status bit can be used to identify an invalid voltage on the V_{PP} pin during fast program and erase operations. The V_{PP} pin is only sampled at the beginning of a program or erase operation. Indeterminate results can occur if V_{PP} becomes invalid during a fast program or erase operation.

When the V_{PP} status bit is set to ‘0’, the voltage on the V_{PP} pin was sampled at a valid voltage; when the V_{PP} status bit is set to ‘1’, the V_{PP} pin has a voltage that is below the V_{PP} lockout voltage, V_{PPLK}.

Once set to ‘1’, the V_{PP} status bit can only be reset to ‘0’ by a Clear Status Register command or a hardware reset. If set to ‘1’ it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

5.6 Program suspend status (bit 2)

The program suspend status bit indicates that a program operation has been suspended and is waiting to be resumed. The program suspend status should only be considered valid when the program/erase controller status bit is set to ‘1’ (program/erase controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the suspend mode.

When the program suspend status bit is set to ‘0’, the program/erase controller is active or has completed its operation; when the bit is set to ‘1’, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the program suspend status bit returns to ‘0’.

5.7 Block protection status (bit 1)

The block protection status bit can be used to identify if a program or erase operation has tried to modify the contents of a protected block.

When the block protection status bit is set to ‘0’, no program or erase operations have been attempted to protected blocks since the last Clear Status Register command or hardware reset; when the block protection status bit is set to ‘1’, a program or erase operation has been attempted on a protected block.

Once set to ‘1’, the block protection status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set to ‘1’ it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

All others bits are reserved.

Table 11. Status register bits

Bit	Name	Logic level	Definition
7	Program/erase controller status	’1’	Ready
		’0’	Busy
6	Erase suspend status	’1’	Suspended
		’0’	In progress or completed
5	Erase status	’1’	Erase error
		’0’	Erase success
4	Program status,	’1’	Program error
		’0’	Program success
3	V_{PP} status	’1’	V_{PP} invalid, abort
		’0’	V_{PP} OK
2	Program suspend status	’1’	Suspended
		’0’	In progress or completed
1	Erase/program in a protected block	’1’	Program/erase on protected block, abort
		’0’	No operations to protected sectors
Other bits reserved			

6 Maximum ratings

Stressing the device above the ratings listed in *Table 12: Absolute maximum ratings*, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the Numonyx SURE Program and other relevant quality documents.

Table 12. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature under bias	–40	125	°C
T_{STG}	Storage temperature	–55	155	°C
V_{IO}	Input or output voltage	–0.6	V_{DDQ} + 0.6 V_{DDQIN} + 0.6	V
V_{DD}, V_{DDQ}, V_{DDQIN}	Supply voltage	–0.6	4.2	V
V_{PP}	Program voltage	–0.6	13.5(1)	V

1. Cumulative time at a high voltage level of 13.5 V should not exceed 80 hours on V_{PP} pin.

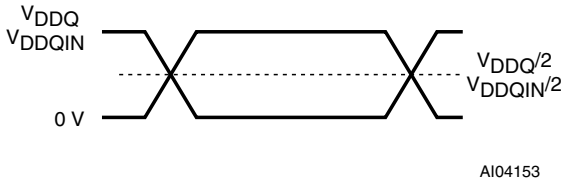
7 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 13: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 13. Operating and AC measurement conditions

Parameter		Value		Units
		Min	Max	
Supply voltage (V_{DD})		2.7	3.6	V
Input/output supply voltage (V_{DDQ})		2.4	V_{DD}	V
Ambient temperature (T_A)	Grade 6	–40	90	°C
	Grade 3	–40	125	°C
Load capacitance (C_L)		30		pF
Clock rise and fall times			4	ns
Input rise and fall times			4	ns
Input pulses voltages		0 to V_{DDQ}		V
Input and output timing ref. voltages		$V_{DDQ}/2$		V

Figure 6. AC measurement input/output waveform



1. $V_{DD} = V_{DDQ}$.

Figure 7. AC measurement load circuit

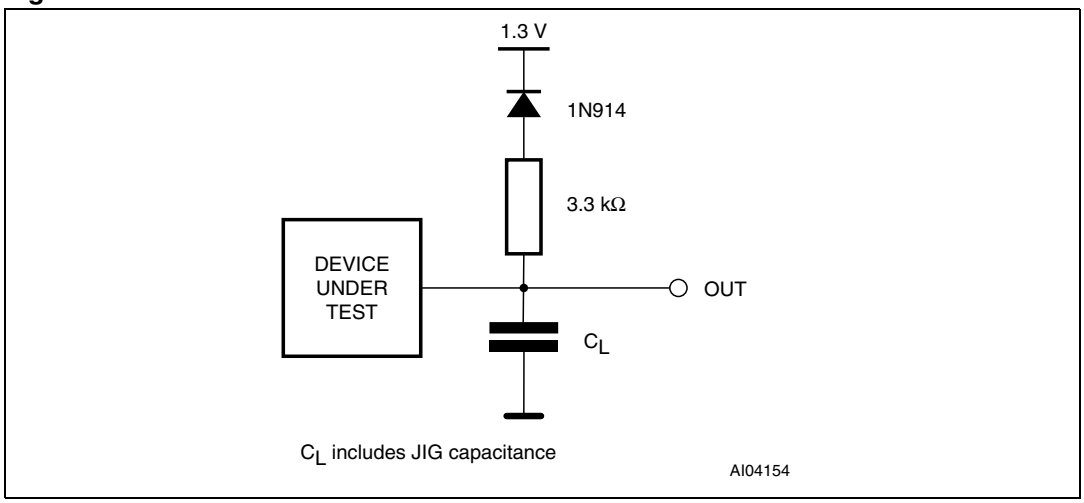


Table 14. Device capacitance(1)(2)

Symbol	Parameter	Test condition	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V	6	8	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	8	12	pF

1. T_A = 25 °C, f = 1 MHz.
2. Sampled only, not 100% tested.

Table 15. DC characteristics

Symbol	Parameter	Test condition		Min	Max	Unit
I_{LI}	Input Leakage current	0 V≤V_{IN} ≤V_{DDQ}			±1	µA
I_{LO}	Output Leakage current	0 V≤V_{OUT} ≤V_{DDQ}			±5	µA
I_{DD}	Supply current (Random Read)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, f_{add} = 6 MHz	M58BW016DT/B		20	mA
			M58BW016FT/B		25	
I_{DDP-UP}(1)	Supply current (Power-up)	$\overline{E}$ = V_{IH}	applies only to M58BW016FT/B		20	mA
I_{DDB}	Supply current (Burst Read)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, f_{clock} = 40 MHz	M58BW016DT/B		30	mA
			M58BW016FT/B			
		$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, f_{clock} = 56 MHz	M58BW016DT/B		30	mA
			M58BW016FT/B		40	mA
I_{DD1}	Supply current (Standby)	$\overline{E}$ = $\overline{RP}$ = V_{DD} ± 0.2 V	M58BW016DT/B		60	µA
			M58BW016FT/B		150	µA
	Supply current (Auto Low-Power)	$\overline{E}$ = V_{SS} ± 0.2 V, $\overline{RP}$ = V_{DD} ± 0.2 V			60	µA
I_{DD2}	Supply current (Reset/Power-down)	$\overline{RP}$ = V_{SS} ± 0.2 V			60	µA
I_{DD3}	Supply current (Program or Erase, Set Lock bit, Erase Lock bit)	Program, Block Erase in progress			30	mA
I_{DD4}	Supply current (Erase/Program Suspend)	$\overline{E}$ = V_{IH}	M58BW016DT/B		40	µA
			M58BW016FT/B		150	µA
I_{PP}	Program current (Read or Standby)	V_{PP} ≥ V_{PP1}			± 30	µA
I_{PP1}	Program current (Read or Standby)	V_{PP} ≤V_{PP1}			± 30	µA
I_{PP2}	Program current (Power-down)	$\overline{RP}$ = V_{IL}			± 5	µA
I_{PP3}	Program current (Program) Program in progress	V_{PP} = V_{PP1}			200	µA
		V_{PP} = V_{PPH}			20	mA
I_{PP4}	Program current (Erase) Erase in progress	V_{PP} = V_{PP1}			200	µA
		V_{PP} = V_{PPH}			20	mA
V_{IL}	Input Low voltage			–0.5	0.2V_{DDQIN}	V
V_{IH}	Input High voltage (for DQ lines)			0.8V_{DDQIN}	V_{DDQ}+0.3	V
V_{IH}	Input High voltage (for input only lines)			0.8V_{DDQIN}	3.6	V
V_{OL}	Output Low voltage	I_{OL} = 100 µA			0.1	V
V_{OH}	Output High voltage CMOS	I_{OH} = –100 µA		V_{DDQ}–0.1		V
V_{PP1}	Program voltage (program or erase operations)			2.7	3.6	V
V_{PPH}	Program voltage (program or erase operations)			11.4	12.6	V
V_{LKO}	V_{DD} supply voltage (erase and program lockout)				2.2	V
V_{PPLK}	V_{PP} supply voltage (erase and program lockout)				11.4	V

1. I_{DDP-UP} is defined only during the power-up phase of the M58BW016FT/B, from the moment current is applied with $\overline{RP}$ Low to the moment when the supply voltage has become stable and $\overline{RP}$ is brought to High.

Figure 8. Asynchronous bus read AC waveforms

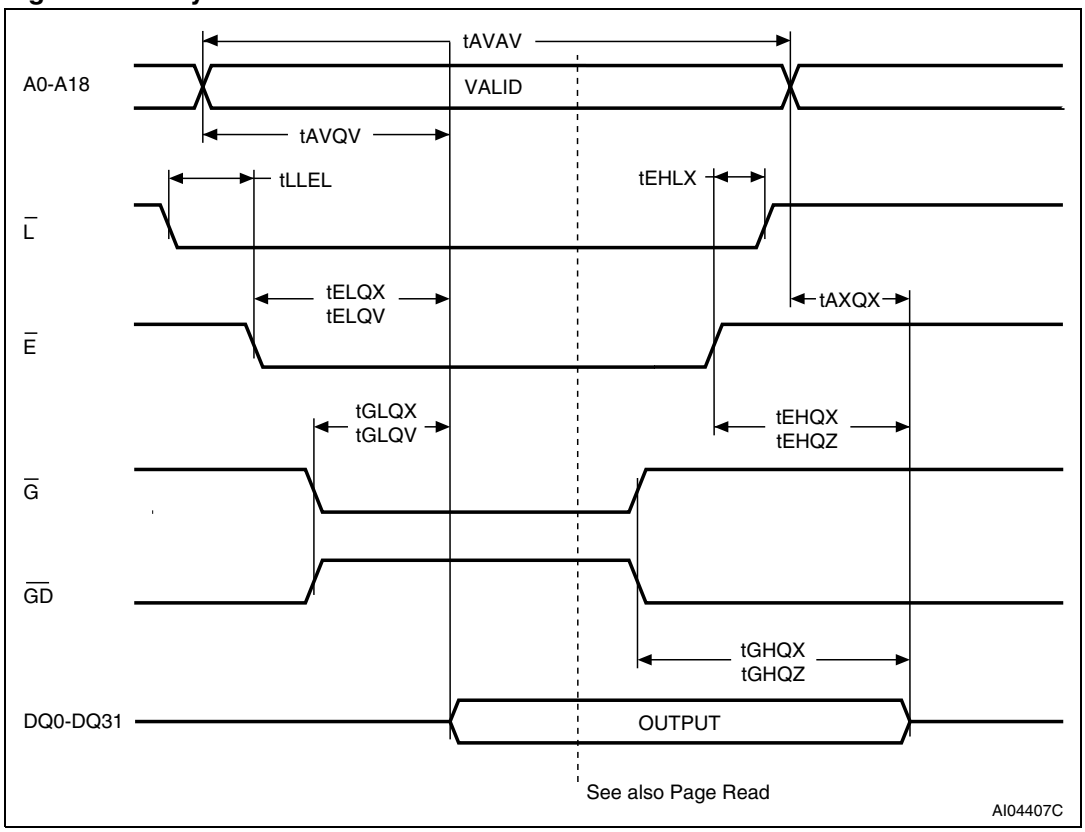


Table 16. Asynchronous bus read AC characteristics

Symbol	Parameter	Test condition		M58BW016		Unit
				70	80	
t_{AVAV}	Address Valid to Address Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	70	80	ns
t_{AVQV}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	70	80	ns
t_{AXQX}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	0	0	ns
t_{EHLX}	Chip Enable High to Latch Enable Transition		Min	0	0	ns
t_{EHQX}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	ns
t_{EHQZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	Max	20	20	ns
t_{ELQV}(1)	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$	Max	70	80	ns
t_{ELQX}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	ns
t_{GHQX}	Output Enable High to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{GHQZ}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	Max	15	15	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	25	25	ns
t_{GLQX}	Output Enable to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{LLEL}	Latch Enable Low to Chip Enable Low		Min	0	0	ns

1. Output Enable $\overline{G}$ may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of Chip Enable $\overline{E}$ without increasing t_{ELQV}.

Figure 9. Asynchronous latch controlled bus read AC waveforms

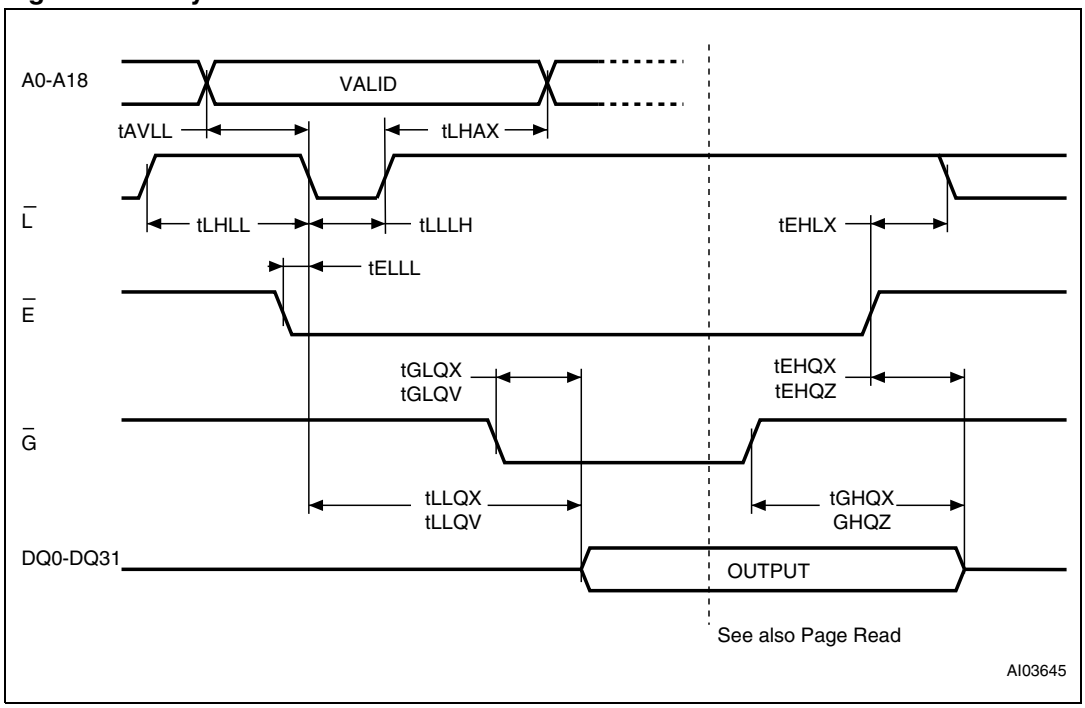


Table 17. Asynchronous latch controlled bus read AC characteristics

Symbol	Parameter	Test condition		M58BW016		Unit
				70	80	
t_{AVLL}	Address Valid to Latch Enable Low	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{EHLX}	Chip Enable High to Latch Enable Transition		Min	0	0	ns
t_{EHQX}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	ns
t_{EHQZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	Max	20	20	ns
t_{ELLL}	Chip Enable Low to Latch Enable Low		Min	0	0	ns
t_{GHQX}	Output Enable High to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{GHQZ}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	Max	15	15	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	25	25	ns
t_{GLQX}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{LHAX}	Latch Enable High to Address Transition	$\overline{E} = V_{IL}$	Min	5	5	ns
t_{LHLL}	Latch Enable High to Latch Enable Low		Min	10	10	ns
t_{LLLH}	Latch Enable Low to Latch Enable High	$\overline{E} = V_{IL}$	Min	10	10	ns
t_{LLQV}	Latch Enable Low to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	70	80	ns
t_{LLQX}	Latch Enable Low to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	0	0	ns

Figure 10. Asynchronous page read AC waveforms

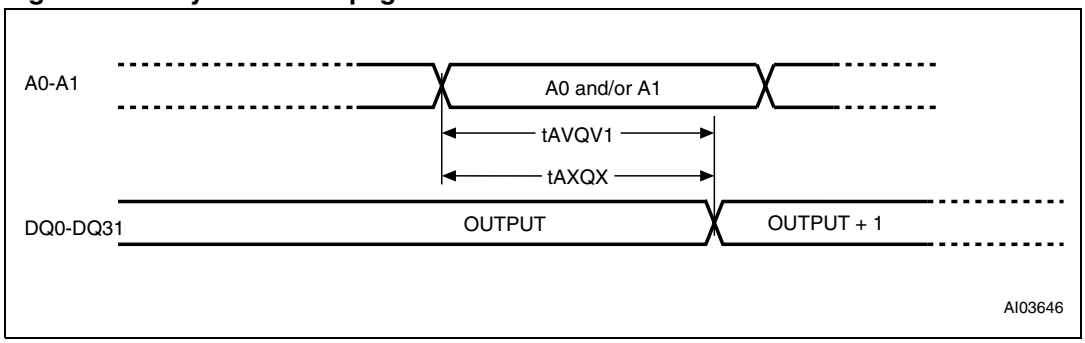


Table 18. Asynchronous page read AC characteristics(1)

Symbol	Parameter	Test condition		M58BW016		Unit
				70	80	
t_{AVQV1}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	25	25	ns
t_{AXQX}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	6	6	ns

1. For other timings see *Table 16: Asynchronous bus read AC characteristics*.

Figure 11. Asynchronous write AC waveforms

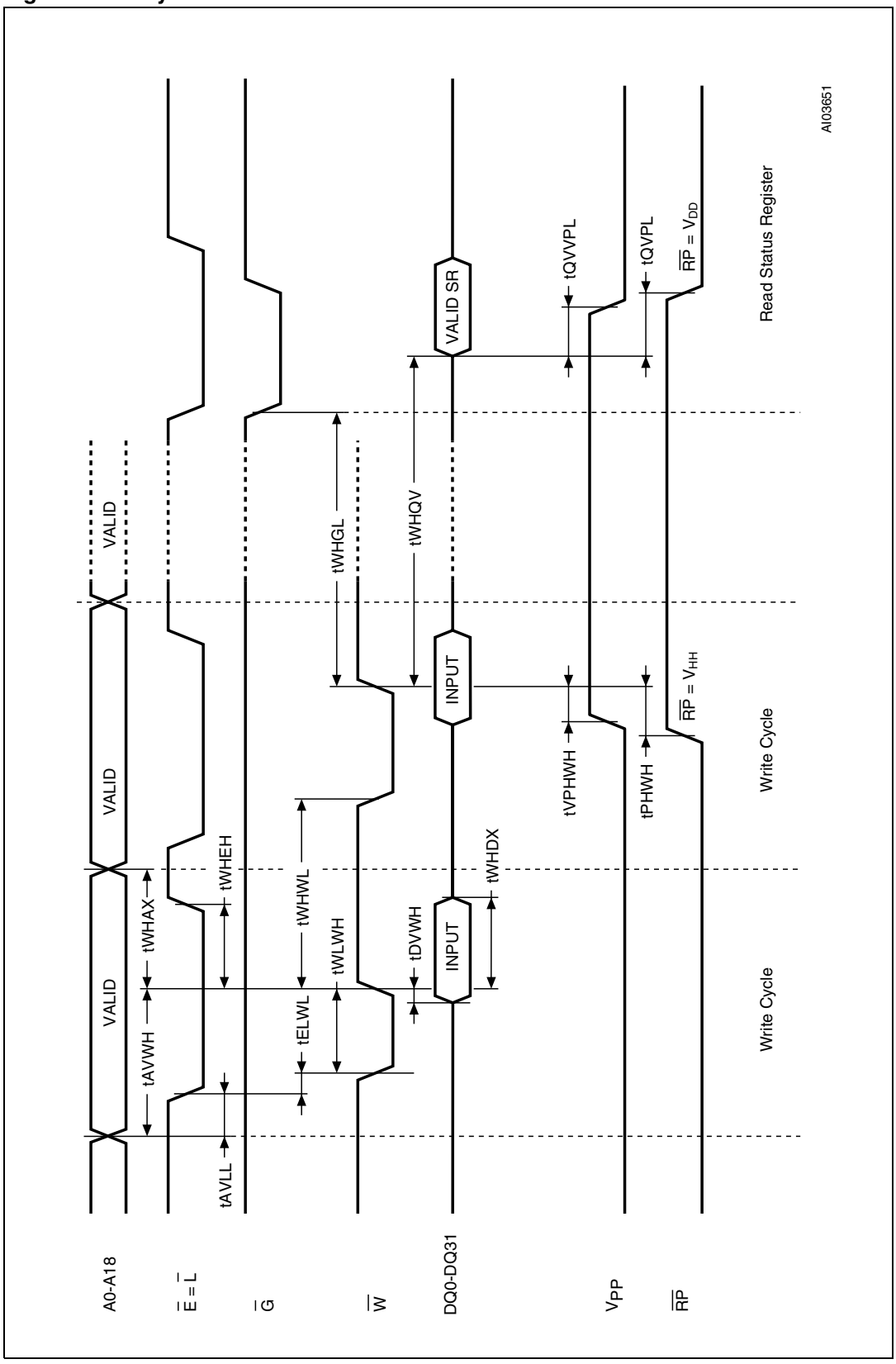


Figure 12. Asynchronous latch controlled write AC waveforms

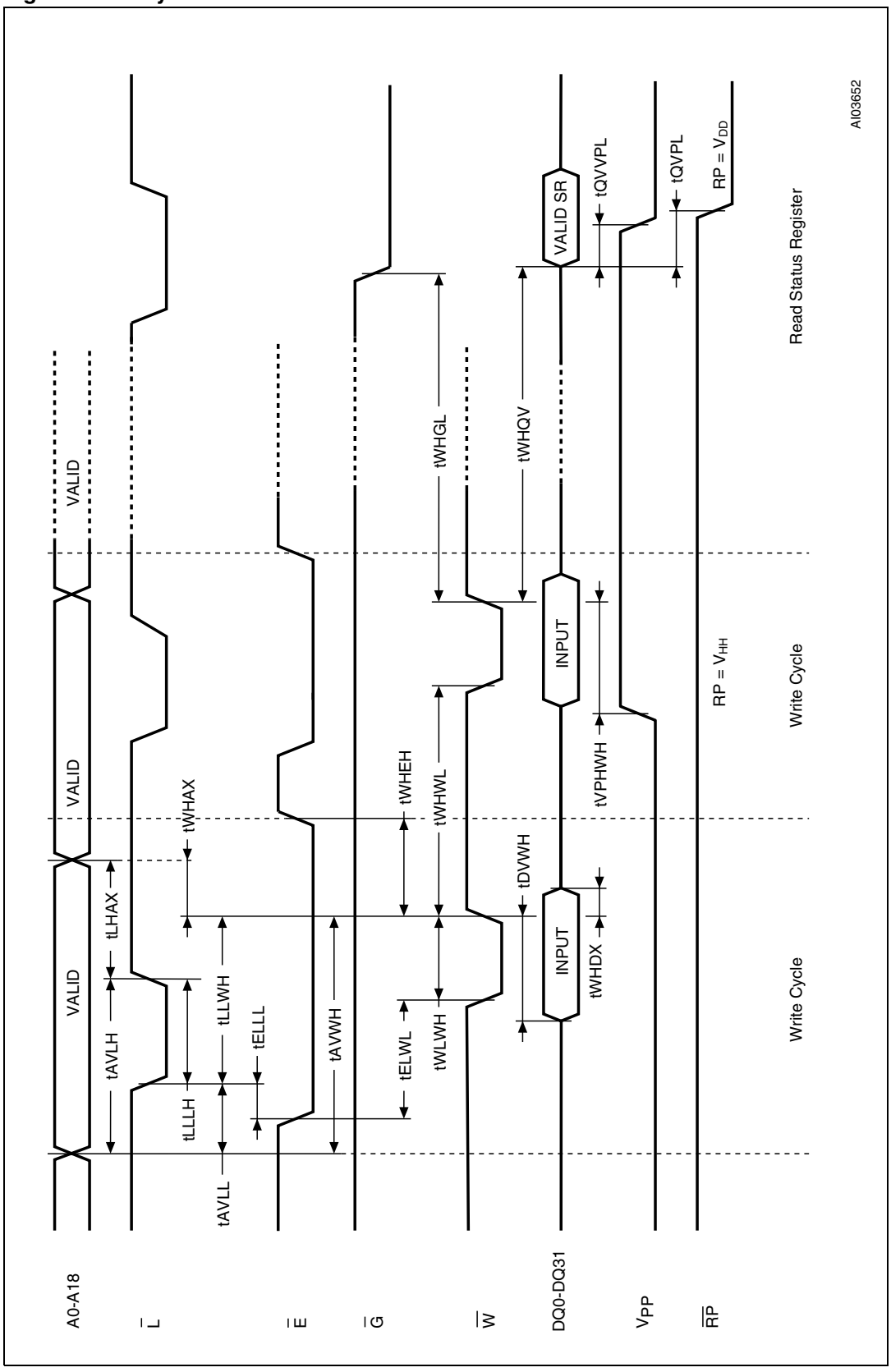
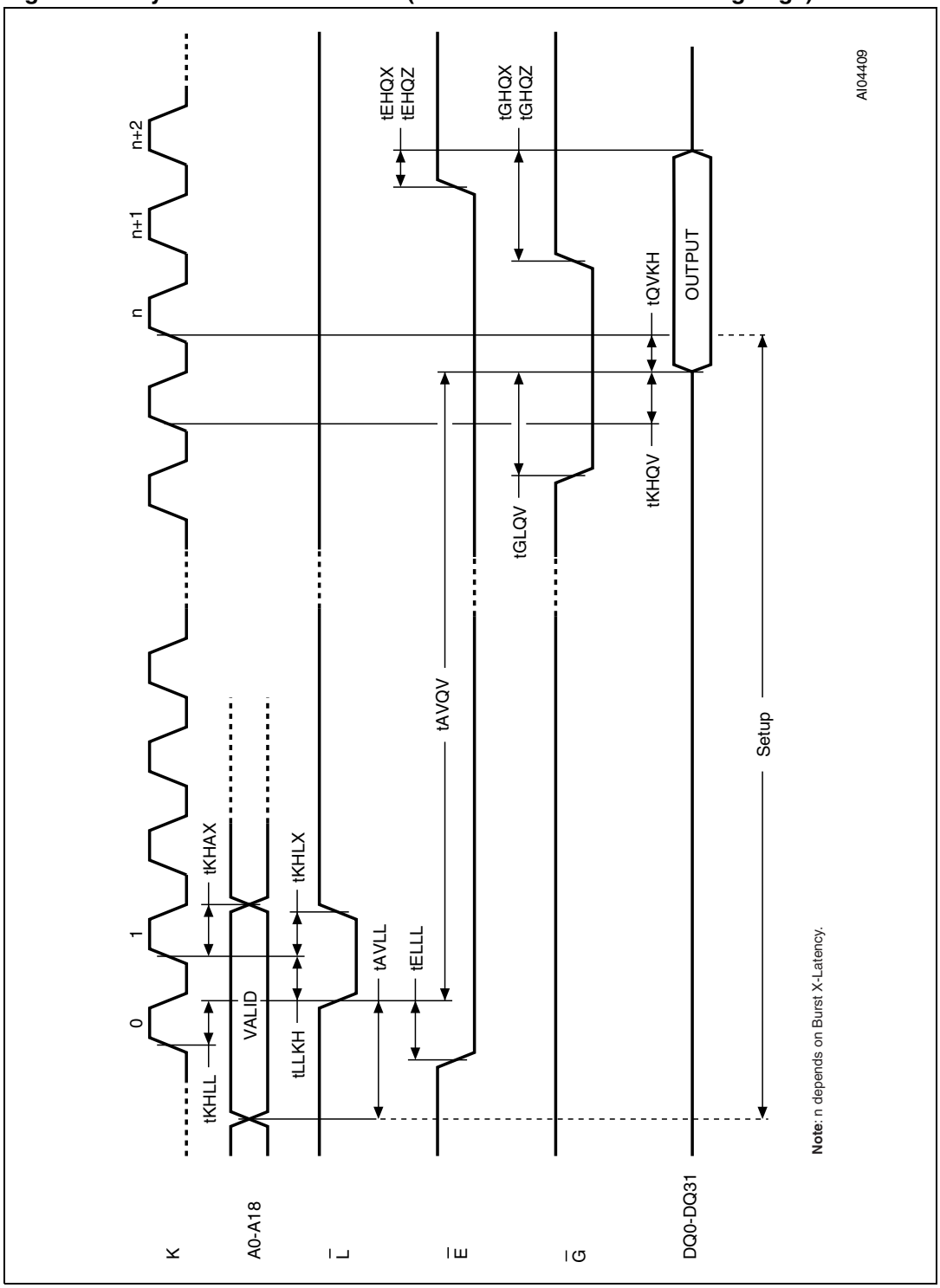


Table 19. Asynchronous write and latch controlled write AC characteristics

Symbol	Parameter	Test condition		M58BW016		Unit
				70	80	
t_{AVLL}	Address Valid to Latch Enable Low		Min	0	0	ns
t_{AVWH}	Address Valid to Write Enable High	$\overline{E} = V_{IL}$	Min	50	50	ns
t_{DVWH}	Data Input Valid to Write Enable High	$\overline{E} = V_{IL}$	Min	50	50	ns
t_{ELLL}	Chip Enable Low to Latch Enable Low		Min	0	0	ns
t_{ELWL}	Chip Enable Low to Write Enable Low		Min	0	0	ns
t_{LHAX}	Latch Enable High to Address Transition		Min	5	5	ns
t_{LLLH}	Latch Enable Low to Latch Enable High		Min	10	10	ns
t_{LLWH}	latch Enable Low to Write Enable High	$\overline{E} = V_{IL}$	Min	50	50	ns
t_{QVVPL}	Output Valid to V_{PP} Low		Min	0	0	ns
t_{VPHWH}	V_{PP} High to Write Enable High		Min	0	0	ns
t_{WHAX}	Write Enable High to Address Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{WHDX}	Write Enable High to Input Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{WHEH}	Write Enable High to Chip Enable High		Min	0	0	ns
t_{WHGL}	Write Enable High to Output Enable Low		Min	150	150	ns
t_{WHQV}	Write Enable High to Output Valid		Min	175	175	ns
t_{WHWL}	Write Enable High to Write Enable Low		Min	20	20	ns
t_{WLWH}	Write Enable Low to Write Enable High	$\overline{E} = V_{IL}$	Min	60	60	ns
t_{QVPL}	Output Valid to Reset/Power-down Low		Min	0	0	ns

Figure 13. Synchronous burst read (data valid from 'n' clock rising edge)



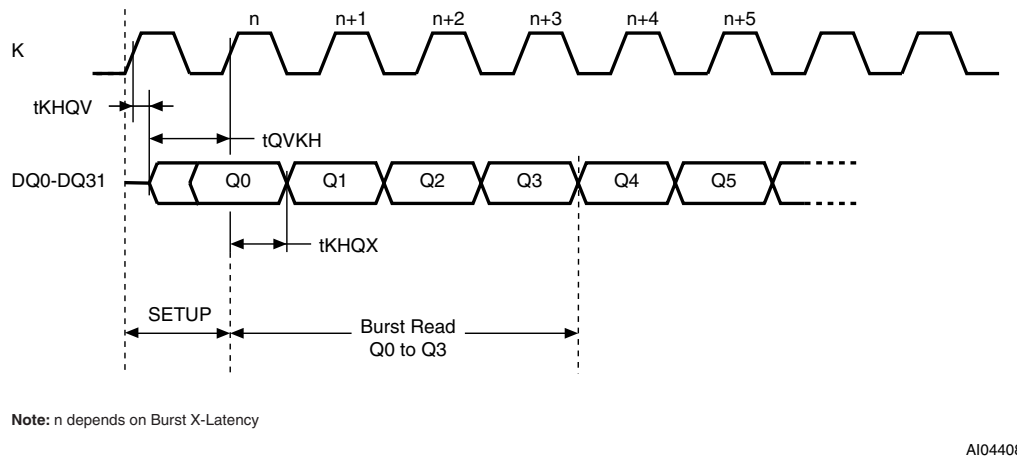
1. The M58BW016F first data output is synchronized with the clock's active edge, while the M58BW016D first data output is not synchronized with the clock's active edge.
2. In the M58BW016F devices the right access time depends on the clock frequency.
3. For further details, please refer to the section 3.2 Clock signal in burst mode in the application note AN2461.

Table 20. Synchronous burst read AC characteristics(1)

Symbol	Parameter	Test condition			M58BW016		Unit
					70	80	
t_{AVLL}	Address Valid to Latch Enable Low	$\overline{E} = V_{IL}$		Min	0	0	ns
t_{BHKH}	Burst Address Advance High to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$		Min	8	8	ns
t_{BLKH}	Burst Address Advance Low to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$		Min	8	8	ns
t_{ELLL}	Chip Enable Low to Latch Enable Low			Min	0	0	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$, $\overline{L} = V_{IH}$		Min	25	25	ns
t_{KHAX}	Valid Clock Edge to Address Transition	$\overline{E} = V_{IL}$		Min	5	5	ns
t_{KHLL}	Valid Clock Edge to Latch Enable Low	$\overline{E} = V_{IL}$		Min	0	0	ns
t_{KHLX}	Valid Clock Edge to Latch Enable Transition	$\overline{E} = V_{IL}$		Min	0	0	ns
t_{KHQX}	Valid Clock Edge to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	M58BW016DT/B	Min	3	3	ns
			M58BW016FT/B	Min	2	2	ns
t_{LLKH}	Latch Enable Low to Valid Clock Edge	$\overline{E} = V_{IL}$	M58BW016DT/B	Min	6	6	ns
			M58BW016FT/B	Min	5	5	ns
t_{QVKH}(2)	Output Valid to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$		Min	6	6	ns
t_{RLKH}	Valid Data Ready Low to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$		Min	6	6	ns
t_{KHQV}	Valid Clock Edge to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$		Max	11	11	ns

1. For other timings see *Table 16: Asynchronous bus read AC characteristics*.
2. Data output should be read on the valid clock edge.

Figure 14. Synchronous burst read (data valid from 'n' clock rising edge)



Note: n depends on Burst X-Latency

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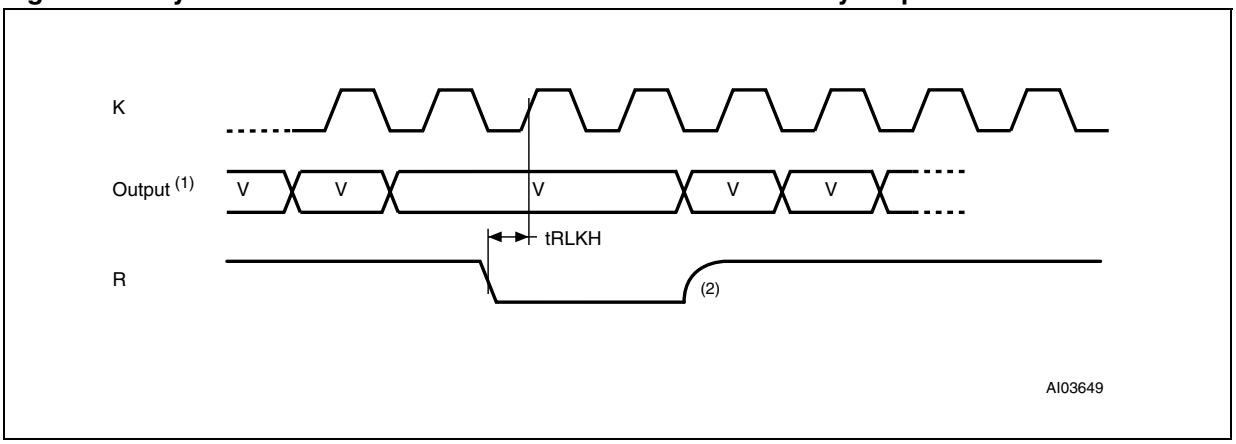
1. For set up signals and timings see synchronous burst read.

Figure 15. Synchronous burst read - continuous - valid data ready output



1. Valid Data Ready = Valid Low during valid clock edge.
2. V= Valid output.
3. R is an open drain output with an internal pull up resistor of 1 MΩ. The internal timing of R follows DQ. An external resistor, typically 300 kΩ for a single memory on the R bus, should be used to give the data valid set up time required to recognize that valid data is available on the next valid clock edge.

Figure 16. Synchronous burst read - burst address advance

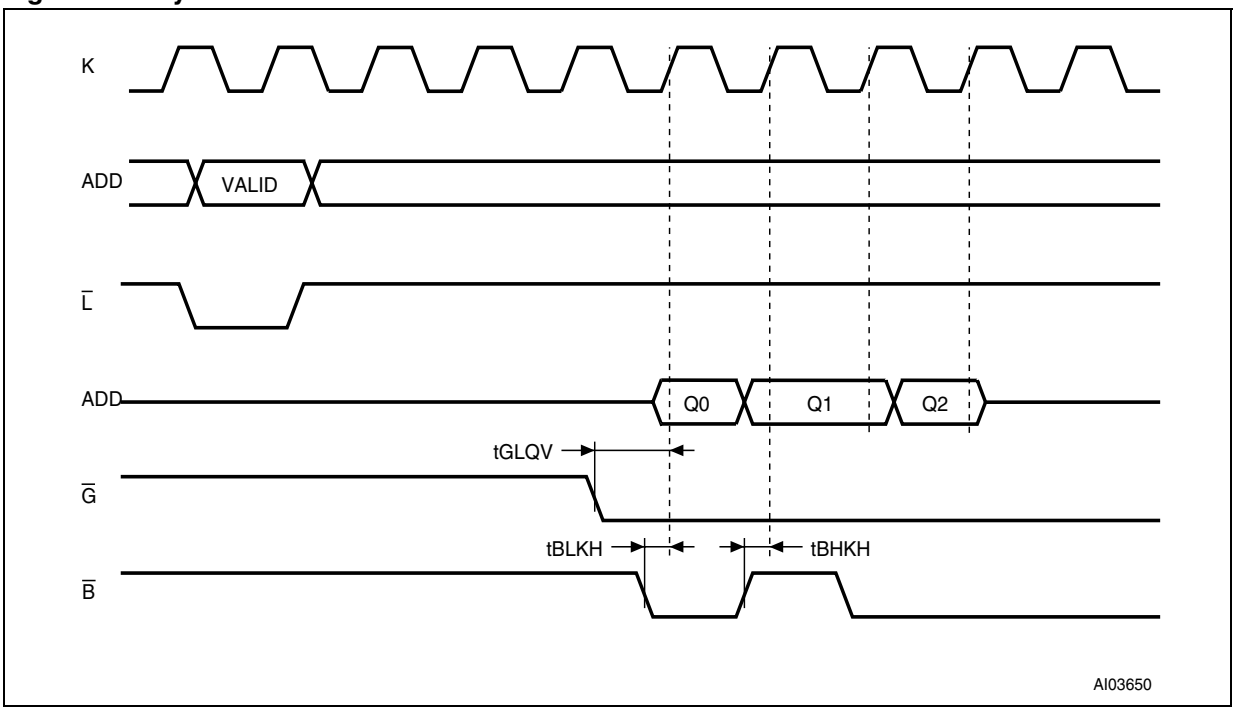


Figure 17. Reset, power-down and power-up AC waveforms - control pins low

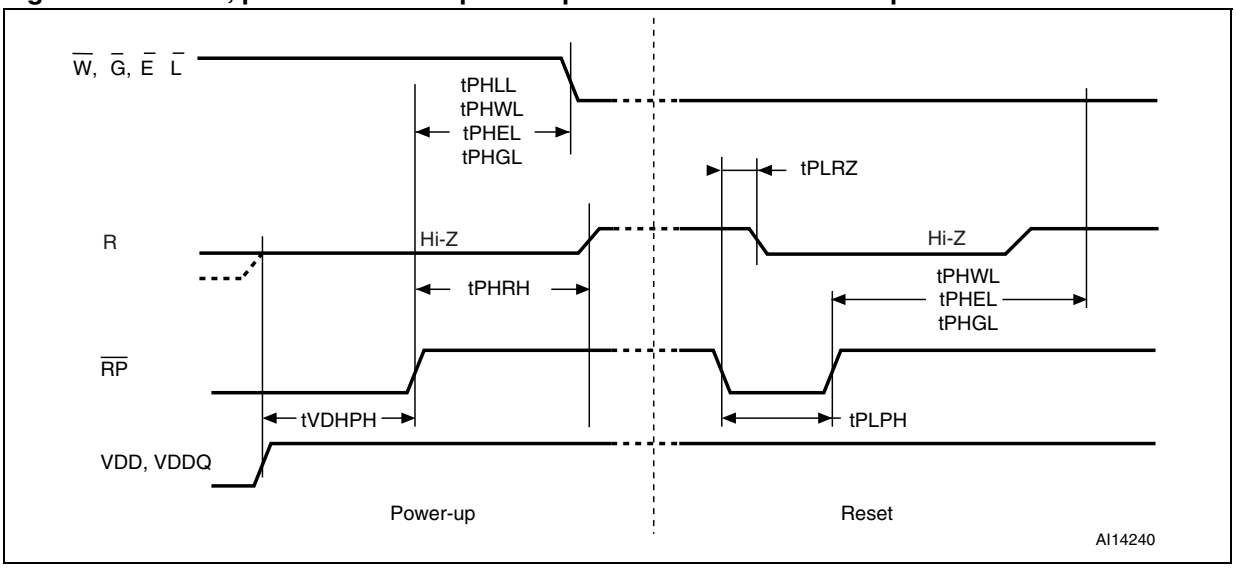


Figure 18. Reset, power-down and power-up AC waveforms - control pins toggling

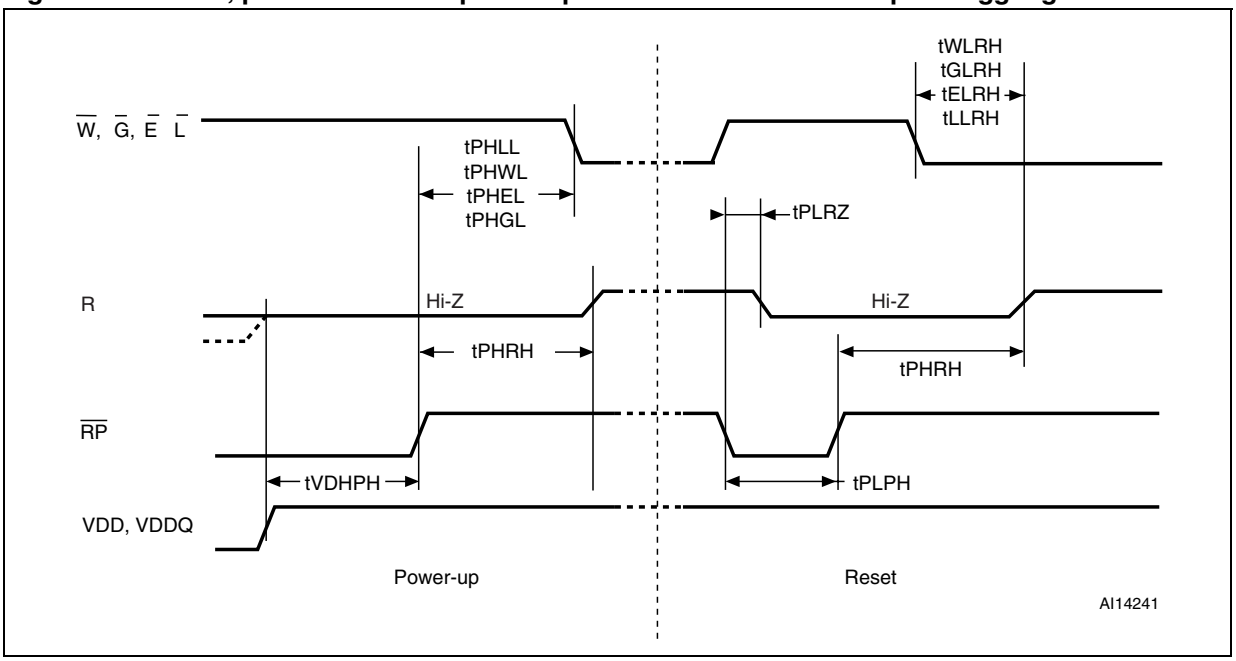
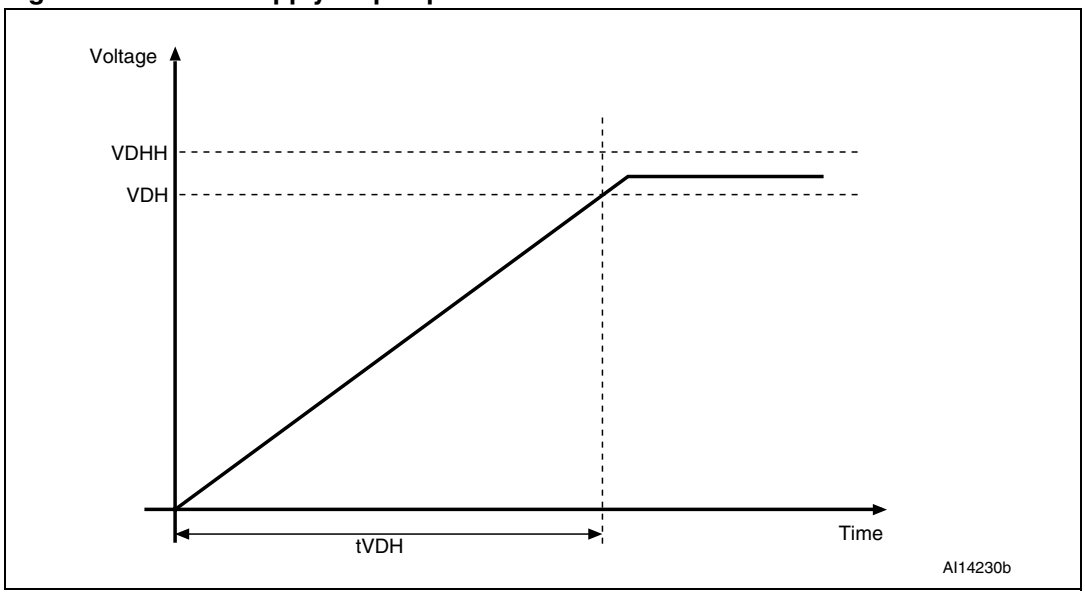


Figure 19. Power supply slope specification



1. Please refer to the application note AN2601.

Table 21. Power supply AC and DC characteristics

Symbol	Description	Min	Max	Unit
V_{DH}	Minimum value of power supply	2.7		V
V_{DHH}	Maximum value of power supply		3.6	V
t_{VDH}	Time required from power supply to reach the V_{DH} value	300	50000	µs

Table 22. Reset, power-down and power-up AC characteristics

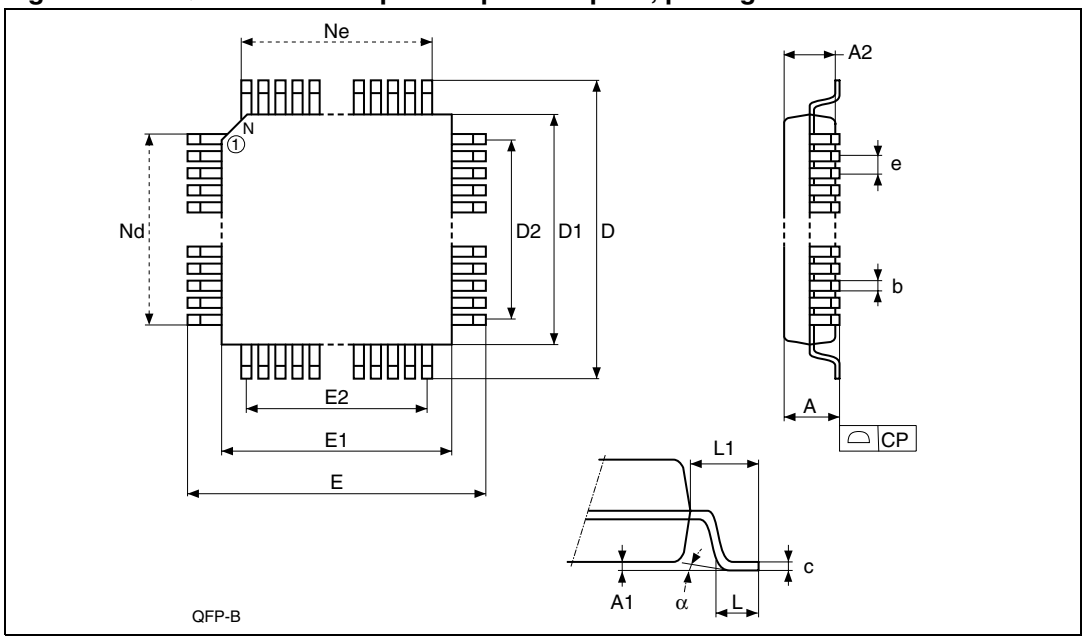
Symbol	Parameter		Min	Max	Unit
t_{PHEL}	Reset/Power-down High to Chip Enable Low		50		ns
t_{PHLL}	Reset/Power-down High to Latch Enable Low		50		ns
t_{PHQV}(1)	Reset/Power-down High to Output Valid			95	ns
t_{PHWL}	Reset/Power-down High to Write Enable Low		50		ns
t_{PHGL}	Reset/Power-down High to Output Enable Low		50		ns
t_{PLPH}	Reset/Power-down Low to Reset/Power-down High		100		ns
t_{PHRH}(1)	Reset/Power-down High to Valid Data Ready High			95	
t_{VDHPH}	Supply voltages High to Reset/Power-down High	M58BW016DT/B	10		µs
		M58BW016FT/B	50		µs
t_{PLRZ}	Reset/Power-down Low to Data Ready High Impedance			80	ns
t_{WLRH}	Write Enable Low to Data Ready High Impedance			80	ns
t_{GLRH}	Output Enable Low to Data Ready High Impedance			80	ns
t_{ELRH}	Chip Enable Low to Data Ready High Impedance			80	ns
t_{LLRH}	Latch Enable Low to Data Ready High Impedance			80	ns

1. This time is $t_{PHEL} + t_{AVQV}$ or $t_{PHEL} + t_{ELQV}$.

8 Package mechanical

In order to meet environmental requirements, Numonyx offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 20. PQFP80 - 80 lead plastic quad flat pack, package outline

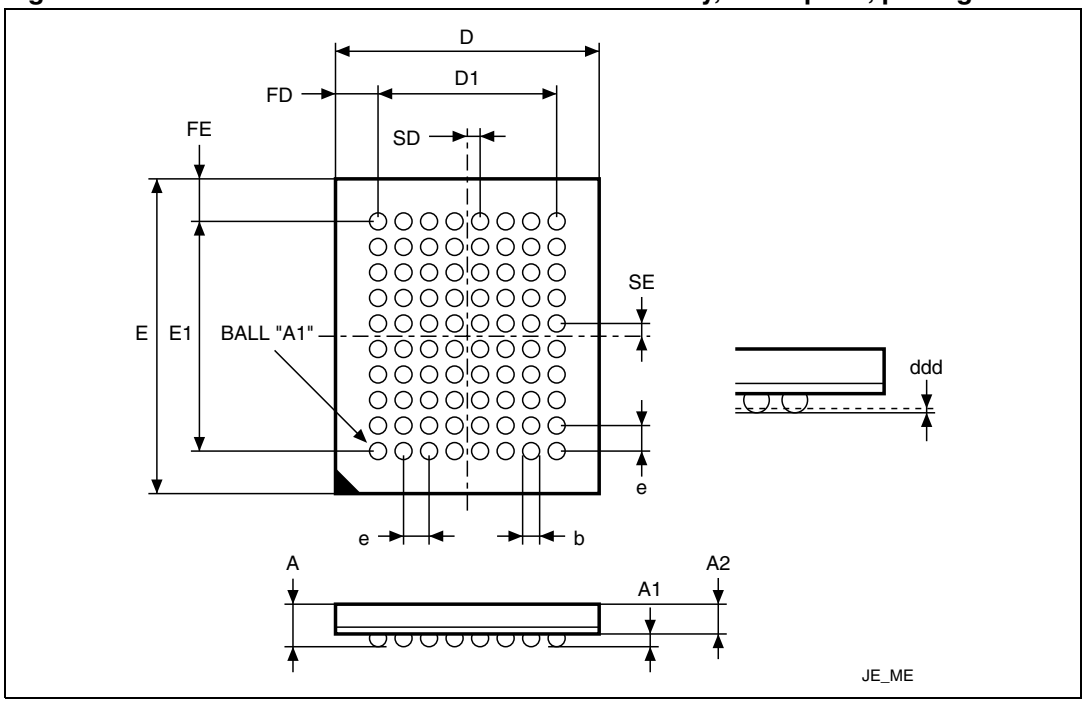


1. Drawing is not to scale.

Table 23. PQFP80 - 80 lead plastic quad flat pack, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.40			0.134
A1		0.25			0.010	
A2	2.80	2.55	3.05	0.110	0.100	0.120
b		0.30	0.45		0.012	0.018
c		0.13	0.23		0.005	0.009
D	23.20	22.95	23.45	0.913	0.903	0.923
D1	20.00	19.90	20.10	0.787	0.783	0.791
D2	18.40	–	–	0.724	–	–
e	0.80	–	–	0.031	–	–
E	17.20	16.95	17.45	0.677	0.667	0.687
E1	14.00	13.90	14.10	0.551	0.547	0.555
E2	12.00	–	–	0.472	–	–
L	0.80	0.65	0.95	0.031	0.026	0.037
L1	1.60	–	–	0.063	–	–
a		0°	7°		0°	7°
N	80			80		
Nd	24			24		
Ne	16			16		

Figure 21. LBGA80 10 × 12 mm - 8 × 10 active ball array, 1 mm pitch, package outline



1. Drawing is not to scale.

Table 24. LBGA80 10 × 12 mm - 8 × 10 active ball array, 1 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.60			0.063
A1		0.40			0.016	
A2			1.05			0.041
b	0.60			0.024		
D	10.00	–	–	0.394	–	–
D1	7.00	–	–	0.276	–	–
ddd			0.15			0.006
E	12.00	–	–	0.472	–	–
E1	9.00	–	–	0.354	–	–
e	1.00			0.039		
FD	1.50	–	–	0.059	–	–
FE	1.50	–	–	0.059	–	–
SD	0.50			0.020		
SE	0.50			0.020		

9 Ordering information

Table 25. Ordering information scheme

Example: M58 BW016D T 8 T 3 F T

Device type

M58

Architecture

B = Burst mode

Operating voltage

W = V_{DD} = 2.7 V to 3.6 V; V_{DDQ} = V_{DDQIN} = 2.4 to V_{DD}

Device function

016D = 16-Mbit (x 32), boot block, burst, 0.15 µm

016F = 16-Mbit (x 32), boot block, burst, 0.11 µm

Array matrix

T = Top boot

B = Bottom boot

Speed

7 = 70 ns

8 = 80 ns (only available in the M58BW016D devices)

Package

T = PQFP80

ZA = LBGA 10 × 12 mm

Temperature range

3 = automotive grade certified(1), –40 to 125 °C

Version

F = silicon version F (only available in the M58BW016D devices)

Option

T = Tape and reel packing

F = ECOPACK package, tape and reel packing

1. Qualified & characterized according to AEC Q100 & Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

Note: Devices are shipped from the factory with the memory content bits erased to '1'.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the Numonyx Sales Office nearest to you.

Appendix A Common Flash interface (CFI)

The common Flash interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query command (RCFI) is issued the device enters CFI query mode and the data structure is read from the memory. *Table 26*, *Table 27*, *Table 28*, *Table 29* and *Table 30* show the addresses used to retrieve the data.

Table 26. Query structure overview

Offset	Sub-section name	Description
00h		Manufacturer code
01h		Device code
10h	CFI Query identification string	Command set ID and algorithm data offset
1Bh	System interface information	Device timing and voltage information
27h	Device geometry definition	Flash memory layout
P(h)(1)	Primary algorithm-specific extended query table	Additional information specific to the primary algorithm (optional)
A(h)(2)	Alternate algorithm-specific extended query table	Additional information specific to the alternate algorithm (optional)

1. Offset 15h defines P which points to the primary algorithm extended query address table.
2. Offset 19h defines A which points to the alternate algorithm extended query address table.

Table 27. CFI - query address and data output(1)(2)

Address A0-A18	Data		Instruction
10h	51h	"Q"	51h; ‘Q’ Query ASCII String 52h; ‘R’ 59h; ‘Y’
11h	52h	"R"	
12h	59h	"Y"	
13h	03h		Primary vendor: Command set and control interface ID code
14h	00h		
15h	35h		Primary algorithm extended query address table: P(h)
16h	00h		
17h	00h		Alternate vendor: Command Set and Control interface ID code
18h	00h		
19h	00h		Alternate algorithm extended query address table
1Ah	00h		

1. The x 8 or byte address and the x 16 or word address mode are not available.
2. Query data are always presented on DQ7-DQ0. DQ31-DQ8 are set to '0'.

Table 28. CFI - device voltage and timing specification

Address A0-A18	Data	Description
1Bh	27h (1)	V_{DD} min, 2.7 V
1Ch	36h(1)	V_{DD} max, 3.6 V
1Dh	B4h(2)	V_{PP} min
1Eh	C6h(2)	V_{PP} max
1Fh	04h	2^n ms typical time-out for Word, DWord prog – not available
20h	00h	2^n ms, typical time-out for max buffer write – not available
21h	0Ah	2^n ms, typical time-out for Erase Block
22h	00h	2^n ms, typical time-out for chip erase – not available
23h-24h	Reserved	
25h	04h	2^n x typical for individual block erase time-out maximum
26h	00h	2^n x typical for chip erase max time-out – not available

1. Bits are coded in binary code decimal, bit7 to bit4 are scaled in Volts and bit3 to bit0 in mV.
2. Bit7 to bit4 are coded in hexadecimal and scaled in Volts while bit3 to bit0 are in binary code decimal and scaled in 100 mV.

Table 29. Device geometry definition

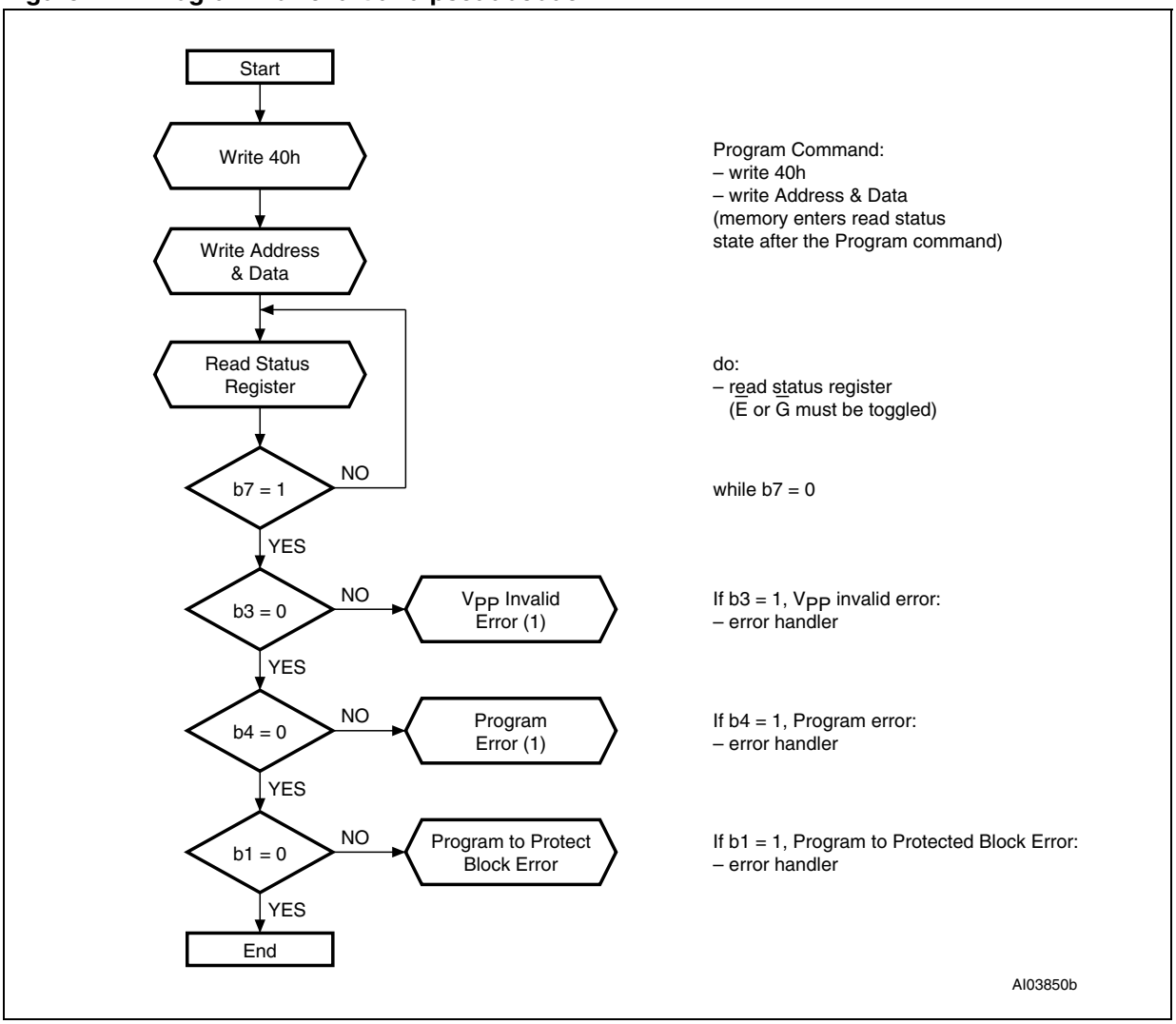
Address A0-A18	Data	Description
27h	15h	2^n number of bytes memory size
28h	03h	Device interface sync./async.
29h	00h	Organization sync./async.
2Ah	00h	Page size in bytes, 2^n
2Bh	00h	
2Ch	02h	Bit7-0 = number of erase block regions in device
2Dh	1Eh	Number (n-1) of blocks of identical size; n=31
2Eh	00h	
2Fh	00h	Erase block region information x 256 bytes per erase block (64 Kbytes)
30h	01h	
31h	07h	Number (n-1) of blocks of identical size; n=8
32h	00h	
33h	20h	Erase block region information x 256 bytes per erase block (8 Kbytes)
34h	00h	

Table 30. Extended query information

Address offset	Address A18-A0	Data (Hex)		Description
(P)h	35h	50h	"P"	Query ASCII string - extended table
(P+1)h	36h	52h	"R"	
(P+2)h	37h	49h	"Y"	
(P+3)h	38h	31h		Major version number
(P+4)h	39h	31h		Minor version number
(P+5)h	3Ah	86h		Optional feature: (1=yes, 0=no) bit0, Chip Erase supported (0=no) bit1, Suspend Erase supported (1=yes) bit2, Suspend Program supported (1=yes) bit3, Lock/Unlock supported (1=yes) bit4, Queue Erase supported (0=no) bit 31-5 reserved for future use
(P+6)h	3Bh	01h		Optional features: synchronous read supported
(P+7)h	3Ch	00h		
(P+8)h	3Dh	00h		
(P+9)h	3Eh	01h		Function allowed after suspend: Program allowed after Erase Suspend (1=yes) Bit 7-1 reserved for future use
(P+A)h	3Fh	Reserved		

Appendix B Flowcharts

Figure 22. Program flowchart and pseudocode



1. If an error is found, the status register must be cleared before further program/erase operations.

Figure 23. Program suspend & resume flowchart and pseudocode

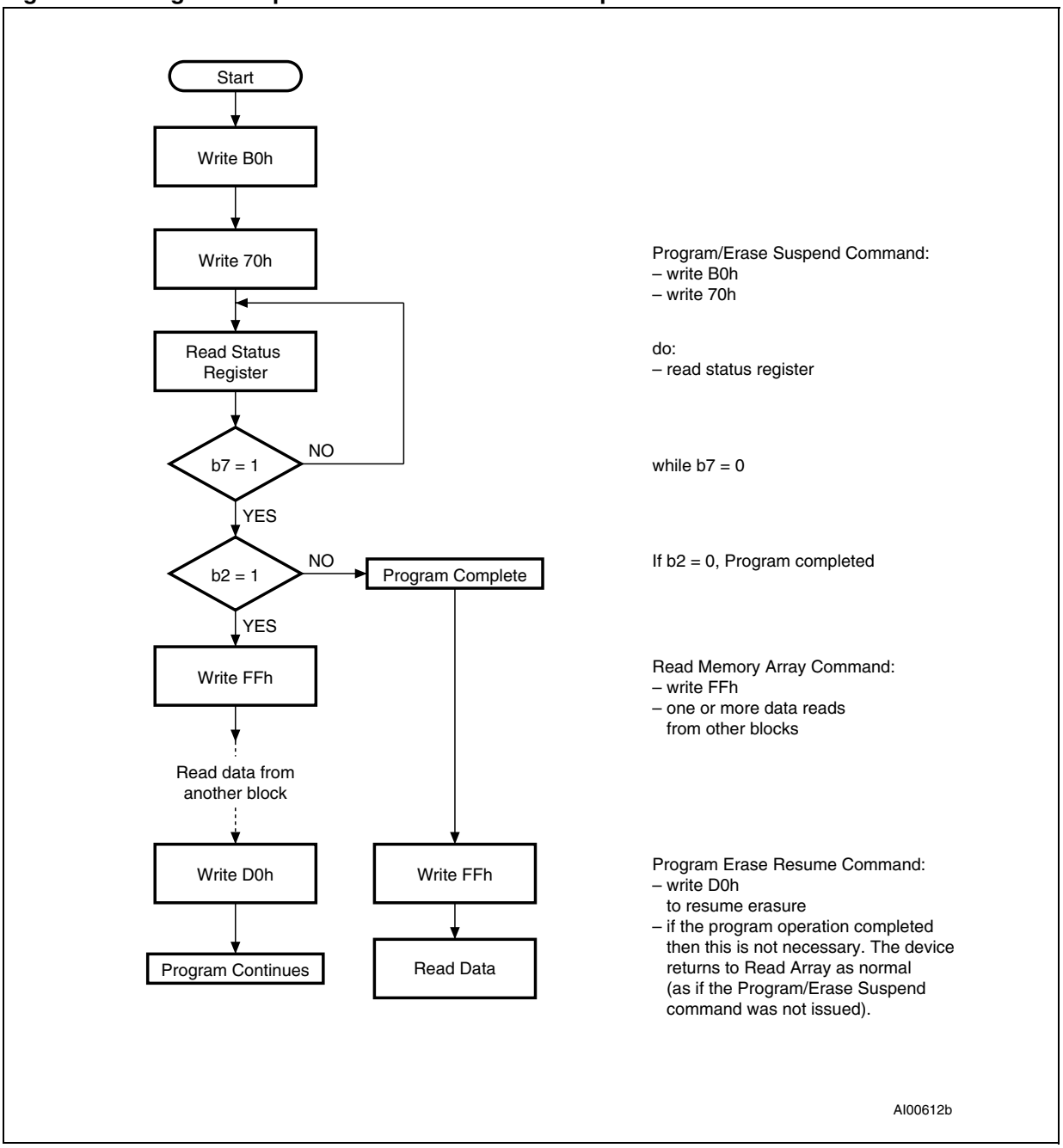
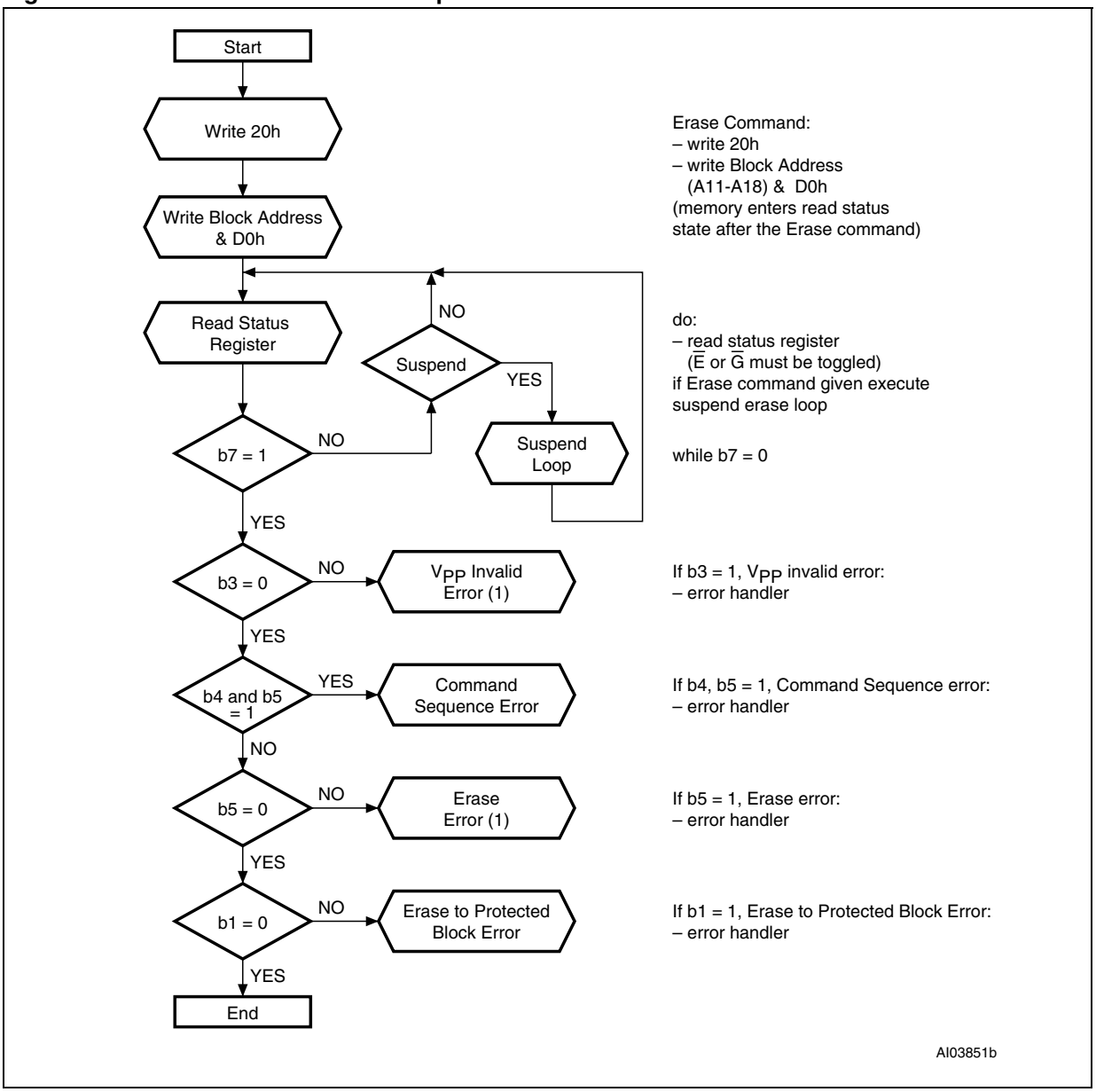
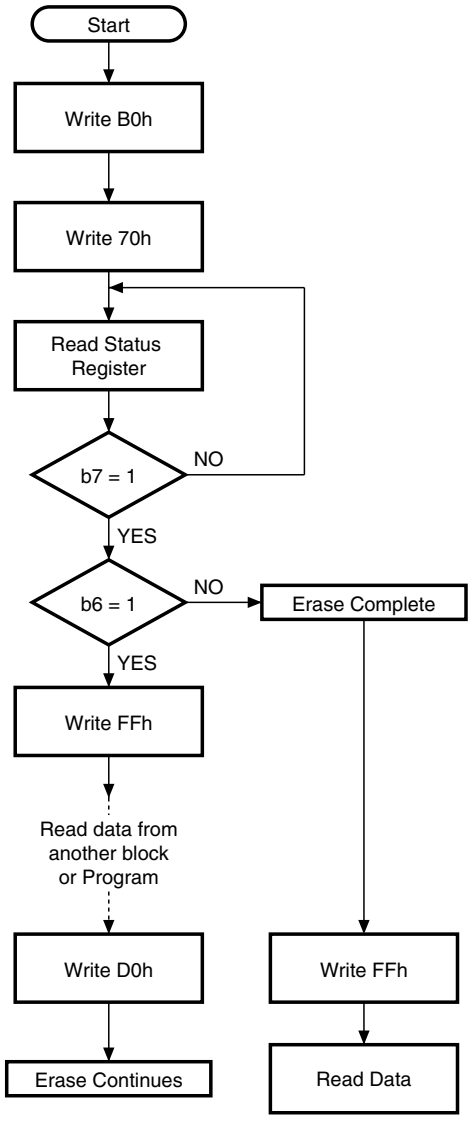


Figure 24. Block erase flowchart and pseudocode



1. If an error is found, the status register must be cleared before further program/erase operations.

Figure 25. Erase suspend & resume flowchart and pseudocode



Program/Erase Suspend Command:
– write B0h
– write 70h

do:
– read status register

while b7 = 0

If b6 = 0, Erase completed

Read Memory Array command:
– write FFh
– one or more data reads from other blocks

Program/Erase Resume command:
– write D0h to resume the Erase operation
– if the Erase operation completed then this is not necessary. The device returns to Read mode as normal (as if the Program/Erase suspend was not issued).

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Figure 26. Power-up sequence followed by synchronous burst read

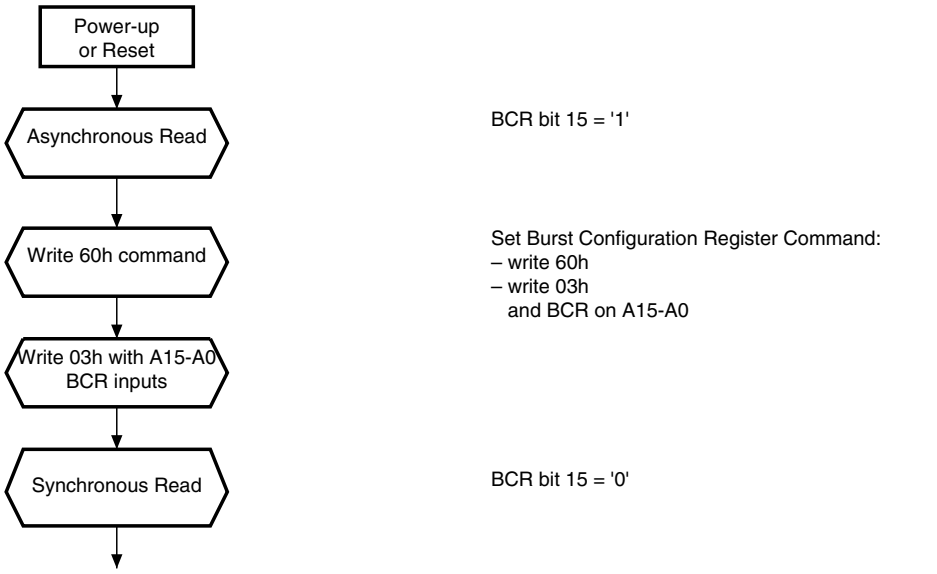


Figure 27. Command interface and program/erase controller flowchart (a)

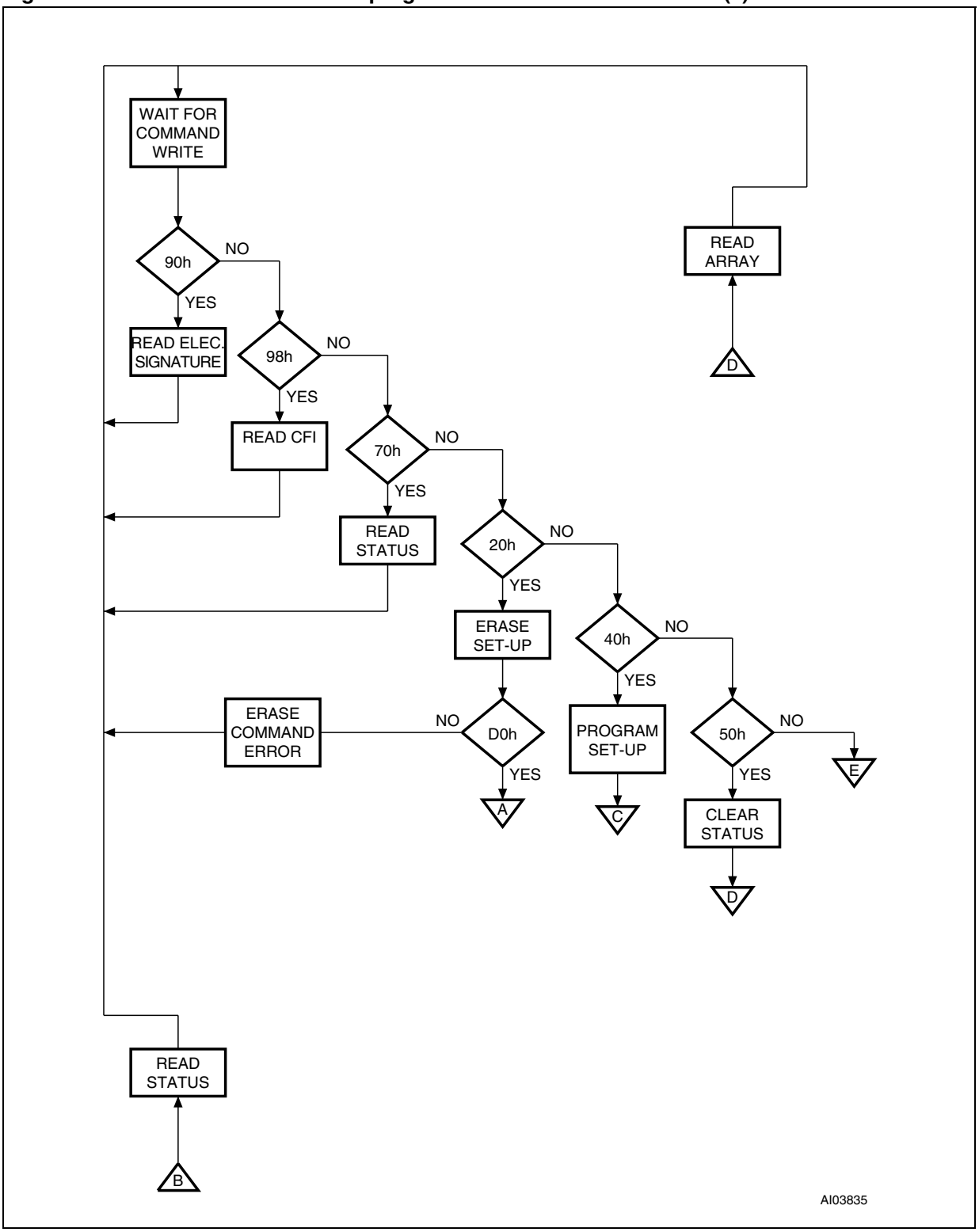


Figure 28. Command interface and program/erase controller flowchart (b)

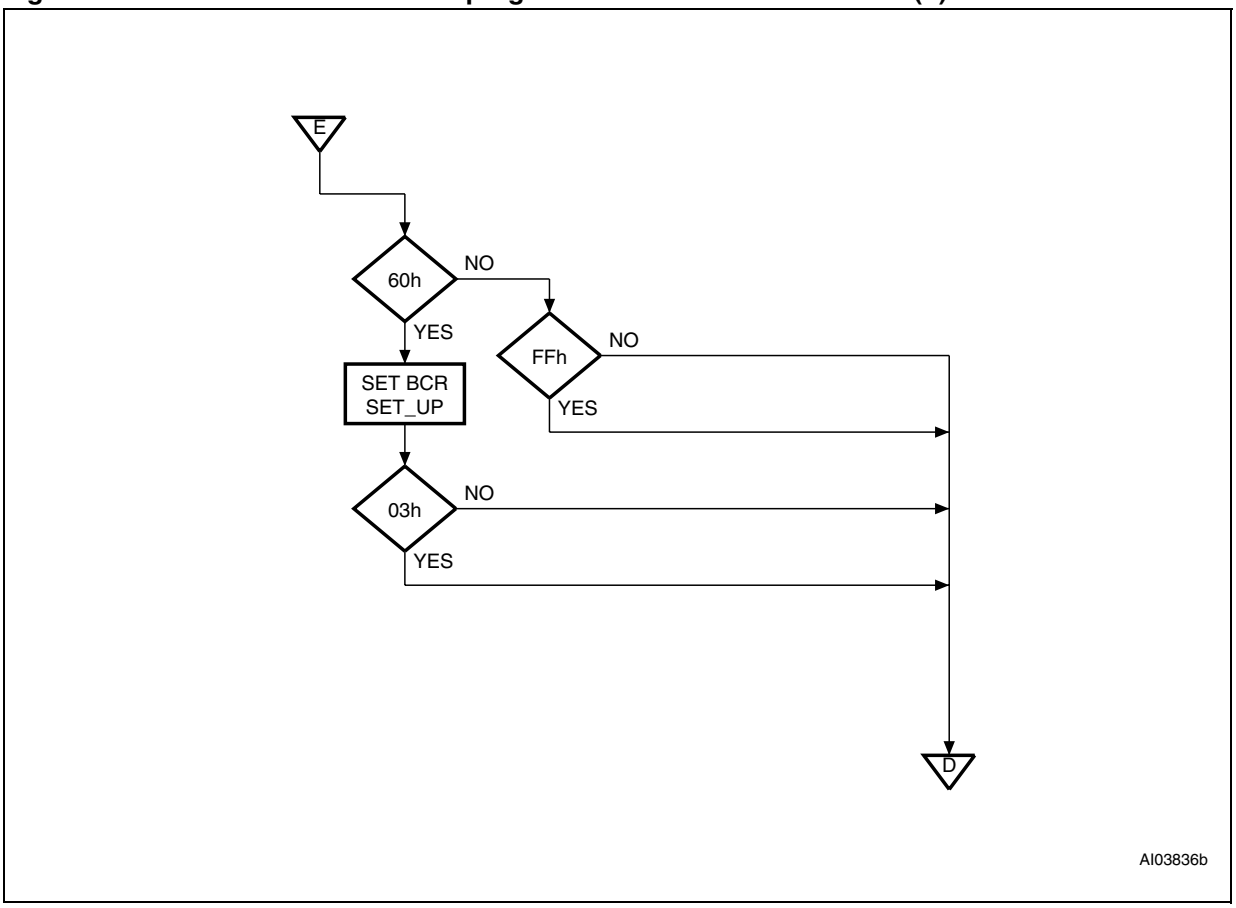


Figure 29. Command interface and program/erase controller flowchart (c)

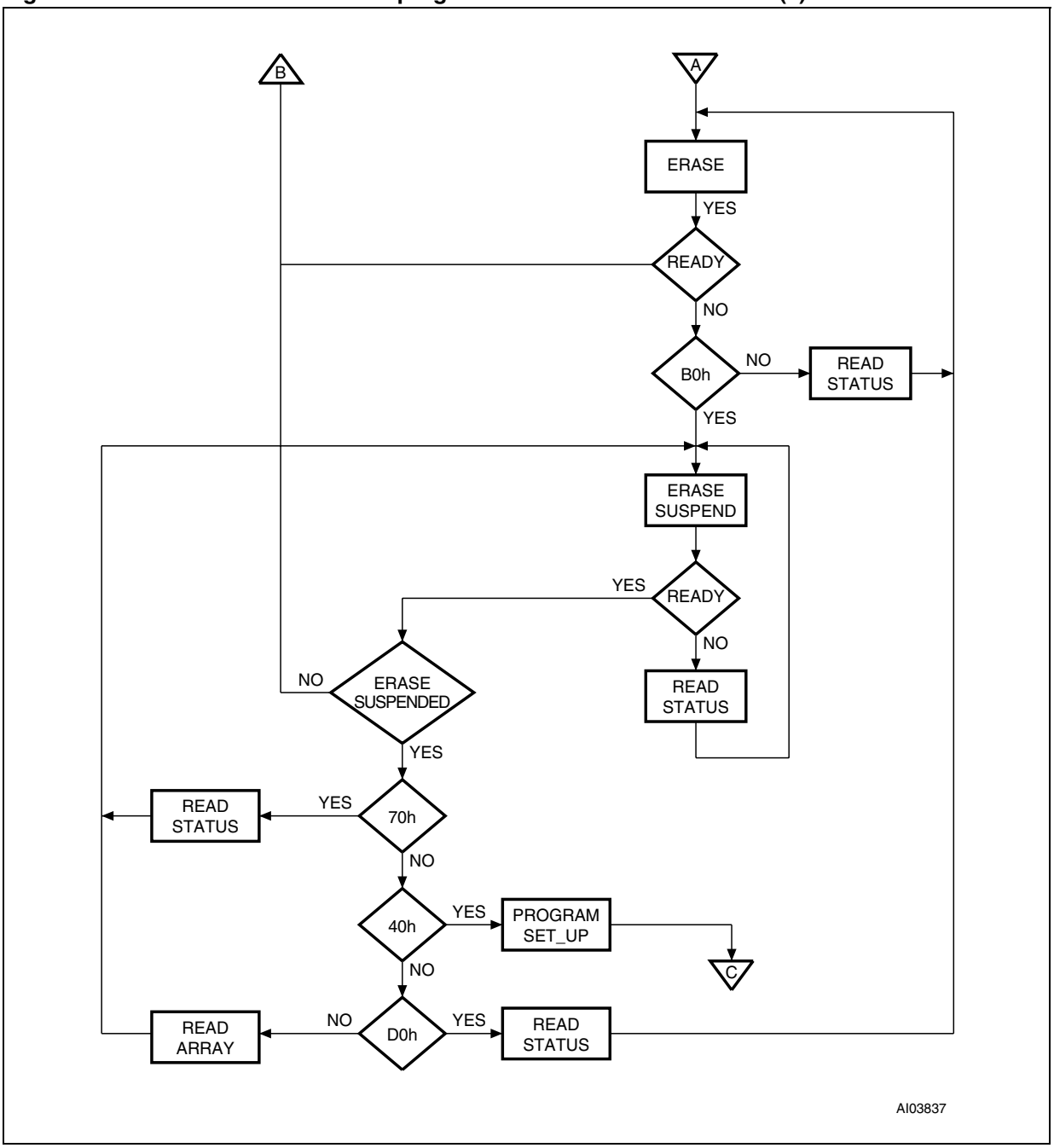
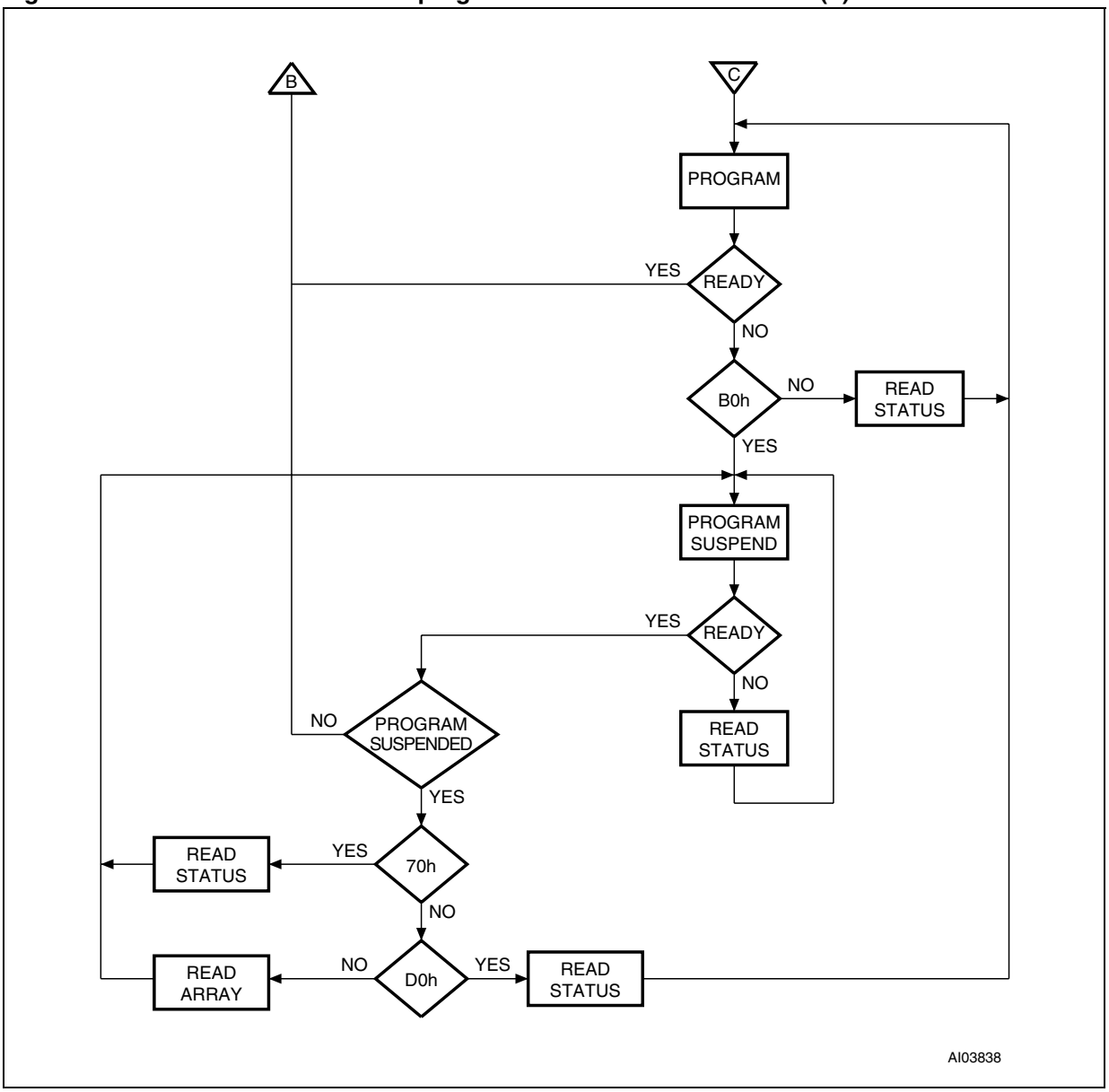


Figure 30. Command interface and program/erase controller flowchart (d)



10 Revision history

Table 31. Document revision history

Date	Version	Changes
January-2001	01	First Issue.
05-Jun-2001	02	Major rewrite and restructure.
15-Jun-2001	03	Nd and Ne values changed in PQFP80 package mechanical table.
17-Jul-2001	04	PQFP80 package outline drawing and mechanical data table updated.
17-Dec-2001	05	t_{LEAD} removed from absolute maximum ratings (*Table 12*). 80, 90 and 100 ns speed classes defined (*Table 16*, *Table 17*, *Table 18*, *Table 19* and *Table 20* clarified accordingly). *Figure 13*, *Figure 14*, *Figure 15* and *Figure 16* clarified. Temperature range 3 and 6 added. *Table 13*, *Table 14*, *Table 15*, *Table 22* and CFI *Table 27*, *Table 28*, *Table 29*, *Table 30* clarified. Document status changed from Product Preview to Preliminary Data.
17-Jan-2002	06	DC characteristics I_{PP}, I_{PP1} and I_{DD1} clarified. AC Bus Read characteristics timing t_{GHQZ} clarified.
30-Aug-2002	6.1	Revision numbering modified: a minor revision will be indicated by incrementing the tenths digit, and a major revision, by incrementing the units digit of the previous version (e.g. revision version 06 becomes 6.0). References of V_{PP} pin used for block protection purposes removed. *Figure 8* modified.
4-Sep-2002	7.0	Datasheet status changed from Preliminary Data to full Datasheet. t_{WLWH} parameter modified in *Table 19: Asynchronous write and latch controlled write AC characteristics*.
13-May-2003	7.1	Revision history moved to end of document. V_{PP} clarified in Program and Block Erase commands and Status Register, V_{PP} Status bit. V_{PPLK} added to DC characteristics table. Timing t_{KHQV} modified.
16-Oct-2003	7.2	Silicon Version added to Ordering Information Scheme.
03-Mar-2005	8	Tuning block protection feature removed from the whole document and root part numbers M58BW016BT/B have been removed. *Figure 22*, *Figure 23*, *Figure 24*, *Figure 25*, *Figure 26* and *Figure 28* updated. LBGA80 package (ZA) removed. Lead-free option added. 90 and 100 ns access times removed and 70 ns added. Temperature rage 6 removed from *Table 25: Ordering information scheme*.
06-Sep-2005	9	Load capacitance updated in *Table 13: Operating and AC measurement conditions*.
3-Mar-2006	10	Updated *Table 25: Ordering information scheme on page 55* and Disclaimer information. Converted document to new template.
16-Jun-2006	11	M58BW016FT and M58BW016FB part numbers added. Small text changes.

Table 31. Document revision history (continued)

Date	Version	Changes
09-Nov-2006	12	LBGA80 package added (see *Figure 21* and *Table 24*). M58BW016FT and M58BW016FB behavior in Burst mode specified under *Section 3.2.1: Synchronous burst read*. I_{DDB}, I_{DD1} and I_{DD4} current values specified for M58BW016FT and M58BW016FB in *Table 15: DC characteristics*, I_{DD5} added. t_{VDHPH} specified for M58BW016FT and M58BW016FB in *Table 22: Reset, power-down and power-up AC characteristics*. t_{KHQX} specified for M58BW016FT and M58BW016FB in *Table 20: Synchronous burst read AC characteristics*. 23h-24h reserved in *Table 28: CFI - device voltage and timing specification*. 3Fh reserved in *Table 30: Extended query information*.
24-Nov-2006	13	I_{DD} current specified for M58BW016DT/B and M58BW016FT/B in *Table 15: DC characteristics*.
05-Oct-2007	14	*Table 7: Burst configuration register* and *Table 22: Reset, power-down and power-up AC characteristics* updated. Modified values for t_{LLKH} in *Table 20: Synchronous burst read AC characteristics*. *Figure 17: Reset, power-down and power-up AC waveforms - control pins low* updated and *Figure 18: Reset, power-down and power-up AC waveforms - control pins toggling* added. Small text changes.
16-Jan-2008	15	Added: *Figure 19: Power supply slope specification* and *Table 21: Power supply AC and DC characteristics*. Changed mechanical data of the LBGA package and the description for the 010 value of M13 M11 bits in *Table 7: Burst configuration register*. Minor text changes.
12-Mar-2008	16	Added: information on data retention and reliability level *on page 1*, note 3 below *Table 7: Burst configuration register*, and note 1, 2, 3 below *Figure 13: Synchronous burst read (data valid from 'n' clock rising edge)*. Modified: note 2 below *Table 7: Burst configuration register* and *Table 25: Ordering information scheme*. Minor text changes.
26-Mar-2008	17	Applied Numonyx branding.

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