

Specification for BT 96040AV-FSTF-12-I2C-COG

Version March 2004

VL-FS-COG-BT96040-03 REV. A
(BT 96040AV-FSTF-12-I2C-COG)

MAR/2004

PAGE 2 OF 10

DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2004.03.23	First Release. Based on a.) Test Specification: VL-TS-COG-BT96040-03 REV. A, 2003-10-31. b.) VL-QUA-012A-S, REV. P, APR/2003 (English version). According to VL-QUA-012A-S, LCD size is small because Unit Per Laminate=35 which is more than 6pcs/Laminate.	CHEN HUI JUAN	SUNNY LEE

CONTENTS

	<u>Page No.</u>
1. GENERAL DESCRIPTION	4
2. MECHANICAL SPECIFICATIONS	4
3. INTERFACE SIGNALS	6
4. ABSOLUTE MAXIMUM RATINGS	7
4.1 ELECTRICAL MAXIMUM RATINGS (Ta=25°C)	7
4.2 ENVIRONMENTAL CONDITION	7
5. ELECTRICAL SPECIFICATIONS	8
5.1 TYPICAL ELECTRICAL CHARACTERISTICS	8
5.2 TIMING SPECIFICATIONS	9
6. LCD COSMETIC CONDITIONS	10

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MAR/2004

PAGE 4 OF 10

**Specification
of
LCD Module Type
Item No.: COG-BT96040-03**

1. General Description

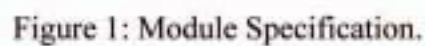
- Ë 96 x 40 dots FSTN Black & White Positive Transflective Dot Matrix LCD module.
- Ë Viewing Angle: 12 O'clock direction.
- Ë Driving duty: 1/40 Duty, 1/7.3 bias.
- Ë Driving IC: 'PHILIPS' PCF 8558U/2/F2 (Gold Bump) LCD controller/driver or equivalent.
- Ë COG.
- Ë Data interface: I²C-bus.
- Ë Bonded pins.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	46.0(W) x 36.2(H) x 1.845(D) (Excluded pins)	mm
Viewing area	40.0(W)x 23.0(H)	mm
Active area	35.2(W)x 18.2(H)	mm
Display format	96 x 40	dots
Weight:	TBD	grams



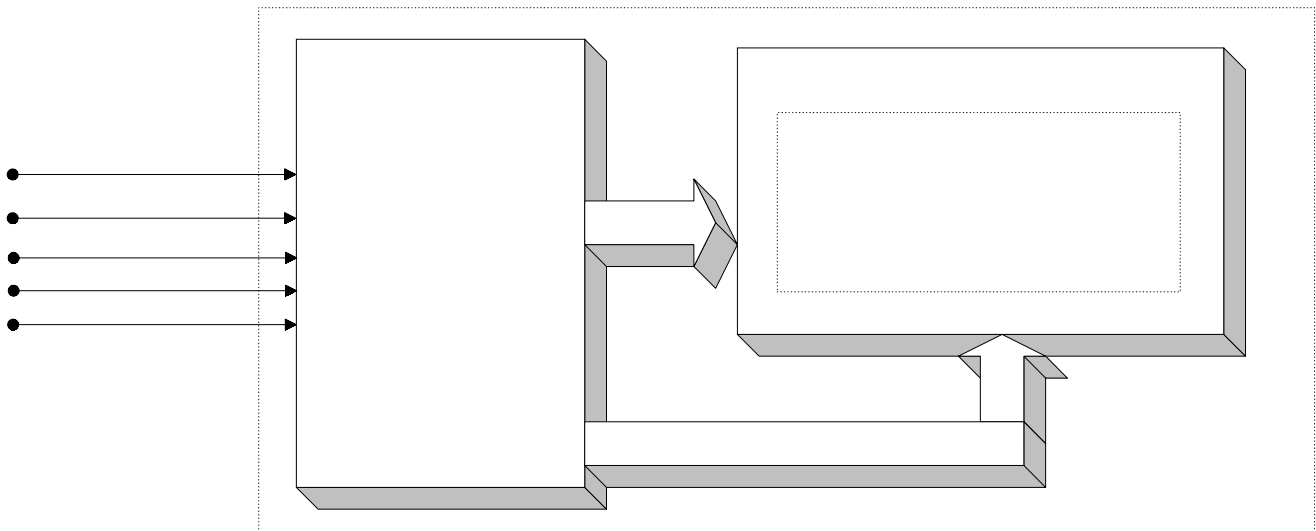


Figure 2: Block Diagram

3. Interface signals

Table 2

Pin No.	Symbol	Description
1	SDA	I ² C-bus serial data input/output
2	VSS	Ground (0V).
3	VLCD	Power supply for LCD driver.
4	VDD	Power supply for logic (+5V).
5	SCL	I ² C-bus serial clock input

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings(Ta = 25 °C)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.5	+8.0	V
Input voltage range (SDA,SCL)	Vin	VSS-0.5	+8.0	V
Supply voltage (LCD)	Vop=VDD-VLCD	0	+11.0	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0℃	+50℃	-10℃	+60℃	Dry
Humidity	95% max. RH for Ta ≤ 40℃ < 95% RH for Ta > 40℃				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s ² = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At $T_a = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	$V_{DD}-V_{SS}$		4.95	5.0	5.05	V
Operating voltage for LCD	$V_{op} = V_{DD} - V_{LCD}$	$T_a = 0\text{ }^{\circ}\text{C}$, $V_{DD} = +5\text{V}$, Character mode, Note 1	-	7.3	-	V
		$T_a = +25\text{ }^{\circ}\text{C}$, $V_{DD} = +5\text{V}$, Character mode, Note 1	6.9	7.1	7.3	V
		$T_a = +50\text{ }^{\circ}\text{C}$, $V_{DD} = +5\text{V}$, Character mode, Note 1	-	6.9	-	V
Operating supply current (Logic&LCD)	I_{DD}	Character mode, $V_{DD} = 5.0\text{V}$	-	100	150	μA
		Checker board, $V_{DD} = 5.0\text{V}$	-	110	160	μA
Input signal voltage low (SDA, SCL)	V_{il}		V_{SS}	-	0.3 V_{DD}	V
Input signal voltage high (SDA, SCL)	V_{ih}		0.7 V_{DD}	-	V_{DD}	V

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

$T_a = 0\text{ }^{\circ}\text{C}$ to $+50\text{ }^{\circ}\text{C}$, $V_{DD} = +5.0\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$; $V_{LCD} = V_{DD} - 3.5\text{V}$ to $V_{DD} - 9\text{V}$, $V_{SS} = 0\text{V}$.

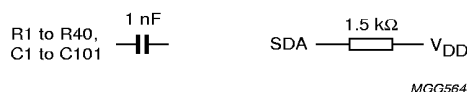
Refer to Figure 3, I²C Bus Timing Diagram of 'PHILIPS' PCF8558.

Table 6

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{FR}	LCD frame frequency (internal oscillator)		37	62.5	94	Hz
$f_{OSC(ext)}$	external clock frequency		90	150	225	kHz
t_{PLCD}	driver delays	$V_{DD} - V_{LCD} = 9\text{ V}$; with test loads	—	—	100	μs
I²C-bus (see Fig.12)						
f_{SCL}	SCL clock frequency		—	—	400	kHz
t_{CLKL}	SCL LOW time		1.3	—	—	μs
t_{CLKH}	SCL HIGH time		0.6	—	—	μs
t_{BUF}	bus free time	between successive STOP and START conditions	1.3	—	—	μs
t_r	SCL and SDA rise time	note 1	—	—	300	ns
t_f	SCL and SDA fall time	note 1	$20 + 0.1 C_b$	—	300	ns
$t_{SU;STA}$	START condition set-up time	repeated start codes only	0.6	—	—	μs
$t_{HD;STA}$	START condition hold time		0.6	—	—	μs
$t_{SU;DAT}$	data set-up time		100	—	—	ns
$t_{HD;DAT}$	data hold time		0	—	—	ns
$t_{SU;STO}$	STOP condition set-up time		0.6	—	—	μs
t_{SW}	tolerable spike width on bus	note 2	—	—	50	ns
C_b	capacitive load per bus line		—	—	400	pF

Notes

- The rise and fall times specified here refer to the driver device (i.e. not PCF8558) and are part of the general fast I²C-bus specification. However, when PCF8558 asserts an acknowledge on SDA, the fall time is given by parameter t_f . C_b = capacitive load per bus line.
- The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width $< t_{SW(max)}$.



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AC test loads.

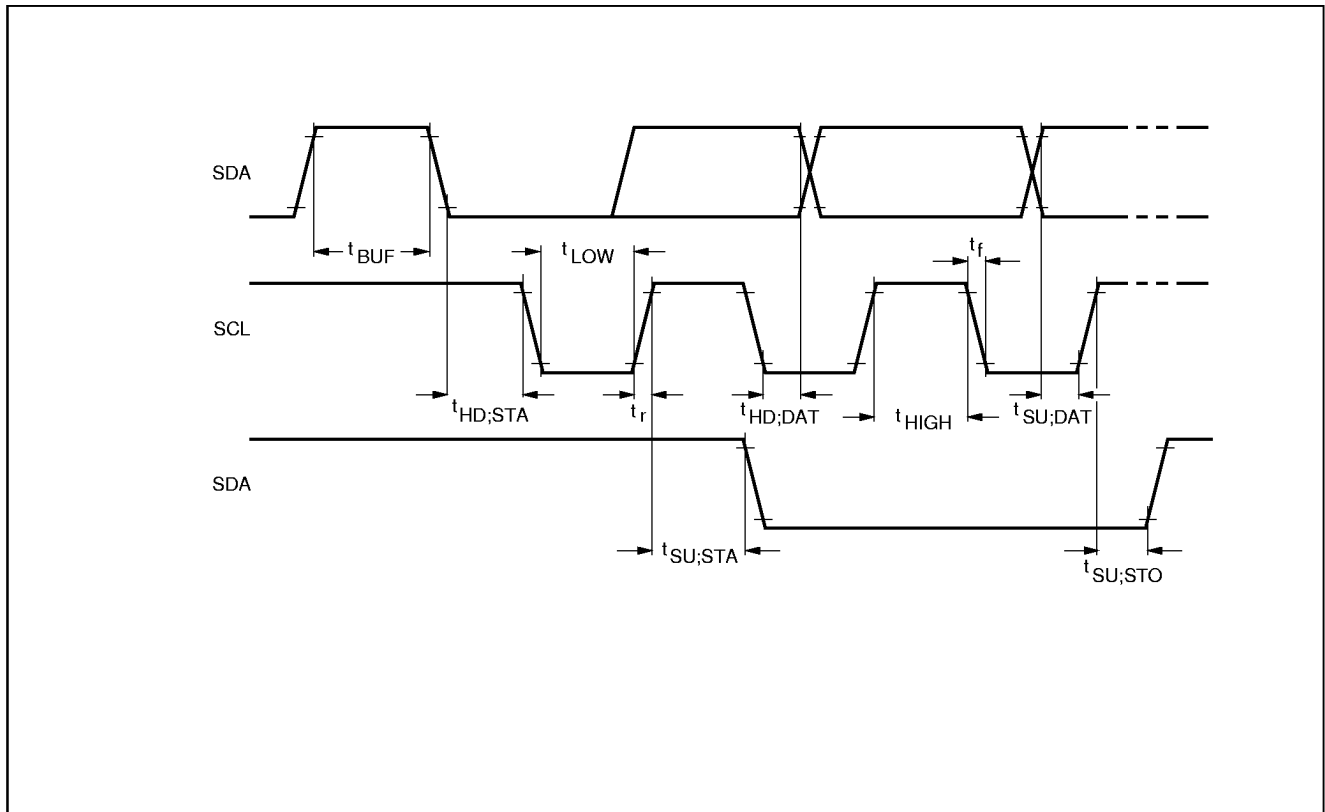


Figure 3: I²C-Bus Timing Diagram

6. LCD Cosmetic Conditions

Refer to VL-QUA-012A-S

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