

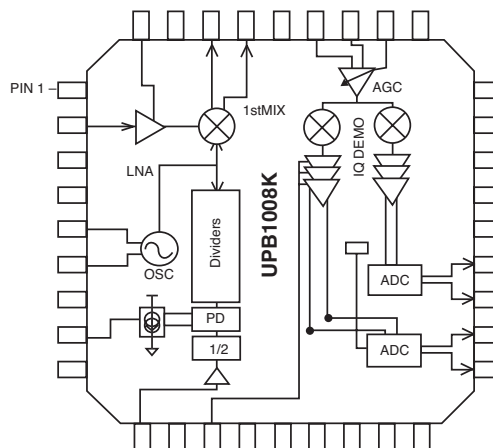
### FEATURES

- **LOW POWER CONSUMPTION:** 52 mW
- **DUAL-CONVERSION IQ DOWN CONVERTER<sup>1</sup>:**  
Reference frequency:  $REF_{in} = 27$  MHz
- **PSEUDO-BASEBAND WITH 2-BIT DIGITIZED OUTPUT**
- **ON-CHIP LNA, ON-CHIP FREQUENCY SYNTHESIZER,  
IF AGC AMPLIFIER:**  
with 45 dB typical range of adjustable gain
- **SMALL 36 PIN QFN PACKAGE:**  
Flat lead style for better RF performance

Note:

1. Based on eRide's proprietary GPS DSP architecture

### BLOCK DIAGRAM



### APPLICATIONS

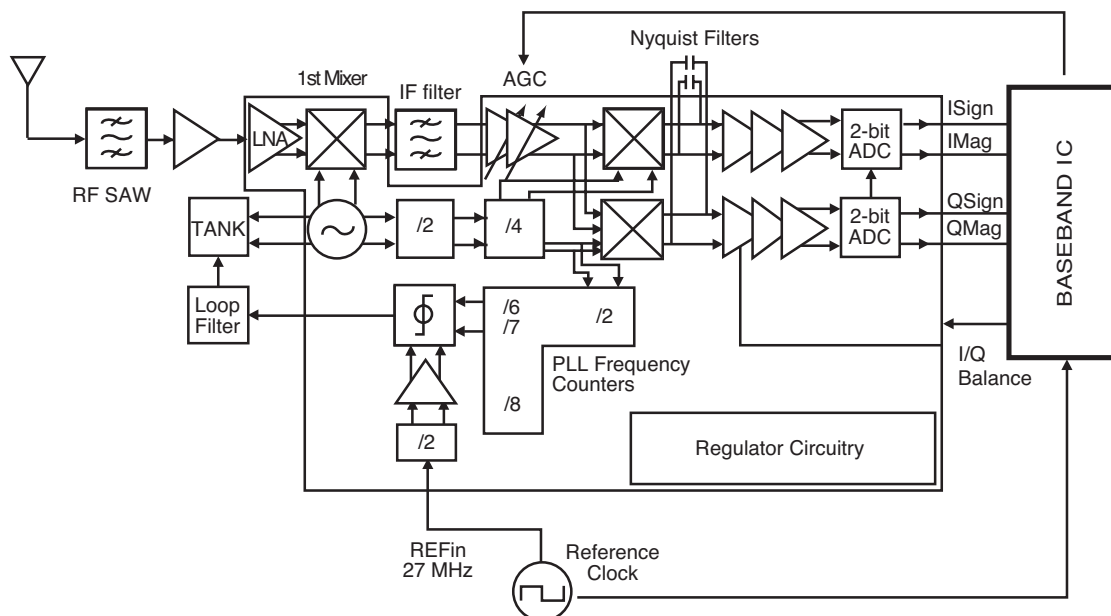
- **E911 ENABLED MOBILE PHONE**
- **IN-VEHICLE NAVIGATION SYSTEMS**
- **LOW POWER HANDHELD GPS RECEIVER**
- **PC/PDA+GPS INTEGRATION**
- **ASSET TRACKING**

### DESCRIPTION

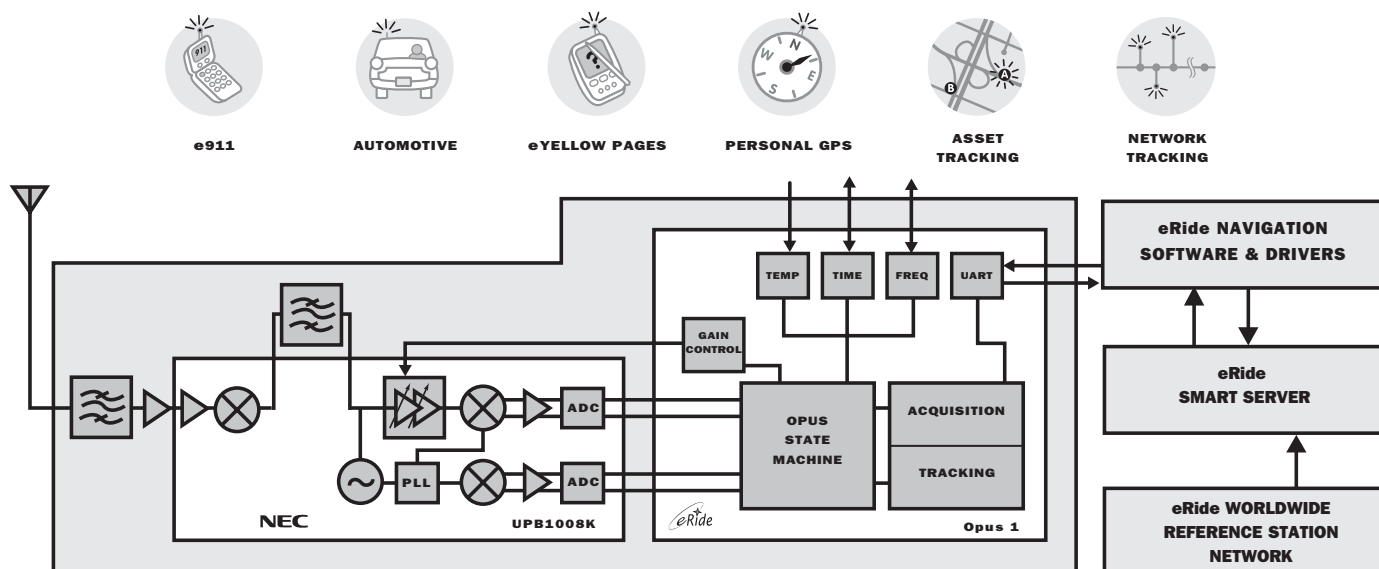
NEC's UPB1008K is a Silicon RFIC especially designed for handheld low power/low cost GPS receivers. The IC combines an LNA, followed by a double-conversion RF/IF downconverter block and a PLL frequency synthesizer on one chip. The second IF Frequency is a pseudo- baseband signal into a on-chip 2-bit A/D converters. The device can operate on a supply voltage as low as 2.7 V, and is housed in a small 36 pin QFN (Quad, Flat, No-lead) package, resulting in a very low power consumption and reduced board space.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

### RF APPLICATION DIAGRAM



## ADVANCED GPS COMPLETE SOLUTION



## ADVANCED GPS COMPLETE SOLUTION

"NEC Corporation and eRide, Inc. have teamed to provide an advanced positioning solution delivering high GPS performance, accuracy, integration and architecture flexibility. The chip set combines CEL's **UPB1008K** receiver IC with eRide's **Opus One** SOC (System-on-a-Chip) Baseband ASIC and is suitable for standard GPS products as well as Cellular Handset applications. Also provided are scalable client navigation software and drivers, plus location-aiding data from eRide's Smart Server. Together, they offer a complete hardware/infrastructure solution.

The chip set's design allows it to operate independently of wireless interface standards - and independently of the host product's CPU and Operating System. This unique approach to system integration makes it easy to deploy the chip set into an wireless application, in any wireless network. A "Universal Hardware" solution, the design promises lower manufacturing costs and, ultimately lower cost to the consumer.

The chip set's advanced positioning architecture offers unmatched sensitivity providing fast, accurate positioning architecture offers unmatched sensitivity providing fast and accurate position fixes, even when indoors or in deep in urban canyons."

## HIGH PERFORMANCE GPS OMNI MODE

LI, C/A code receiver

| Performance                  | Indoor                    | Outdoor                         |
|------------------------------|---------------------------|---------------------------------|
| Time to First Fix w/ aiding  | 5-7sec                    | 1-3sec                          |
| Time to First Fix w/o aiding | 10-20sec                  | 3-5sec                          |
| Accuracy                     | 10-25m cep                | 2-5m cep                        |
| Sensitivity                  | -155dBm<br>in 1sec dwells | -142dBm<br>in two 10msec dwells |

Superior performance in high reflection indoor environments and in urban canyon types of outdoor environments

## POWER DISSIPATION

|           |            |
|-----------|------------|
| First Fix | 400 mW     |
| Tracking  | 200-300 mW |
| Stand By  | 30 mW      |

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.0\text{ V}$ , unless otherwise specified)

| SYMBOLS             | PARAMETERS AND CONDITIONS                                     | UNITS | MIN | TYP | MAX  |
|---------------------|---------------------------------------------------------------|-------|-----|-----|------|
| I <sub>CC</sub>     | Total Circuit Current, No Signals                             | mA    | 14  | 18  | 23.5 |
| V <sub>CC</sub>     | Supply Voltage                                                | V     | 2.7 | 3.0 | 3.3  |
| I <sub>CC_PD</sub>  | Power down current, PIN 13 = V <sub>IL</sub>                  | μA    | –   | 1   | 10   |
| I <sub>CC rf</sub>  | RF Block Circuit Current (pin 3), No signal                   | μA    | 0.4 | 0.5 | 0.7  |
| I <sub>CC lo</sub>  | VCO Block Circuit Current (pin 7), No signal                  | mA    | 4.1 | 5.6 | 7.2  |
| I <sub>CC pll</sub> | PLL Block Circuit Current (pin 9), No signal                  | mA    | 2.7 | 3.6 | 4.7  |
| I <sub>CC bb</sub>  | Baseband Block Circuit Current (pin 23), No signal, open load | mA    | 2.5 | 3.4 | 4.3  |
| I <sub>CC if</sub>  | IF Block Circuit Current (pin 28) , No signal                 | mA    | 2.7 | 3.7 | 4.7  |
| I <sub>CC ina</sub> | Pre-Amplifier Open Connector Current (pin 36), No signal      | mA    | 1.0 | 1.4 | 1.8  |

**LNA/RF DOWNCONVERTER**(f<sub>RFIn</sub> = 1575.42 MHz, f<sub>1stLOin</sub> = 1400 MHz, P<sub>LO</sub> = -10 dBm, f<sub>1stIF</sub> = 175 MHz, Pin 13: V<sub>IL</sub> = 3 V, Z<sub>L</sub> differential = 32Ω & Z<sub>s</sub> = Γ<sub>opt</sub>)

| SYMBOLS                  | PARAMETERS AND CONDITIONS                                                        | UNITS | MIN | TYP | MAX |
|--------------------------|----------------------------------------------------------------------------------|-------|-----|-----|-----|
| CGLNA_MIX                | Power conversion gain from 2nd LNA/mixer to 1st IF, P <sub>RFIn</sub> = -50 dBm  | dB    | 18  | 23  | 28  |
| NFLNA_MIX                | Noise Figure of 2nd LNA/mixer(SSB), Input matched                                | dB    | –   | 5   | –   |
| P <sub>1dB</sub> LNA_MIX | 1 dB Compression refer to source, Input matched                                  | dBm   | –   | -38 | –   |
| Z <sub>LNAin</sub>       | RF Input Impedance of LNA                                                        | Ohm   | –   | 31  | –   |
| Z <sub>MIXout</sub>      | IF Output Impedance of Mixer                                                     | Ohm   | –   | 32  | –   |
| ALO-IF                   | Local Signal Leak to IF, f <sub>1stLOin</sub> =1400 MHz, P <sub>LO</sub> = 0 dBm | dBm   | –   | -35 | –   |
| ALO-RF                   | Local Signal Leak to RF, f <sub>1stLOin</sub> =1400 MHz, P <sub>LO</sub> = 0 dBm | dBm   | –   | -50 | –   |

**PLL**

| SYMBOLS           | PARAMETERS AND CONDITIONS                                                   | UNITS | MIN | TYP  | MAX |
|-------------------|-----------------------------------------------------------------------------|-------|-----|------|-----|
| I <sub>CPH</sub>  | PLL Charge Pump High Side Current @ V <sub>CPout</sub> = V <sub>CC</sub> /2 | μA    | –   | 200  | –   |
| I <sub>CPOL</sub> | PLL Charge Pump Low Side Current @ V <sub>CPout</sub> = V <sub>CC</sub> /2  | μA    | –   | -200 | –   |
| f <sub>PD</sub>   | Phase Comparison Frequency                                                  | MHz   | –   | 13.5 | –   |

**CRYSTAL OSCILLATOR/REFERENCE AMPLIFIER BLOCK**

| SYMBOLS            | PARAMETERS AND CONDITIONS               | UNITS  | MIN | TYP | MAX |
|--------------------|-----------------------------------------|--------|-----|-----|-----|
| V <sub>REFin</sub> | Reference input minimum level           | mVpp   | 50  | 200 | –   |
| f <sub>REF</sub>   | Input Frequency of Reference Input      | MHz    | –   | 27  | –   |
| VT                 | VCO Control Voltage, PLL Locked         | V      | 0.8 | 1.5 | 2.2 |
| C/N                | VCO C/N, Δ1kHz, Loop band width = 5 kHz | dBc/Hz | 57  | 62  | –   |

**AGC AMPLIFIER, I-Q DEMODULATOR, and ADC BLOCK**(f<sub>1stFin</sub> = 175 MHz, Z<sub>in</sub> = 600Ω)

| SYMBOLS              | PARAMETERS AND CONDITIONS                                                                                                   | UNITS | MIN | TYP | MAX |
|----------------------|-----------------------------------------------------------------------------------------------------------------------------|-------|-----|-----|-----|
| CGAGC/MIX            | Maximum voltage conversion gain of AGC amplifier/ I-Q mixer, P <sub>in</sub> = -60 dBm, V <sub>AGC</sub> = 0.5 V, Unmatched | dB    | –   | 30  | –   |
|                      | Minimum voltage conversion gain of AGC amplifier/ I-Q mixer, P <sub>in</sub> = -60 dBm, V <sub>AGC</sub> = 2.0 V, Unmatched | dB    | –   | -15 | –   |
| AAGC/MIX             | AGC control range, V <sub>AGC</sub> = 0.5 V to 2 V                                                                          | dB    | 25  | 45  | –   |
| P <sub>1dB</sub> AGC | 1 dB compression input to AGC amplifier, set voltage gain = 30 dB                                                           | dBm   | –   | -45 | –   |
| V <sub>AGC</sub>     | AGC control voltage                                                                                                         | V     | 0.5 | –   | 2.0 |
| BW                   | 3dB Mixer Bandwidth                                                                                                         | MHz   | –   | 10  | –   |
| V <sub>IQ-C</sub>    | IQ BalanceControl Voltage, Gain(Ich) = Gain (Qch)                                                                           | V     | –   | 2.1 | 2.8 |
| A <sub>IQ-C</sub>    | IQ Balance Control Gain Range, V <sub>IQ-C</sub> = 0 to 3 V                                                                 | dB    | 4.0 | 6.5 | –   |
| Duty Ich             | Ich Mag Bit Output Pulse Duty, P <sub>1stFin</sub> = -84 dBm V <sub>AGC</sub> = 0.5 V, V <sub>IQ-C</sub> = 0 V              | %     | 50  | –   | –   |
| Duty Qch             | Qch Mag Bit Output Pulse Duty, P <sub>IF2in</sub> = -88 dBm V <sub>AGC</sub> = 0.5 V, V <sub>IQ-C</sub> = 0 V               | %     | 50  | –   | –   |

**BASEBAND AMPLIFIER BLOCK** (Z<sub>s</sub> = 2kΩ & Z<sub>L</sub> = 2 kΩ)

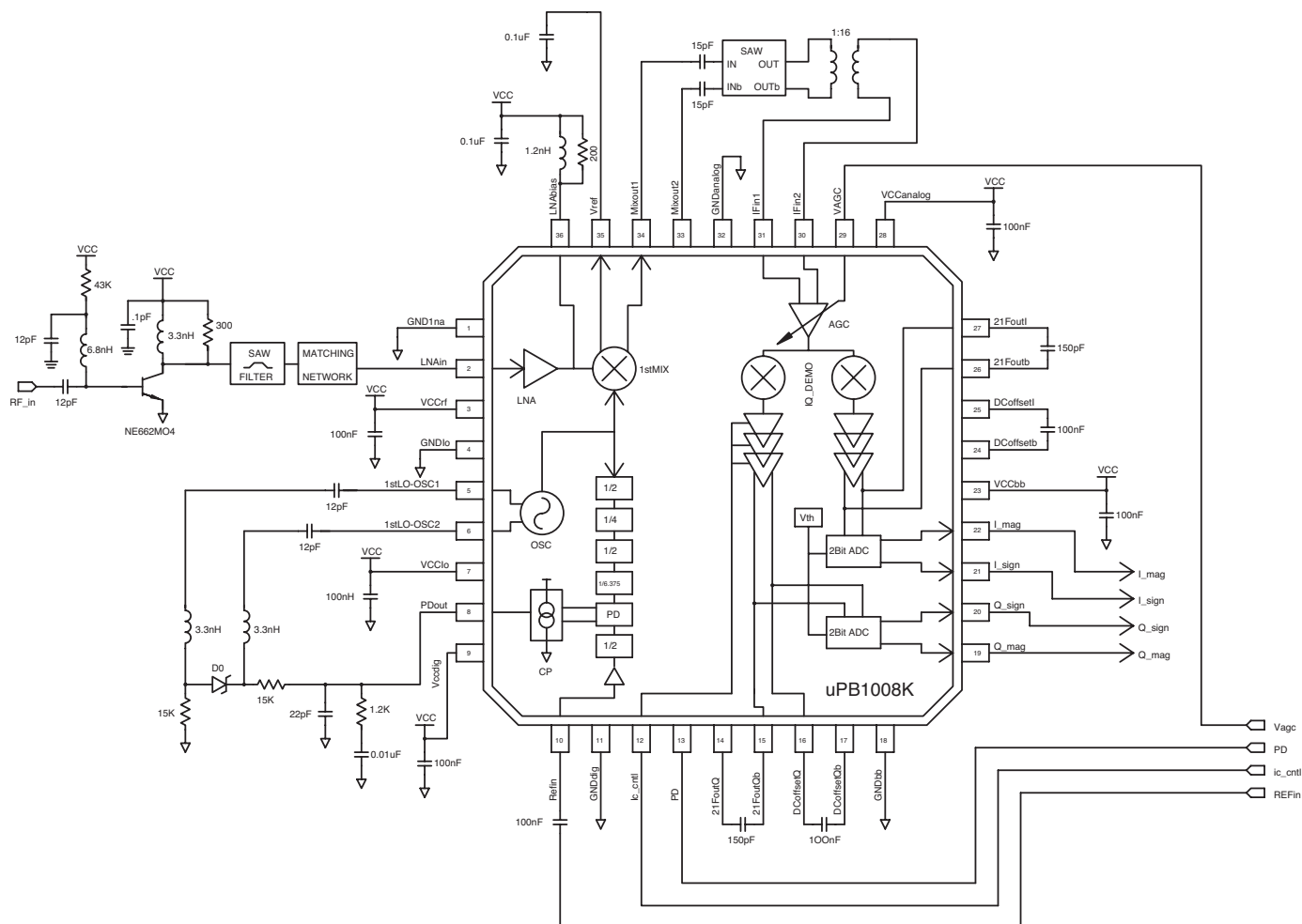
| SYMBOLS            | PARAMETERS AND CONDITIONS                          | UNITS | MIN | TYP | MAX |
|--------------------|----------------------------------------------------|-------|-----|-----|-----|
| V <sub>BBOH</sub>  | Baseband output logic high, C <sub>L</sub> = 10 pF | V     | 2.0 | –   | –   |
| V <sub>B BOL</sub> | Baseband output logic low, C <sub>L</sub> = 10 pF  | V     | 0   | –   | 0.5 |

| SYMBOLS               | PARAMETERS                           | UNITS           | RATINGS     |
|-----------------------|--------------------------------------|-----------------|-------------|
| V <sub>CC</sub>       | Supply Voltage <sup>4</sup>          | V <sub>CC</sub> | 3.6         |
| P <sub>D</sub>        | Total Power Dissipation <sup>3</sup> | mW              | 361         |
| T <sub>OP</sub>       | Operating Temperature                | °C              | -40 to +85  |
| T <sub>STG</sub>      | Storage Temperature                  | °C              | -55 to +150 |
| I <sub>CC_total</sub> | Total Circuit Current <sup>4</sup>   |                 |             |

1. Operation in excess of any one of these parameters may result in permanent damage.
2. More than two items must not be reached simultaneously.
3.  $T_A = +85^{\circ}\text{C}$ , mounted on a 50 x 50 x 1.6 mm double-sided copper clad epoxy glass PWB.
4.  $T_A = 25^{\circ}\text{C}$

| SYMBOLS              | PARAMETERS                        | UNITS | MIN | TYP  | MAX             |
|----------------------|-----------------------------------|-------|-----|------|-----------------|
| V <sub>CC</sub>      | Supply Voltage                    | V     | 2.7 | 3.0  | 3.3             |
| T <sub>OP</sub>      | Operating Temperature             | °C    | -40 | +25  | +85             |
| f <sub>RFIn</sub>    | RF Input Frequency                | MHz   |     | 1575 |                 |
| f <sub>REFIn</sub>   | Reference Frequency               | MHz   |     | 27   |                 |
| f <sub>1stLo</sub>   | 1st LO Oscillating Frequency      | MHz   |     | 1400 |                 |
| f <sub>1stIFIn</sub> | 1st IF Input Frequency            | MHz   |     | 175  |                 |
| f <sub>2ndLOIn</sub> | 2nd LO Input Frequency            | MHz   |     | 175  |                 |
| V <sub>IH</sub>      | Power Down Control Voltage "High" | V     | 2   |      | V <sub>CC</sub> |
| V <sub>IL</sub>      | Power Down Control Voltage "Low"  | V     | 0   |      | 0.5             |

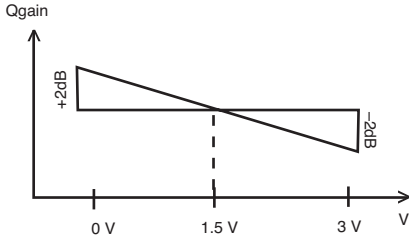
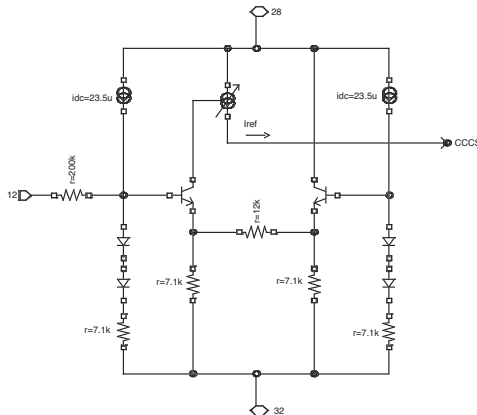
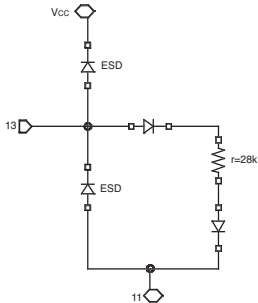
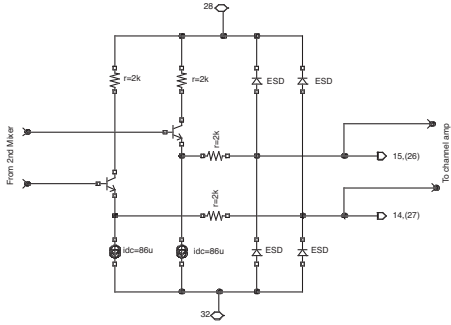
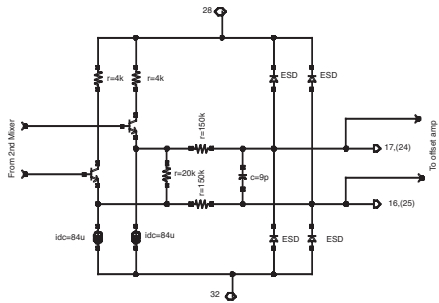
## APPLICATION CIRCUIT

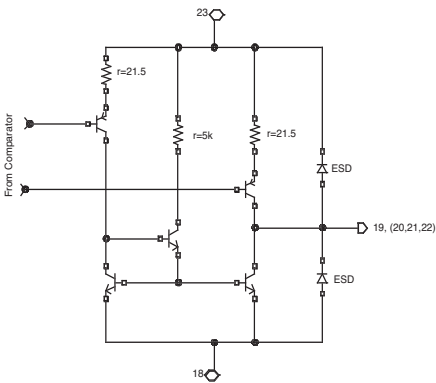
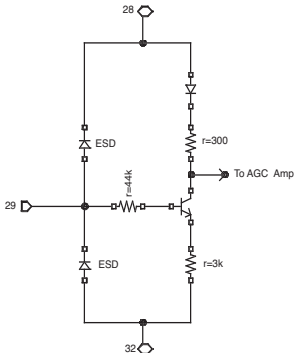
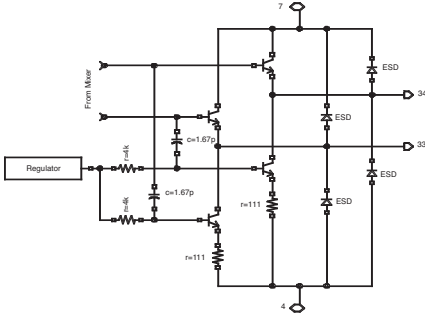


# PIN FUNCTIONS

| Pin No. | Symbol     | Function and Application                                                                                                                                       | Internal Equivalent Circuit |
|---------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|
| 1       | GNDIna     | Ground pin of LNA                                                                                                                                              |                             |
| 2       | LNAin      | Input pin of low noise amplifier. It is a single-ended open collector design. Capacitive coupling is required; external matching will improve gain or NF.      |                             |
| 3       | VCCrf      | Supply voltage pin of LNA, RF mixer and VCO voltage regulator.                                                                                                 |                             |
| 4       | GNDlo      | Ground pin of 1st LO Oscillator circuit and RF Mixer.                                                                                                          |                             |
| 5       | 1stLO-OSC1 | Pin 5 & 6 are base pins of the differential amplifier for 1st LO oscillator. These pins require an LC (varactor) tank circuit to oscillate at around 1400 MHz. |                             |
| 6       | 1stLO-OSC2 |                                                                                                                                                                |                             |
| 7       | VCClo      | Supply voltage pin of oscillator circuit for 1st LO Oscillator and RF mixer                                                                                    |                             |
| 8       | PDout      | This is a current mode charge pump output. For connection to a passive RC loop filter for driving external varactor diode of 1stLO-OSC.                        |                             |
| 9       | VCCdig     | Supply voltage pin of digital portion of the chip.                                                                                                             |                             |
| 10      | REFin      | Input pin of reference frequency buffer. This pin should be equipped with external 27 MHz oscillator (e.g. TCXO).                                              |                             |
| 11      | GNDdig     | Ground pin of digital portion of the chip.                                                                                                                     |                             |

## PIN FUNCTIONS

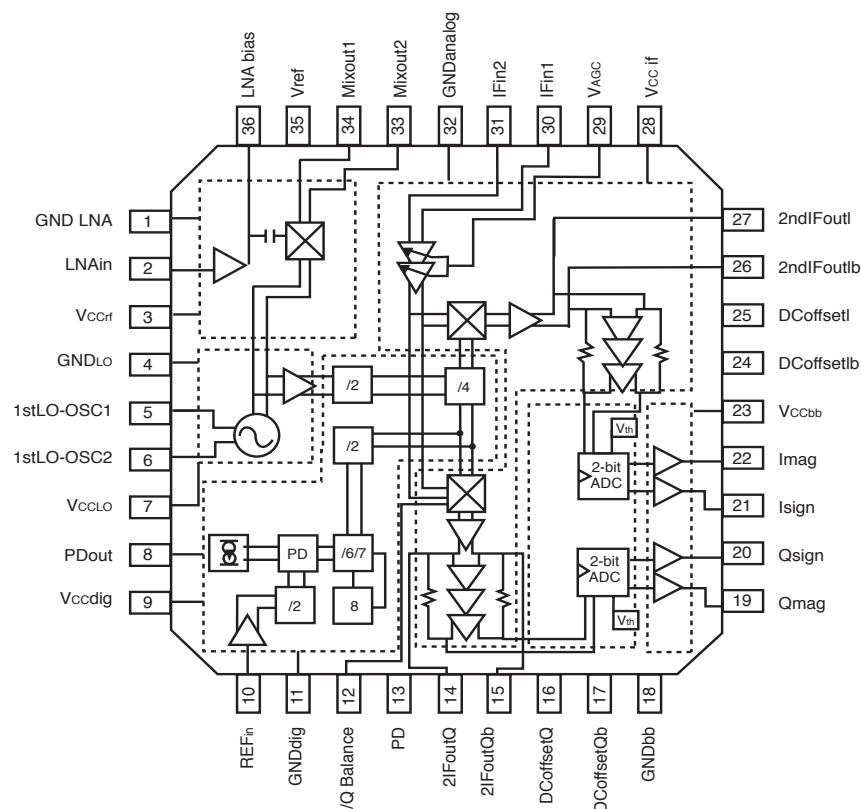
| Pin No. | Symbol              | Function and Application                                                                                                                                                                                                                                      | Internal Equivalent Circuit                                                           |
|---------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| 12      | I/Q Balance Control | <p>The voltage on this pin controls the Q channel IF Amplifier Gain. Gain control of <math>\pm 2</math> dB can be achieved for 0~3 V. Leave open-circuited if not used.</p>  |    |
| 13      | PD1                 | <p>Standby mode control. Low=whole chip OFF &amp; High=Whole chip ON.</p>                                                                                                                                                                                     |   |
| 14      | 2IFout-Q            | <p>Differential output pins of quadrature demodulator Q output. Adding a lowpass shunt capacitor between these pins will define the IF Bandwidth.</p>                                                                                                         |  |
| 15      | 2IFout-Qb           |                                                                                                                                                                                                                                                               |                                                                                       |
| 16      | DC offset Q         | <p>DC offset compensation pin for C arm. A low pass capacitor shunt to Pin 17 is required.</p>                                                                                                                                                                |  |
| 17      | DC offset Qb        | <p>DC offset compensation pin for Q-bar arm. A low pass capacitor shunt to Pin 16 is required.</p>                                                                                                                                                            |                                                                                       |

| Pin No. | Symbol     | Function and Application                                                                                                                                                   | Internal Equivalent Circuit                                                           |  |
|---------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|--|
| 18      | GNDbb      | Ground pin of CMOS output driver.                                                                                                                                          |     |  |
| 19      | Qmag       | Digitized Q signal. Magnitude bit of 2-bit ADC output.                                                                                                                     |                                                                                       |  |
| 20      | Qsign      | Digitized Q signal. Sign bit of 2-bit ADC output.                                                                                                                          |                                                                                       |  |
| 21      | Isign      | Digitized I signal. Sign bit of 2-bit ADC output.                                                                                                                          |                                                                                       |  |
| 22      | Imag       | Digitized I signal. Magnitude bit of 2-bit ADC output.                                                                                                                     |                                                                                       |  |
| 23      | VCCbb      | Supply voltage pin of CMOS output driver.                                                                                                                                  |                                                                                       |  |
| 24      | DCOffsetlb | DC offset compensation pin for I-bar arm. A low pass capacitor shunt to Pin 25 is required.                                                                                | See pin 16 & 17 schematic                                                             |  |
| 25      | DCOffsetl  | DC offset compensation pin for I arm. A low pass capacitor shunt to Pin 24 is required.                                                                                    | See pin 14 & 15 schematic                                                             |  |
| 26      | 2IFout-lb  | Differential output pins of quadrature demodulator I output. Adding a lowpass shunt capacitor between these pins will define the IF bandwidth.                             |                                                                                       |  |
| 27      | 2IFout-l   |                                                                                                                                                                            |                                                                                       |  |
| 28      | VCC if     | Supply voltage pin of analog portion of the chip.                                                                                                                          |   |  |
| 29      | VAGC       | Gain control voltage pin of IF amplifier. This voltage performs reverse control,(i.e., VAGC up → gain down). If this pin is left open, then it is default at maximum gain. |                                                                                       |  |
| 30      | IF-in1     | Differential input pins of 1st IF AGC amplifier                                                                                                                            |                                                                                       |  |
| 31      | IF-in2     |                                                                                                                                                                            |                                                                                       |  |
| 32      | GNDanalog  | Ground pin of analog portion of the chip.                                                                                                                                  |                                                                                       |  |
| 33      | Mixout2    | Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.                                                                |  |  |
| 34      | Mixout1    |                                                                                                                                                                            |                                                                                       |  |

## PIN FUNCTIONS

| Pin No. | Symbol  | Function and Application                                                                                                                             | Internal Equivalent Circuit |
|---------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|
| 35      | Vref    | Base-emitter junction voltage with respect to ground. May be used for biasing an external discrete transistor. Regulation will develop PTAT current. |                             |
| 36      | LNAbias | LNA output pin. External bias (VCC) and matching for gain is required.                                                                               | See pin 2 schematic         |

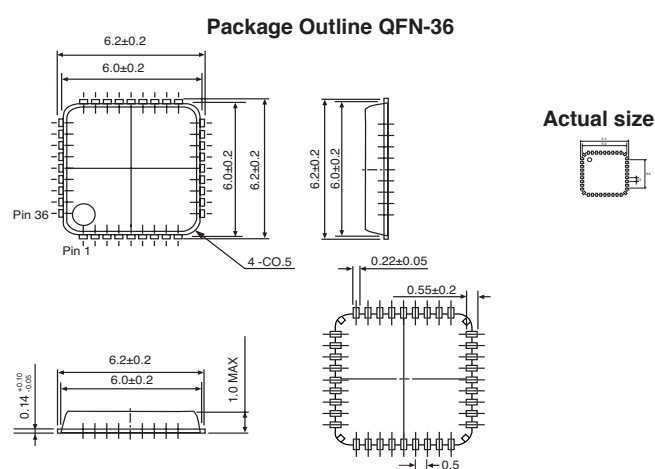
INTERNAL BLOCK DIAGRAM



ORDERING INFORMATION

| Part Number | Package            |
|-------------|--------------------|
| UPB1008K-A  | 36 Pin plastic QFN |

OUTLINE DIMENSIONS (Units in mm)



**Caution:**  
The island pins located on the corners are needed to fabricate products in our plant, but do not serve any other function.  
  
Consequently the island pins should not be soldered and should remain non-connection pins.

Life Support Applications  
These NEC products are not intended for use in life support devices, appliances, or systems where the malfunction of these products can reasonably be expected to result in personal injury. The customers of CEL using or selling these products for use in such applications do so at their own risk and agree to fully indemnify CEL for all damages resulting from such improper use or sale.

Subject: Compliance with EU Directives

CEL certifies, to its knowledge, that semiconductor and laser products detailed below are compliant with the requirements of European Union (EU) Directive 2002/95/EC Restriction on Use of Hazardous Substances in electrical and electronic equipment (RoHS) and the requirements of EU Directive 2003/11/EC Restriction on Penta and Octa BDE.

CEL Pb-free products have the same base part number with a suffix added. The suffix –A indicates that the device is Pb-free. The –AZ suffix is used to designate devices containing Pb which are exempted from the requirement of RoHS directive (\*). In all cases the devices have Pb-free terminals. All devices with these suffixes meet the requirements of the RoHS directive.

This status is based on CEL's understanding of the EU Directives and knowledge of the materials that go into its products as of the date of disclosure of this information.

| Restricted Substance<br>per RoHS | Concentration Limit per RoHS<br>(values are not yet fixed) | Concentration contained<br>in CEL devices |     |
|----------------------------------|------------------------------------------------------------|-------------------------------------------|-----|
|                                  |                                                            | -A                                        | -AZ |
| Lead (Pb)                        | < 1000 PPM                                                 | Not Detected                              | (*) |
| Mercury                          | < 1000 PPM                                                 | Not Detected                              |     |
| Cadmium                          | < 100 PPM                                                  | Not Detected                              |     |
| Hexavalent Chromium              | < 1000 PPM                                                 | Not Detected                              |     |
| PBB                              | < 1000 PPM                                                 | Not Detected                              |     |
| PBDE                             | < 1000 PPM                                                 | Not Detected                              |     |

If you should have any additional questions regarding our devices and compliance to environmental standards, please do not hesitate to contact your local representative.

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