UMC

UM6104 Series

1K× 4 CMOS SRAM

Features

- Single +5 volt Power supply
- Access times: 250/2000 ns (max.)
- Current: for UM6104 Operating: 7 mA (max.)
  Standby: 10 μA (max.)
  for UM6104-1 Operating: 5 mA (max.)
  Standby: 3 μA (max.)
- Fully static operation, no clock or refreshing required
- Directly TTL compatible: All inputs and outputs
- Common I/O using three-state output
- On-chip address register, synchronous circuitry
- Available in 18 pin DIP package

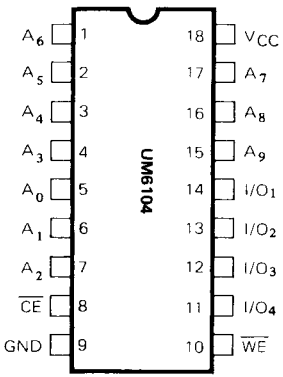
General Description

The UM6104 is a 1,024 x 4 fully static CMOS SRAM. The device utilizes synchronous circuitry to achieve high performance and low power operation.

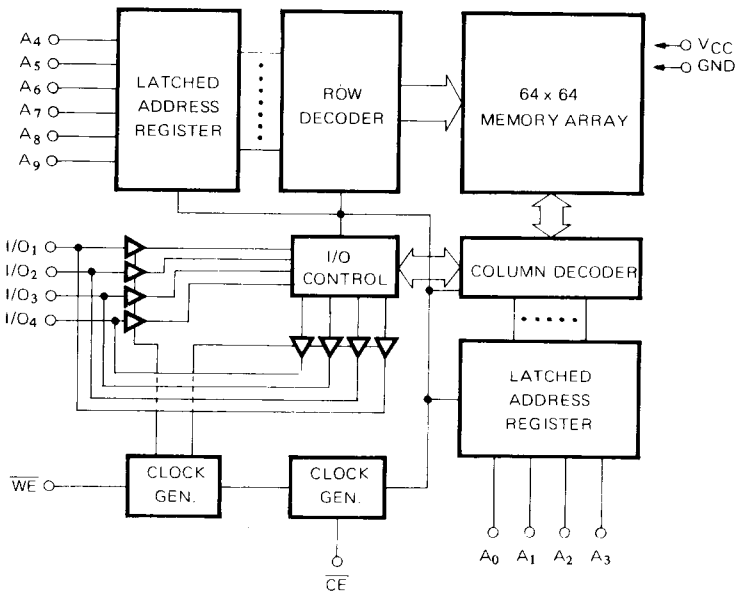
On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

UM6104-1 is usually used in low voltage or low power consumption applications such as telephonic equipment and portable devices.

Pin Configuration



Block Diagram



Pin Description

Designation	Description
$A_0 - A_9$	Address Input
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$I/O_1 - I/O_4$	Data Input/Output
V_{CC}	Power Supply (+5V)
GND	Ground

Recommended DC Operating Conditions

(T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{CC}+ 0.3V	V
V_{IL}	Input Low Voltage	−0.3	0	+0.8	V
C_L	Output Load	—	—	100	pF
TTL	Output Load	—	—	1	—

Absolute Maximum Ratings *

V_{CC} to GND . . . . . −0.5V to +7.0V

IN, IN/OUT Volt to GND . . . . . −0.5V to V_{CC} +0.3V

Operating Temperature, T_{OPR} . . . . . 0°C to +70°C

Storage Temperature, T_{STG} . . . . . −55°C to +125°C

Temperature Under Bias, T_{BIAS} . . . . . −10°C to +85°C

Power Dissipation, P_T 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, GND = 0V)

Symbol	Parameter	UM6104		UM6104-1		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
$\|I_{LI}\|$	Input Leakage Current	—	1	—	1	μA	V_{IN} = GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current	—	1	—	1	μA	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = GND to V_{CC}
I_{CC1}	Dynamic Operating Current	—	7	—	5	mA	f = 1 MHz, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0 mA
I_{SB1}	Standby Power Supply Current	—	10	—	3	μA	$\overline{CE} \geqslant V_{CC} - 0.2V$, $V_{IN} \geqslant V_{CC} - 0.2V$ or $V_{IN} \leqslant 0.2V$
V_{OL}	Output Low Voltage	—	0.4	—	0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4	—	2.4	—	V	I_{OH} = −1.0 mA

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	I/O Operation	V_{CC} Current
Standby	H	X	High Z	I_{SB1}
Read	L	H	D_{OUT}	I_{CC1}
Write	L	L	D_{IN}	I_{CC1}

Note: X : H or L

Capacitance

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}*	Input Capacitance		7	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		10	pF	$V_{I/O}$ = 0V

* This parameter is sampled and not 100% tested.

AC Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ± 100%)

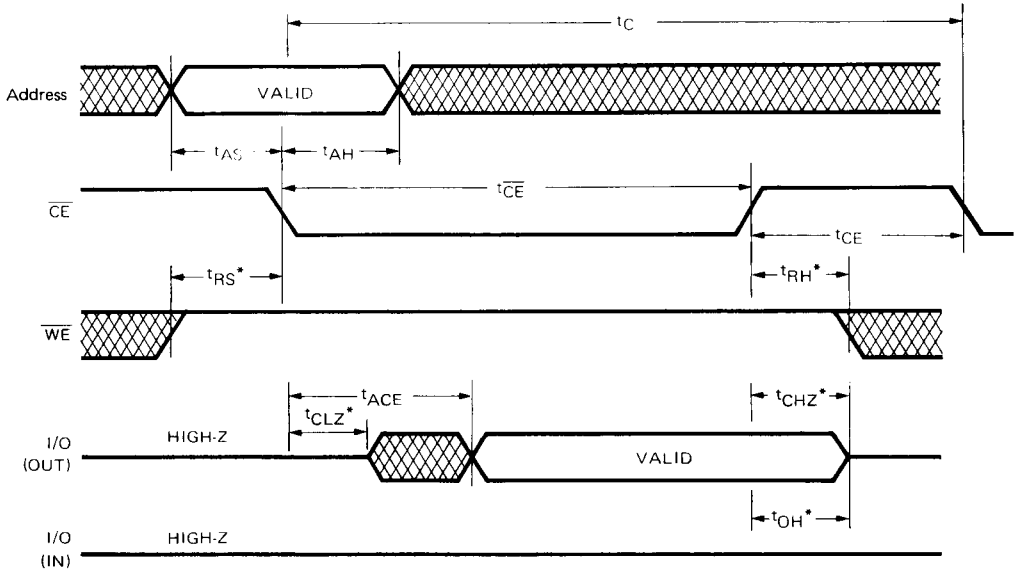
Symbol	Parameter	UM6104 Min.	UM6104 Max.	UM6104-1 Min.	UM6104-1 Max.	Unit
Read/Write Cycle						
t_C**	Read or Write Cycle Time	350	–	2500	–	ns
t_{CE}	Chip Enable Pulse Positive Width	100	–	500	–	ns
$t_{\overline{CE}}$*	Chip Enable Pulse Negative Width	250	–	2000	–	ns
t_{AS}	Address Set-up Time	20	–	100	–	ns
t_{AH}	Address Hold Time	100	–	0	–	ns
Read Cycle						
t_{ACE}	Chip Enable Access Time	–	250	–	2000	ns
t_{CLZ}	Chip Enable to Output in Low Z	50	–	100	–	ns
t_{CHZ}	Chip Disable to Output in High Z	–	80	–	500	ns
t_{OH}	Output Hold from Chip Disable or Write Enable	0	–	0	–	ns
t_{RS}	Read Set-up Time	0	–	0	–	ns
t_{RH}	Read Hold Time	0	–	0	–	ns
t_{RD}	Read Enable Time	250	–	2000	–	ns
Write Cycle						
t_{WHZ}	Write to Output in High Z	–	80	–	500	ns
t_{DW}	Data to Write Time Overlap	200	–	1500	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	ns
t_{WS}	Write Set-up Time	–20	–	–100	–	ns
t_{WD}	Write Enable Time	250	–	2000	–	ns

*For Read Modify Write Cycle, $t_{\overline{CE}} = t_{RD} + t_{WD} + t_f$

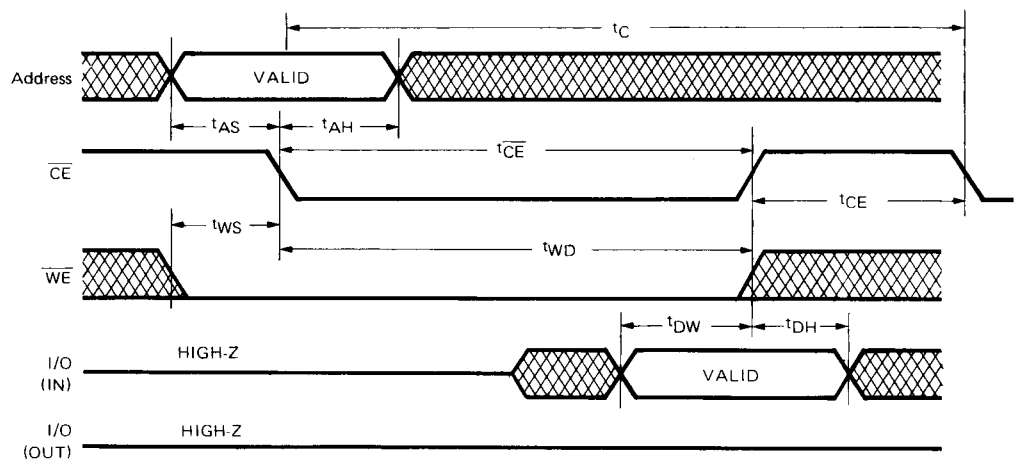
**$t_C = t_{\overline{CE}} + t_{CE} + t_R + t_F$.

Timing Waveforms

READ CYCLE TIMING DIAGRAM

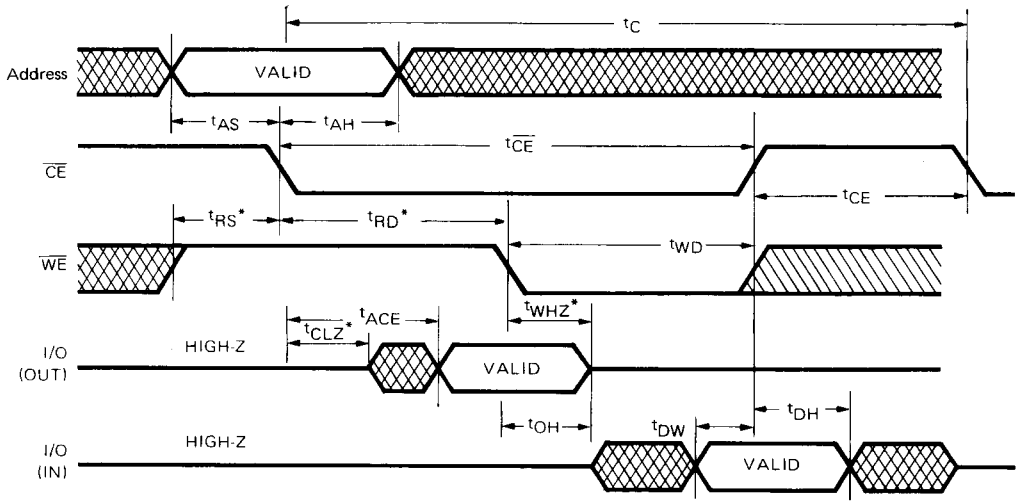


WRITE CYCLE TIMING DIAGRAM

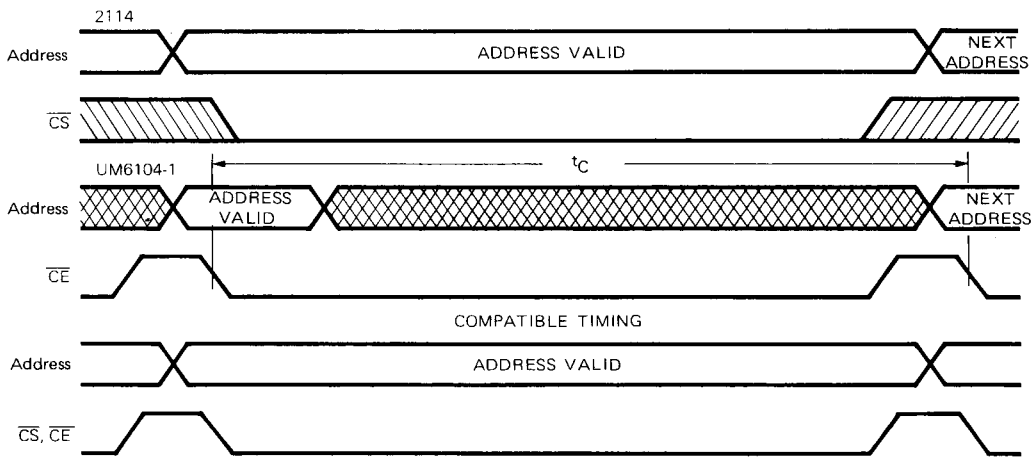


Timing Waveforms (Continued)

READ MODIFY WRITE CYCLE TIMING DIAGRAM



2114 COMPATIBILITY



2114 – REQUIRES THE ADDRESS TO REMAIN VALID THROUGHOUT THE CYCLE.

UM6104-1 – REQUIRES VALID ADDRESS FOR ONLY A SMALL PORTION OF THE CYCLE, BUT REQUIRES $\overline{CE}$ TO FALL TO INITIATE EACH CYCLE.

*This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1,2

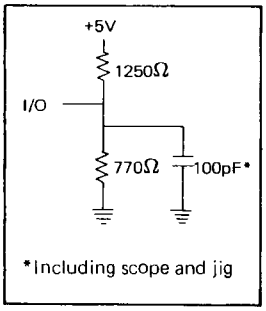


Fig. 1 Output Load

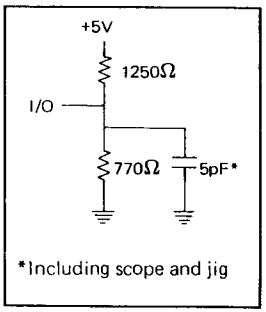


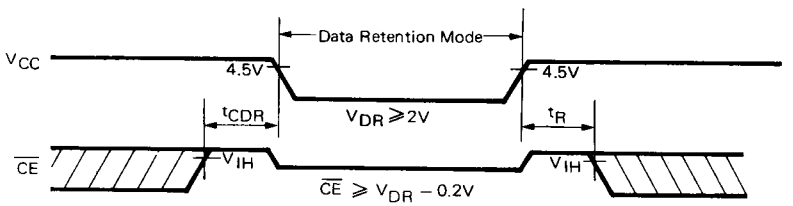
Fig. 2 Output Load for t_{CLZ}, t_{CHZ}, t_{WHZ}

Data Retention Characteristics (T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DR}	V_{CC} for Data Retention	2.0	–	V	$\overline{CE} \geq V_{CC} - 0.2V$
I_{CCDR}	Data Retention Current	–	5	μA	V_{CC} = 3.0V, $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2$
t_{CDR}	Chip Disable to Data Retention Time	0	–	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}*	–	ns	

*t_{RC} = Read Cycle Time

Low V_{CC} Data Retention Waveform



Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
UM6104	250	7	0.01	18L DIP
UM6104-1	2000	5	0.003	18L DIP