UMC

T-46-23-12

UM6116-25/-35/-45

2K× 8 High Speed CMOS SRAM

Features

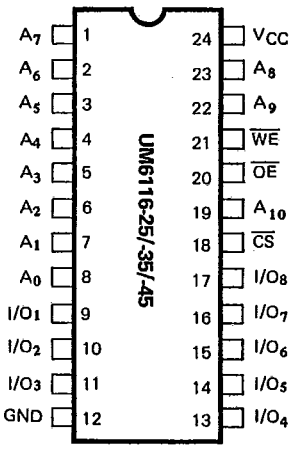
- Single +5 volt power supply
- Access times: 25/35/45 ns (max.)
- Current: Operating: 90 mA (max_f)
  Standby: 5 mA (max.)
- Fully static operation, no clock or refreshing required
- Directly TTL compatible: All inputs and outputs
- Common I/O using three-state output
- Available in 24 pin DIP or Skinny DIP packages (See ordering information page 6)

General Description

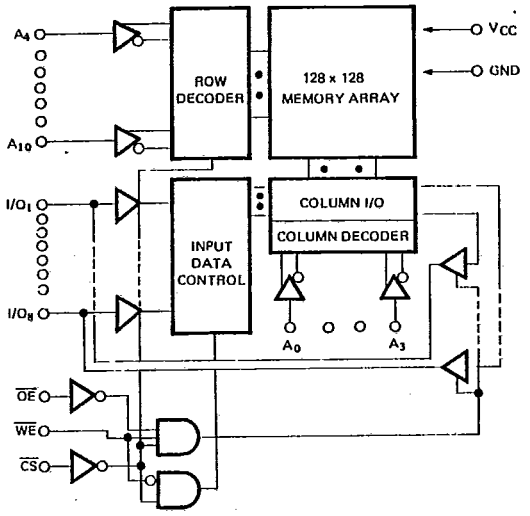
The UM6116-25/-35/-45 is a high speed 16,384-bit static random access memory organized as 2,048 words by 8 bits and operates on a single 5-volt supply. It is built with UMC's high performance CMOS process. Six-transistor, full CMOS memory cell provides low standby current and high-reliability. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

High Speed SRAM

Pin Configuration



Block Diagram



Pin Description

Designation	Description
$A_0 - A_{10}$	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
$I/O_1 - I/O_8$	Data Input/Output
V_{CC}	Power Supply (+5V)
GND	Ground

Recommended DC Operating Conditions

(T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{CC}+ 0.5	V
V_{IL}	Input Low Voltage	–0.3	0	+0.8	V
C_L	Output Load	–	–	30	pF
TTL	Output Load	–	–	1	–

Absolute Maximum Ratings *

V_{CC} to GND ..... –0.5V to +7.0V
IN, IN/OUT Voltage to GND ..... –0.5V to V_{CC} +0.5V
Operating Temperature, T_{opr} ..... 0°C to +70°C
Storage Temperature, T_{stg} ..... –55°C to +125°C
Temperature Under Bias, T_{bias} ..... –10°C to +85°C
Power Dissipation, P_T 1.0W
Soldering Temp. & Time ..... 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, GND = 0V)

Symbol	Parameter	UM6116-25/-35/-45		Unit	Test Conditions
		Min.	Max.		
$\|I_{LI}\|$	Input Leakage Current	–	10	μA	V_{IN} = GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current	–	10	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}
I_{CC}	Active Power Supply Current	–	90	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
I_{CC1}	Dynamic Operating Current	–	90	mA	Min. Cycle, Duty = 100% $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
I_{SB}	Standby Power Supply Current	–	15	mA	$\overline{CS}$ = V_{IH}
I_{SB1}		–	5	mA	$\overline{CS}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V
V_{OL}	Output Low Voltage	–	0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4	–	V	I_{OH} = –1.0 mA

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	V_{CC} Current
Standby	H	X	X	High Z	I_{SB}, I_{SB1}
Output Disabled	L	H	H	High Z	I_{CC}, I_{CC1}
Read	L	L	H	D_{OUT}	I_{CC}, I_{CC1}
Write	L	X	L	D_{IN}	I_{CC}, I_{CC1}

Note: X : H or L

Capacitance (T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}*	Input Capacitance		4	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		7	pF	$V_{I/O}$ = 0V

*This Parameter is sampled and not 100% tested.

AC Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%)

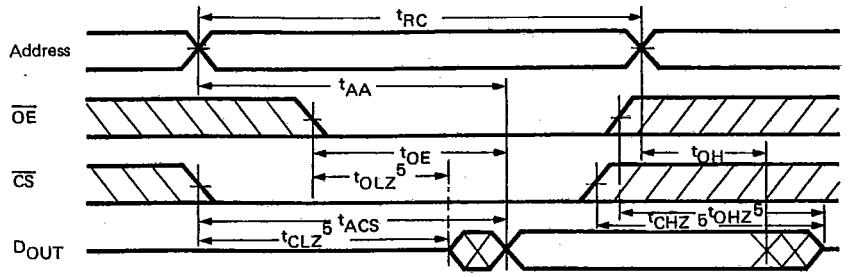
Symbol	Parameter	UM6116-25		UM6116-35		UM6116-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	25	–	35	–	45	–	ns
t_{AA}	Address Access Time	–	25	–	35	–	45	ns
t_{ACS}	Chip Select Access Time	–	25	–	35	–	45	ns
t_{OE}	Output Enable to Output Valid	–	15	–	20	–	20	ns
t_{CLZ1}	Chip Selection to Output in Low Z	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z	5	–	5	–	5	–	ns
t_{CHZ}	Chip Deselection to Output in High Z	–	12	–	15	–	15	ns
t_{OHZ}	Output Disable to Output in High Z	–	12	–	15	–	15	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	ns
Write Cycle								
t_{WC}	Write Cycle Time	25	–	35	–	45	–	ns
t_{CW}	Chip Selection to End of Write	20	–	30	–	40	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	ns
t_{AW}	Address Valid to End of Write	20	–	30	–	40	–	ns
t_{WP}	Write Pulse Width	20	–	30	–	40	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	ns
t_{WHZ}	Write to Output in High Z	–	10	–	15	–	20	ns
t_{DW}	Data to Write Time Overlap	10	–	12	–	12	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	ns
t_{OHZ}	Output Disable to Output in High Z	0	10	0	15	0	20	ns
t_{OW}	Output Active from End of Write	5	–	5	–	5	–	ns

Notes: t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

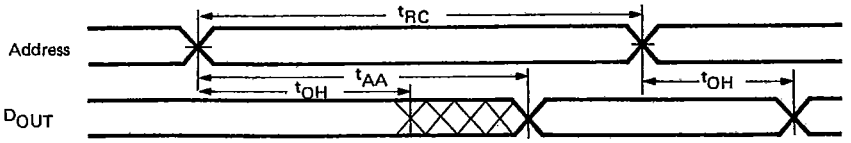
T-46-23-12

Timing Waveforms

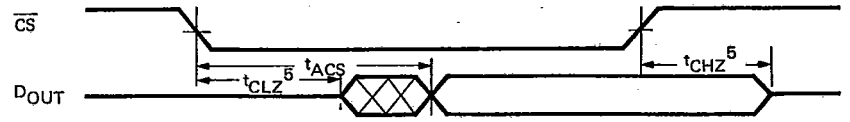
READ CYCLE 1 (1)



READ CYCLE 2 (1, 2, 4)



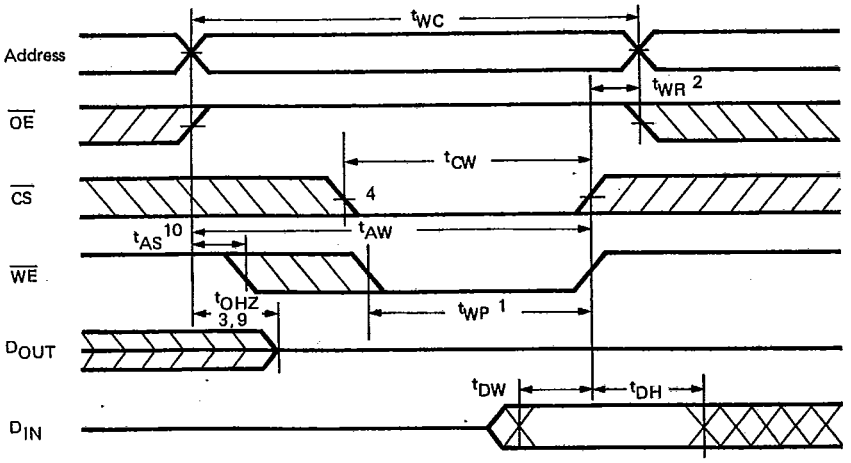
READ CYCLE 3 (1, 3, 4)



Notes:

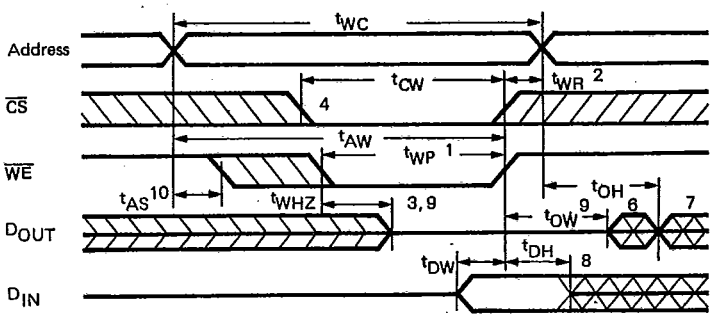
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE 1



Timing Waveforms (Continued)

WRITE CYCLE 2 (5)



Notes:

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
3. During this period, I/O pins are in the output state so the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
6. D_{OUT} is the same phase of write data of this write cycle.
7. D_{OUT} is the read data of next address.
8. If $\overline{CS}$ is low during thie period, I/O pins are in the output state. So the data input signals of opposite phase to the outputs must not be applied to I/O pins.
9. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
10. t_{AS} is measured from the address valid to the beginning of write.

High Speed SRAM

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1, 2

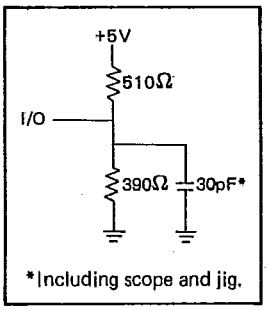


Figure 1. Output Load

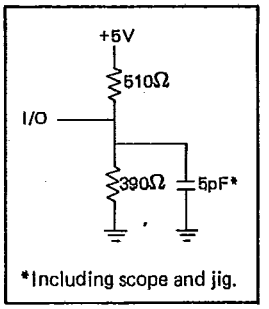
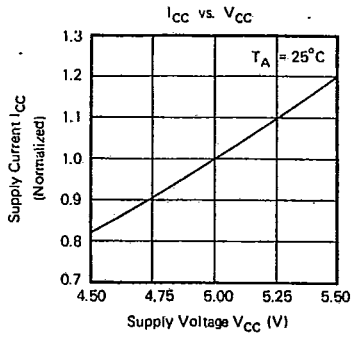
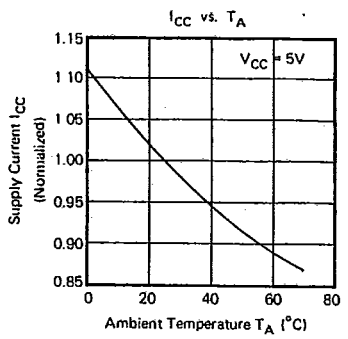
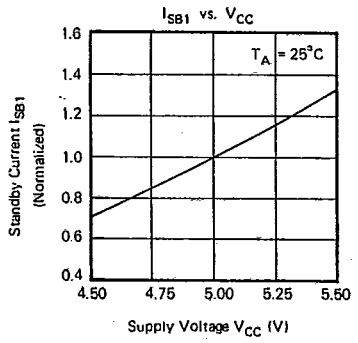


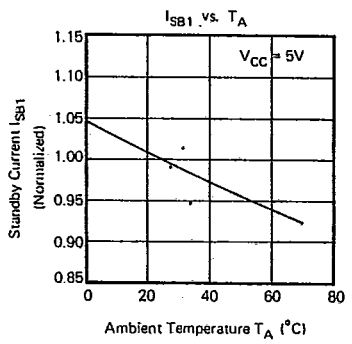
Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}

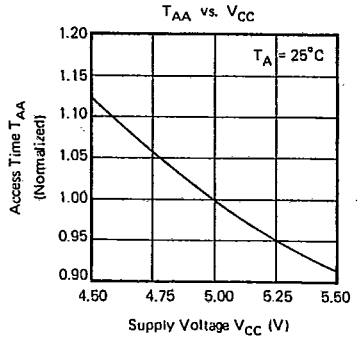
Characteristic Curves

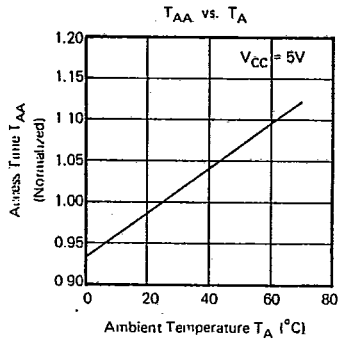












Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
UM6116-25	25 ns	90	5	24L DIP
UM6116-35	35 ns	90	5	24L DIP
UM6116-45	45 ns	90	5	24L DIP
UM6116K-25	25 ns	90	5	24L Skinny DIP
UM6116K-35	35 ns	90	5	24L Skinny DIP
UM6116K-45	45 ns	90	5	24L Skinny DIP