

ELECTRICAL SPECIFICATIONS:

1.0 INDUCTANCE: (P1-J1);(P2-J2);(P3-J3);(P4-J6) : 30 uH MIN. @0.01V, 10KHz
(P5-J4);(P6-J5);(P7-J7);(P8-J8) : 30 uH MIN. @0.01V, 10KHz
(P1-J1);(P2-J2);(P3-J3);(P4-J6) : 10 uH MIN @0.01V, 10KHz, 40mA
(P5-J4);(P6-J5);(P7-J7);(P8-J8) : 10 uH MIN @0.01V, 10KHz, 40mA

2.0 DC RESISTANCE:
P6-J5; P7-J7; P8-J8; P3-J3; P4-J6; P5-J4; P2-J2; P1-J1 : 0.2 OHM MAX

3.0 LEAKAGE INDUCTANCE: : 0.15 uH @ 1MHz MAX

4.0 COMMON MODE: (SEE FIGURE 1)

FREQUENCY (MHz)	CMA (-dB)	
	TYPICAL	MIN
1	8	5
5	17	15
20	23	15
70	25	20
200	22	17
500	11	6

5.0 DIELECTRIC WITHSTAND: (P1-J1 TO P2-J2); (P3-J3 TO P4-J6) : 1500VAC
(P5-J4 TO P6-J5); (P7-J7 TO P8-J8) : 200VAC

* ALL CARRYING CONDUCTORS SHALL HAVE CROSS SECTION AREA GREATER THAN
WIRE SIZE 36AWG.



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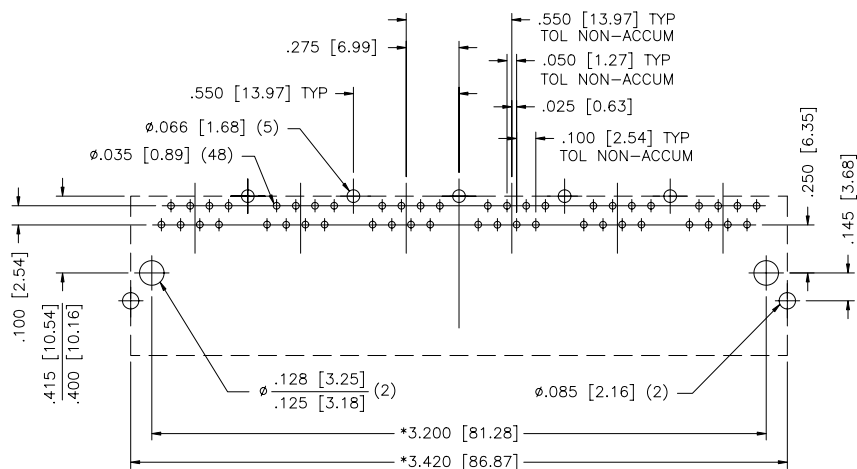
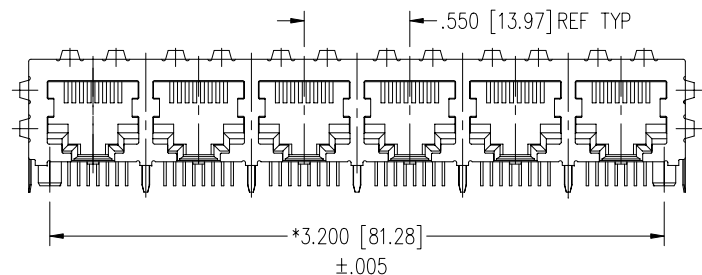
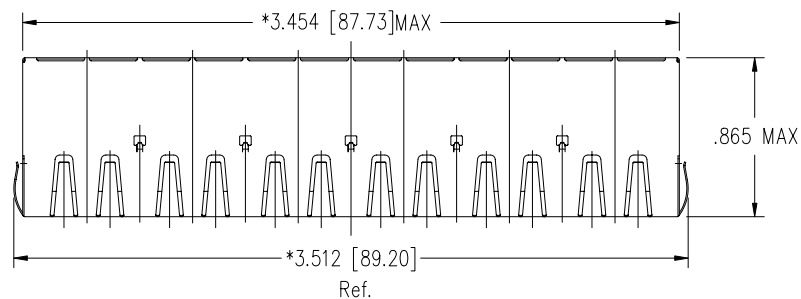


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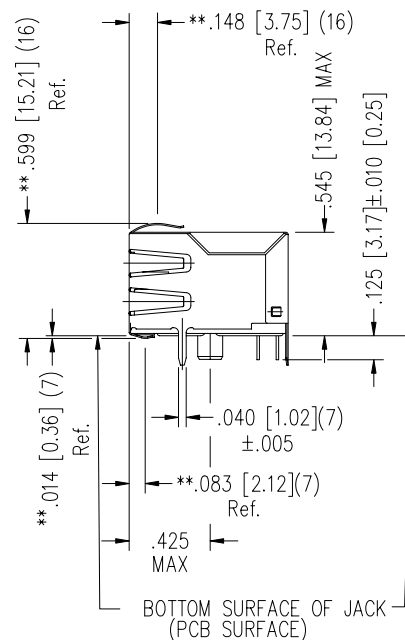
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P.C.B. RECOMMENDED HOLE LAYOUT
SEEN FROM COMPONENT SIDE
TOLERANCE ±.003 [0.08] UNLESS OTHERWISE SPECIFIED

NOTES:

- TOLERANCES COMPLY WITH F.C.C. DIMENSION REQUIREMENTS
- DIMENSIONS SHOWN WITH "*" TO BE CENTRAL ABOUT CENTER LINE
- "***" ON DIMENSION INDICATES HIGHEST POINT OF BEAM
- PINS NOT ELECTRICALLY CONNECTED MAYBE OMITTED. SEE ELECTRICAL DRAWING FOR OMITTED PINS.
- STANDARD 50 MICRO-INCH SELECTIVE GOLD PLATING
- ALL POLYMERS FLAMMABILITY - UL94V0



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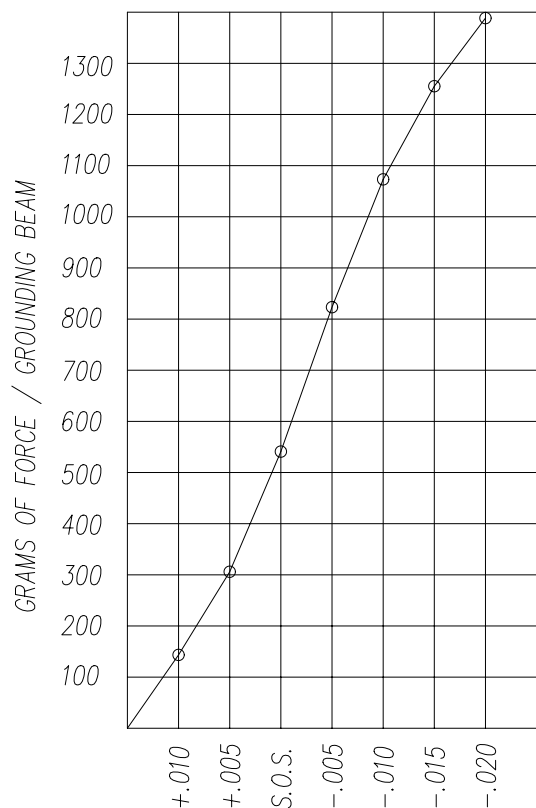
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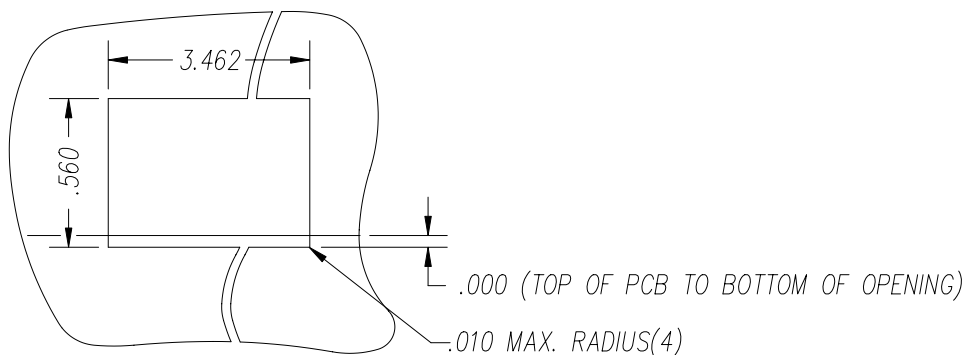
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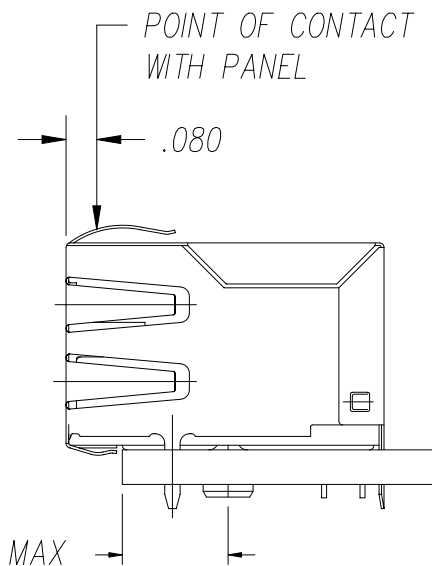


PANEL GROUNDING BEAM DEFLECTION
S.O.S. = SUGGESTED OPENING SIZE



SUGGESTED PANEL OPENING

CT660100X2



THE SUGGESTED PANEL OPENING IS INTENDED TO GIVE THE USER THE ABILITY TO HAVE REASONABLE JACK / PANEL CLEARANCES YET MAINTAIN RELIABLE GROUNDING CAPABILITY. THESE VARIABLES CAN BE ADJUSTED IN EITHER DIRECTION BUT MAY CARRY SOME CONSEQUENCES IN THE FORM OF LOWER MATING FORCES OR TIGHTER ASSEMBLY TOLERANCES. FORCE VALUES ON THE GRAPH ARE GENERAL AVERAGES TAKEN AT THE POINT OF CONTACT SHOWN ABOVE. THE SUGGESTED PANEL OPENING INCLUDES APPROXIMATELY .020 CLEARANCE ON THE SIDES AND TOP AND .005 ON THE BOTTOM.



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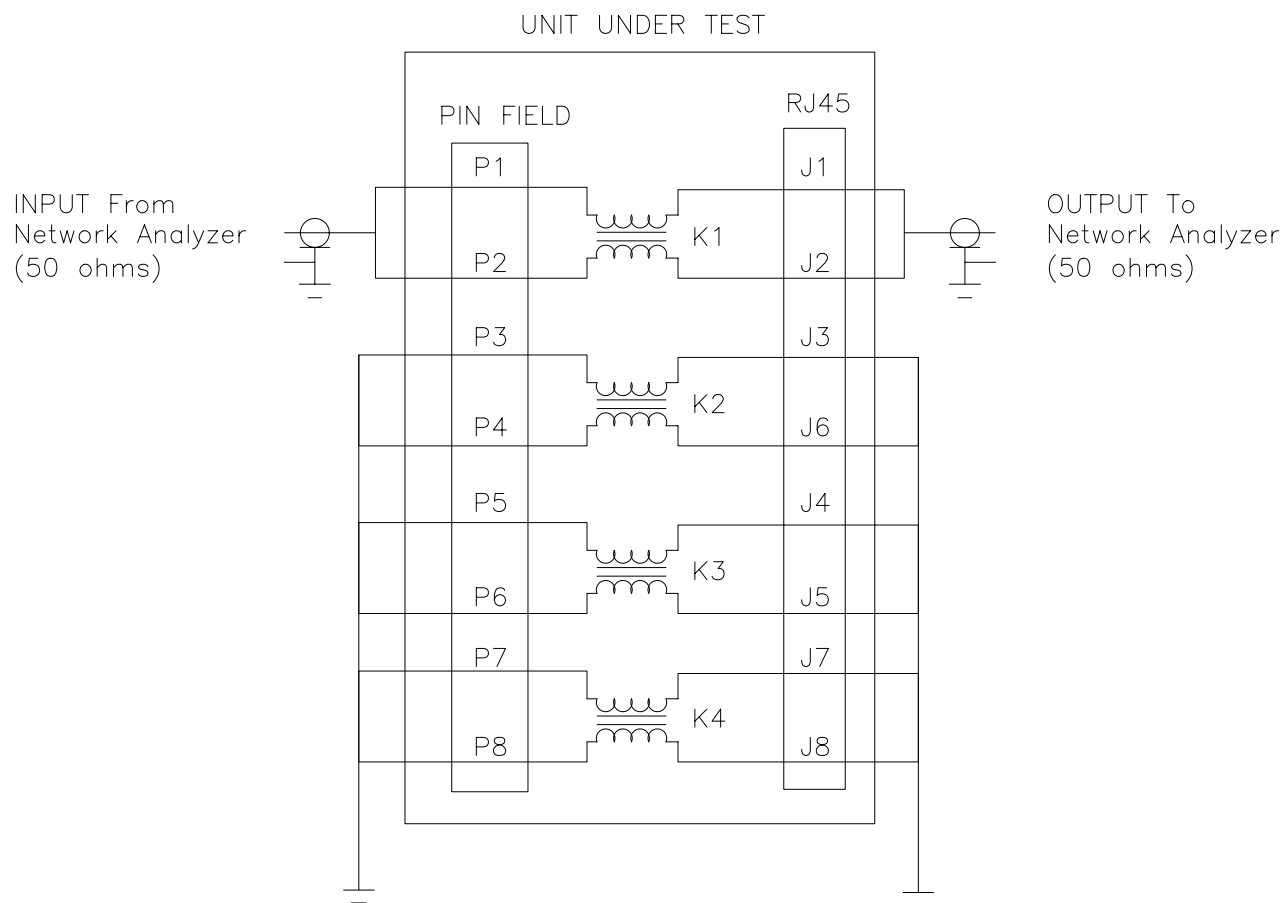
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NOTE: Setup shown for P1/P2 to J1/J2 path.
Measurements for each signal pair to be taken
with other circuits connected to ground

FIGURE 1: TEST SETUP FOR COMMON MODE REJECTION



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