Typical Applications

Base Stations
Test + Measurement

Features

Surface Mount Package
Reflow Process Compatible
Low Phase Noise
Build in PLL-Circuit

Output Frequency range 10 MHz – 160 MHz

Standard frequencies 10; 25; 26; 39.3216; 52; 56; 61.44;77.76; 104 MHz
122.88; 153.6; 155.52; 160 MHz

Reference Frequency

Parameter	Min	Typ	Max.	Units	Condition	Ordering Code[5]
Input frequency	2		100	MHz	± 2 ppm	
Parameter	**Min**	**Typ**	**Max.**	**Units**	**Condition**	
Signal		HCMOS				IFH
Reference Level	0.5		4	V_{pp}	HCMOS / similar sinewave	
Reference Input Impedance	2			kΩ		

Output Frequency

Parameter	Min	Typ	Max.	Units	Condition	Ordering Code[5]
output frequency	10		160	MHz		
Signal		HCMOS				RFH
Load		15.0		pF		
Rise and Fall time			5	ns	@ 15 pF 10 to 90 %	
Duty cycle	40		60	%	@ Vs/2	

Supply voltage (Vs)

Parameter	Min	Typ	Max.	Units	Condition	Ordering Code[5]
Supply voltage [Standard]	3.135	3.3	3.465	VDC		SV033
Current consumption			50	mA	steady state @ +25°C & 3.3VDC	

Additional parameters

Parameter	Min	Typ	Max.	Units	Condition	
Phase Noise[3]		-90		dBc/Hz	10 Hz	@ 122,88 MHz
		-110		dBc/Hz	100 Hz	HCMOS
		-131		dBc/Hz	1 kHz	
		-148		dBc/Hz	10 kHz	
		-156		dBc/Hz	100 kHz	
		-157		dBc/Hz	1 MHz	
Jitter		0.77		ps RMS	@ 10Hz .. 150kHz	

Additional parameters

Parameter	Min	Typ	Max.	Units	Condition
Weight			9	g	
Processing & Packing		Handling & processing note			
Operating temperature range	-20		+70	°C	
Operable temperature range	-30		+85		
Storage temperature range	-55		+125	°C	

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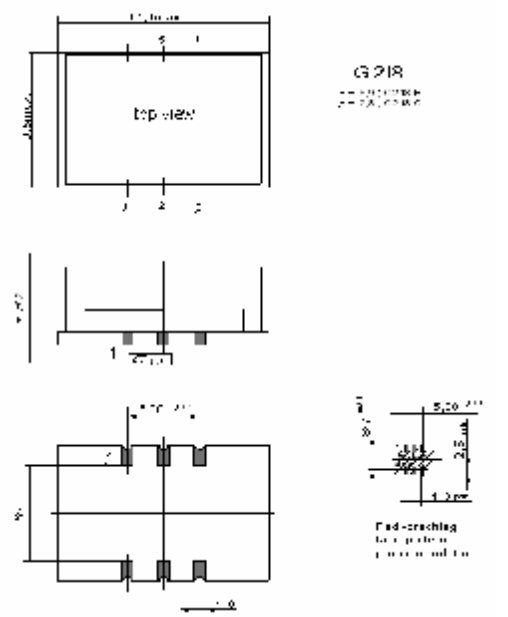
Type G218B
Input : Single ended (HCMOS or Sinewave)
Output : Single ended HCMOS

Code	Height "H"	Pin Length "L"
A1	5.9	NA



Dimensions : mm

	Pin Connections	Description
1	Ref. Frequency in	High stable input frequency for syncronisation
2	VCXO Control	**Test output** of the control voltage for the VCXO Only for modul test or observance
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance
4	RF-OUT	RF syncronised output.
5	Lock Detector Output	**Test output** signal for PLL lock detected. High signal **à** PLL in lock Low signal **à** PLL out of lock Only for modul test or observance
6	Vs	Power supply pin

Marking
C3310A1-xxxx Frequency * VI AYYWW

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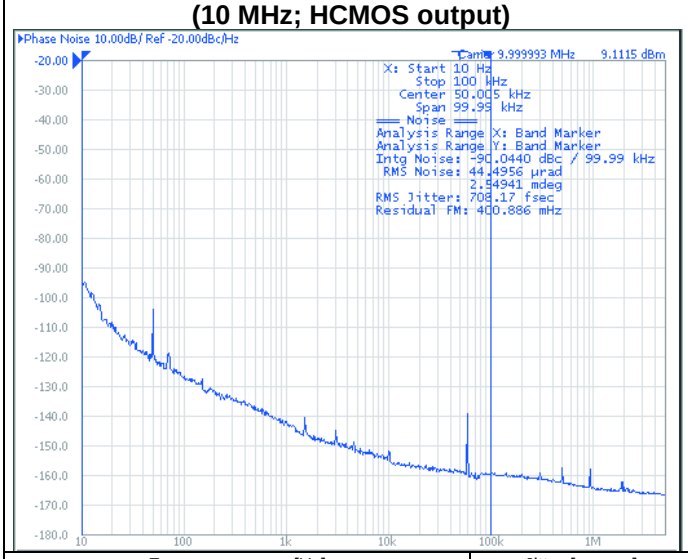
Absolute Maximum Ratings

Parameter	Min	Typ	Max.	Units	Condition
Supply voltage (Vs)			**6.0**	V	
Maximum output load @ CMOS			40	pF	

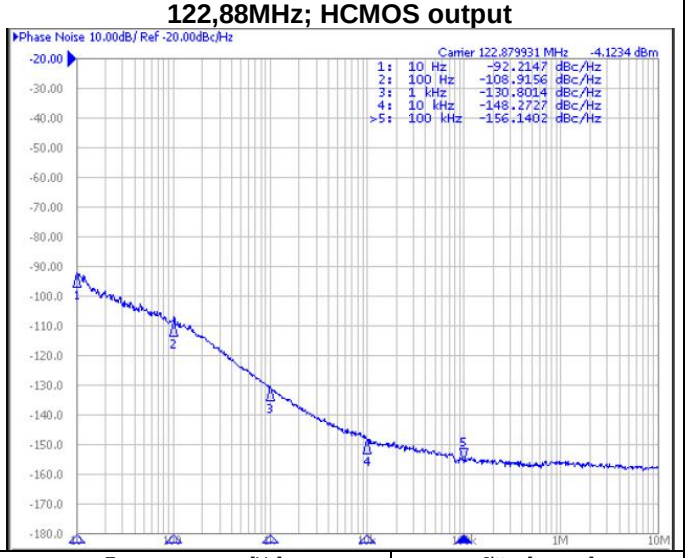
Typical Phase Noise and Jitter

(10 MHz; HCMOS output)



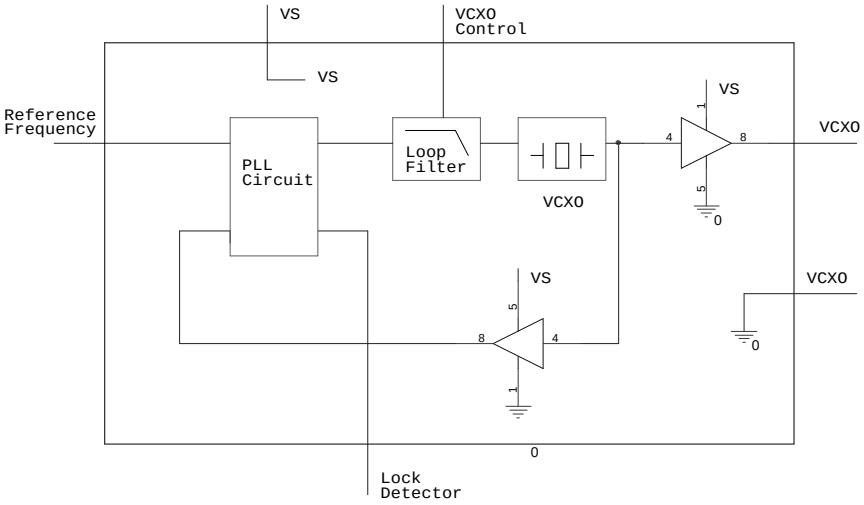
Frequency range [Hz]	Jitter [ps rms]
10Hz to 100kHz	0.708ps

122,88MHz; HCMOS output



Frequency range [Hz]	Jitter [ps rms]
10Hz to 150kHz	0,775ps

Block Diagramm



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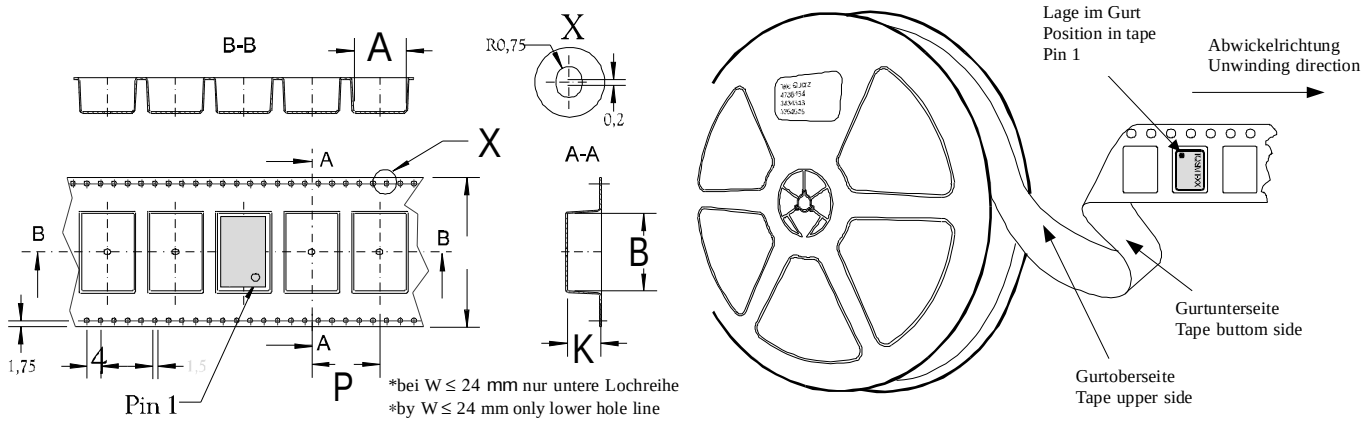
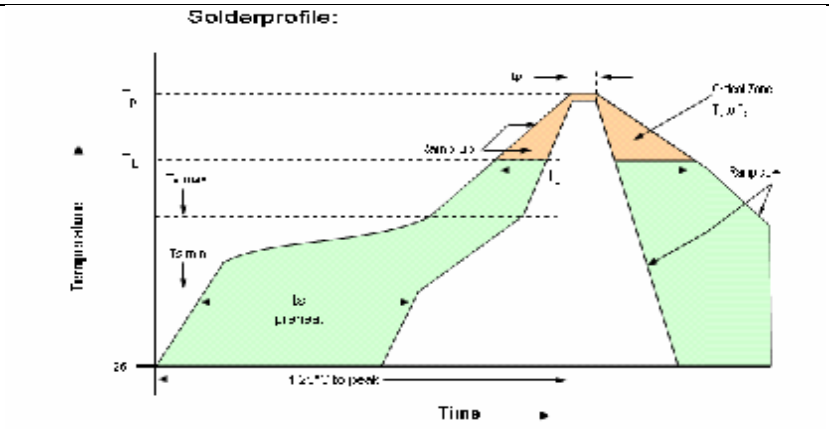
Standard Shipping Method



Production tolerance complying DIN IEC 286-3

Enclosure Type	Tape width W [mm]	Quantity per meter	Quantity per reel	Dimension P	
G218B	tbd	tbd	850	tbd	

Recommended Reflow Profile



Profile Feature	Pb-Free Assembly /Sn-Pb Assembly	Profile Feature	Pb-Free Assembly /Sn-Pb Assembly
Average ramp-up rate (T_L to Tp)	3°C/second max.	Time 25°C to Peak Temperature	8 minutes max.
Preheat -Temperature Min Ts_{min}) -Temperature Min Ts_{max}) -Time (min to max) (ts)	150°c 200°c 60-180 seconds	Time maintained above - Temperature (T_L) - Time (t_L)	 217°C 60-150 seconds
Ts_{max} to T_L - Ramp-up Rate	3°C/second max.		
Time maintained above - Temperature (T_L) - Time (t_L)	217°C 60-150 seconds	Time within 5°C of actual Peak Temperature (tp)	20-40 seconds
Peak Temperature (Tp)	max 260°C	Ramp-down Rate	6°C/second max.

Note: All temperatures refer to topside of the package, measured on the package body surface.
SMD oscillators must be on the top side of the PCB during the reflow process.

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How to Order this Product:

Model	Ref. Freq	Freq out	Supply Voltage Code	RF Output Code	Package Code
C3310			SV033	RFH	A1

Supply:

SV033: 3.3V

Signal:

RFH: HCMOS

Enclosures:

A1: H: 5.9 L: NA

Dimension: mm

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