# 8-CHANNEL POWER SUPPLY SEQUENCER AND MONITOR

## FEATURES

- **Single Supply Voltage: 3.3 V**
- **Low Power Consumption**
- **Sequences and Monitors up to 8 Voltage Rails**
- **Rail Voltages Sampled Every 50 $\mu$s With 3.2-mV Resolution**
- **Four Configurable Digital Outputs for Power-On-Reset and Other Functions**
- **Configurable Rail Enable Output Polarity**
- **Flexible Rail Sequencing: Timeline (ms), Parent Rail Regulation Window, Parent Rail Achieving Defined Threshold**
- **Under and Overvoltage Thresholds: Settable Per-Rail**
- **Regulation Expiration Time: Settable Per-Rail**
- **Flexible Rail Shutdown: Parent Rail Shutdown can Shutdown Child Rails, Independent Rail Configuration**
- **Per-Rail Alarm Conditions, with Timestamp: Under and Overvoltage Glitch, Sustained Under and/or Overvoltage, Rail Did Not Start**
- **I²C Interface for Configuration and Monitoring**
- **Microsoft Windows™ GUI for Configuration and Monitoring**

## APPLICATIONS

- **Telecommunications Switches**
- **Servers**
- **Networking Equipment**
- **Test Equipment**
- **Any System Requiring Sequencing of Multiple Voltage Rails**

## DESCRIPTION

The UCD9080 Power Supply Sequencer controls the enable sequence of up to 8 independent voltage rails and provides four general purpose digital outputs. The device operates from a 3.3-V supply, provides 3.2-mV resolution of voltage rails, and requires no external memory or clock. The UCD9080 monitors the voltage rails independently at more than a 20 kHz rate and has a high degree of rail sequence and rail error response configurability. The sequencing of rails can be based on timed events, or timed events in conjunction with other rails achieving regulation or a voltage threshold. In addition, each rail is monitored for undervoltage and overvoltage glitches and thresholds. Each rail the UCD9080 monitors can be configured to shutdown a user-defined set of other rails, and alarm conditions are monitored on a per-rail basis.

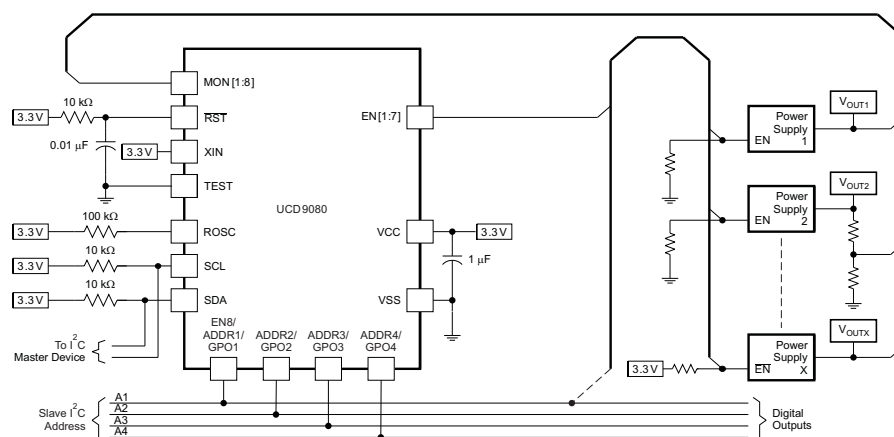Figure 1 shows the UCD9080 Power Supply Sequencer in a typical application

**PRODUCT PREVIEW**



**Figure 1. Typical Application Diagram**

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| $T_A$ | PACKAGED DEVICES [1][2] | MSOP SYMBOL |
|---|---|---|
| −40°C to 85°C | UCD9080RHBR | RHB |
| | UCD9080RHBT | |

(1) The package is available taped and reeled. Add the R suffix for reeled quantities. Add the T suffix for taped quantities.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS[1]

| | | VALUE | UNIT |
|---|---|---|---|
| | Voltage applied at VCC to VSS | −0.3 to 4.1 | V |
| | Voltage applied to any pin[2] | −0.3 to $V_{CC}$ + 0.3 | V |
| | Diode current at any device terminal | ±2 | mA |
| $T_{stg}$ | Storage temperature | −40 to 85 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to $V_{SS}$.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage during operation | 3 | 3.3 | 3.6 | V |
| | Supply during configuration changes | 3 | 3.3 | 3.6 | |
| $T_A$ | Operating free-air temperature range | −40 | | 85 | °C |

## ELECTRICAL CHARACTERISTICS

These specifications are over recommended ranges of supply voltage and operating free-air temperature, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $I_S$ | Supply current into $V_{CC}$ excluding external current | $V_{CC}$ = 3 V | | 300 | 350 | µA |
| $I_C$ | Supply current during configuration | 2.5 V / 3.6 V | 3 | | 7 | mA |
| **STANDARD INPUTS (RST, TEST)** | | | | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 3 V | $V_{SS}$ | | $V_{SS}$ +0.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 3 V | 0.8×$V_{CC}$ | | $V_{CC}$ | V |
| **SCHMITT TRIGGER INPUTS (SDA, SCL, ADDR1, ADDR2, ADDR3, ADDR4)** | | | | | | |
| $V_{IT+}$ | Positive-going input threshold voltage | $V_{CC}$ = 3 V | 1.5 | | 1.9 | V |
| $V_{IT−}$ | Negative-going input threshold voltage | $V_{CC}$ = 3 V | 0.9 | | 1.3 | V |
| $V_{hys}$ | Input voltage hysteresis, ($V_{IT+}$− $V_{IT−}$) | $V_{CC}$ = 3 V | 0.5 | | 1 | V |
| $I_{lkg}$ | High impedance leakage current | RST, TEST, SDA, SCL, ADDR1, ADDR2, ADDR3, ADDR4 | | | ±50 | nA |

## ELECTRICAL CHARACTERISTICS (continued)

These specifications are over recommended ranges of supply voltage and operating free-air temperature, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG INPUTS (MON1, MON2, MON3, MON4, MON5, MON6, MON7, MON8, ROSC)** | | | | | | | |
| $V_{CC}$ | Analog supply voltage | $V_{SS} = 0$ V | | 1.8 | | 3.6 | V |
| $V_{CC}$(min) | $V_{CC}$ minimum voltage when sampling | | | 2.35 | | | V |
| $V_{(R<1..8>)}$ | Analog input voltage | Internal voltage reference | | 0 | | 2.5 | V |
| | | External voltage reference ($V_{CC} = 3.3$ V used as reference) | | 0 | | $V_{CC}$ | |
| $C_I$ [1] | Input capacitance | Only one terminal can be selected at a time (MON1–MON8) | | | | 27 | pF |
| $R_I$ [1] | Input MUX ON resistance | $0$ V $\leq$ VAx $\leq$ VCC, $V_{CC} = 3$ V | | | | 2000 | Ω |
| $I_{lkg}$ | High-impedance leakage current | MON1–MON8 | | | | ±50 | nA |
| VREF+ | Positive internal reference voltage output | REF2_5V = 1 for 2.5 V $I_{(VREF+)} \leq I_{(VREF+)}$max | $V_{CC} = 3$ V | 2.35 | 2.5 | 2.65 | V |
| | | REF2_5V = 0 for 1.5 V $I_{(VREF+)} \leq I_{(VREF+)}$max | $V_{CC} = 3$ V | 1.41 | 1.5 | 1.59 | V |
| $V_{CC}$(min) | VCC minimum voltage, Positive built-in reference active | REF2_5V = 0, $I_{(VREF+)} \leq 1$ mA | | 2.2 | | | V |
| | | REF2_5V = 1, $I_{(VREF+)} \leq 0.5$ mA | | $V_{REF+} + 0.15$ | | | V |
| | | REF2_5V = 1, $I_{(VREF+)} \leq 1$ mA | | $V_{REF+} + 0.15$ | | | V |
| $V_{(acc)}$ | Accuracy of voltage sampling from rails | Internal reference (2.5 V) | | ±6.8 | ±12 | ±17.4 | mV |
| | | External reference (3.3 V/$V_{CC}$) | | ±0.2 | ±1.6 | ±6.8 | |
| $T_{REF+}$ [1] | Temperature coefficient of built-in reference | $I_{(VREF+)}$ is a constant in the range of $0$ mA $\leq I_{(VREF+)} \leq 1$ mA, VCC = 3 V | | | | ±100 | ppm/°C |
| **DCO OPERATING PERIOD** | | | | | | | |
| $t_{(PERIOD)}$ | | $V_{CC} = 3$ V, $T_A = 25$°C, $R_{OSC} = 100$ kΩ | | 227 | 204 | 185 | nS |
| **MISCELLANEOUS** | | | | | | | |
| $T_{retention}$ | Retention of configuration parameters | $T_J = 25$°C | | 100 | | | Years |
| **POR, Brownout, Reset (see [2][3])** | | | | | | | |
| $t_{d(BOR)}$ | | | | | | 2000 | µs |
| $VCC_{(start)}$ | | | | | 0.7×V(B_IT-) | | V |
| $V_{(B\_IT-)}$ | Brownout | dVCC/dt $\leq 3$ V/s | | | | 1.71 | V |
| $V_{hys(B\_IT-)}$ | | | | 70 | 130 | 180 | mV |
| $t_{(reset)}$ | | Pulse length needed at RST pin to accept reset internally, $V_{CC} = 3$ V | | 2 | | | µs |
| **DIGITAL OUTPUTS (EN8/GPO1, GPO2, GPO3, GPO4, EN1, EN2, EN3, EN4, EN5, EN6, EN7, SDA)** | | | | | | | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$(max) = −1.5 mA, [4] $V_{CC} = 3$ V | | $V_{CC} - 0.25$ | | $V_{CC}$ | V |
| | | $I_{OH}$(max) = −6 mA, [5] $V_{CC} = 3$ V | | $V_{CC} - 0.6$ | | $V_{CC}$ | |
| $V_{OL}$ | VOL Low-level output voltage | $I_{OH}$(max)= −1.5 mA, [4] $V_{CC} = 3$ V | | $V_{SS}$ | | $V_{SS} + 0.25$ | V |
| | | $I_{OH}$(max) = −6 mA, [5] $V_{CC} = 3$ V | | $V_{SS}$ | | $V_{SS} + 0.6$ | |
| $I_{lkg}$ | High-impedance leakage current | $V_{CC} = 3$ V | | | | ±50 | nA |

(1) Not production tested. Limits verified by design.
(2) The current consumption of the brown-out module is already included in the $I_{CC}$ current consumption data.
(3) During power up, device initialization starts following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$.
(4) The maximum total current, $I_{OH}$max and $I_{OL}$max, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
(5) The maximum total current, $I_{OH}$max and $I_{OL}$max, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

The UCD9080 is compatible with 3.3-V IO ports of microcontrollers, TMS320™ DSP Family as well as ASICs. The UCD9080 is available in a plastic 32-pin QFN package (RHB).
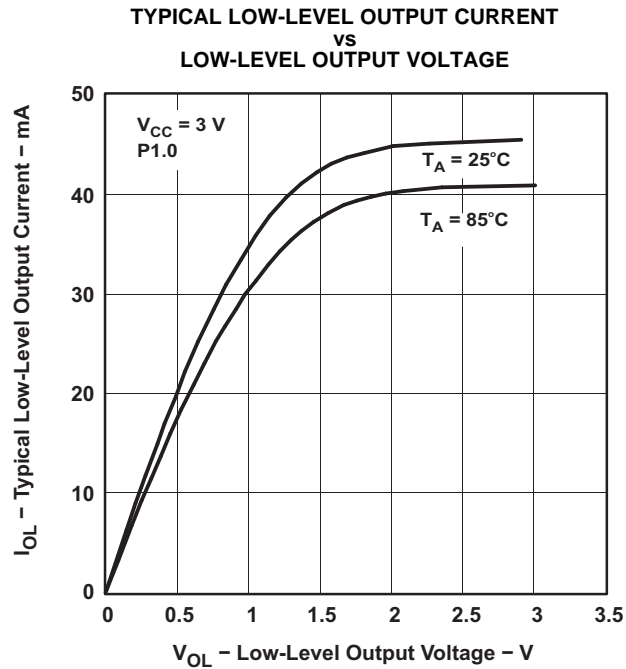
**PRODUCT PREVIEW**

**PRODUCT PREVIEW**

## DIGITAL OUTPUTS (only one output is loaded at a time)

**TYPICAL LOW-LEVEL OUTPUT CURRENT**
**vs**
**LOW-LEVEL OUTPUT VOLTAGE**

$V_{CC}$ = 3 V
P1.0

$T_A$ = 25°C

$T_A$ = 85°C

$I_{OL}$ − Typical Low-Level Output Current − mA

$V_{OL}$ − Low-Level Output Voltage − V

**Figure 2.**

**TYPICAL HIGH-LEVEL OUTPUT CURRENT**
**vs**
**HIGH-LEVEL OUTPUT VOLTAGE**

$V_{CC}$ = 3 V
P1.0

$T_A$ = 85°C

$T_A$ = 25°C

$I_{OH}$ − Typical High-Level Output Current − mA

$V_{OH}$ − High-Level Output Voltage − V

**Figure 3.**

$V_{CC}$

$V_{hys(B\_IT-)}$

$V_{(B\_IT-)}$

$V_{CC(start)}$

1

Set signal for
POR circuitry

0

$t_{d(BOR)}$

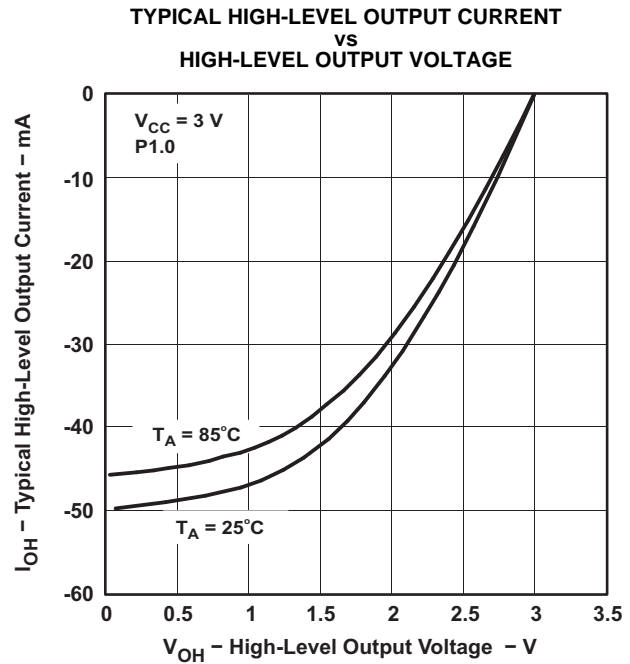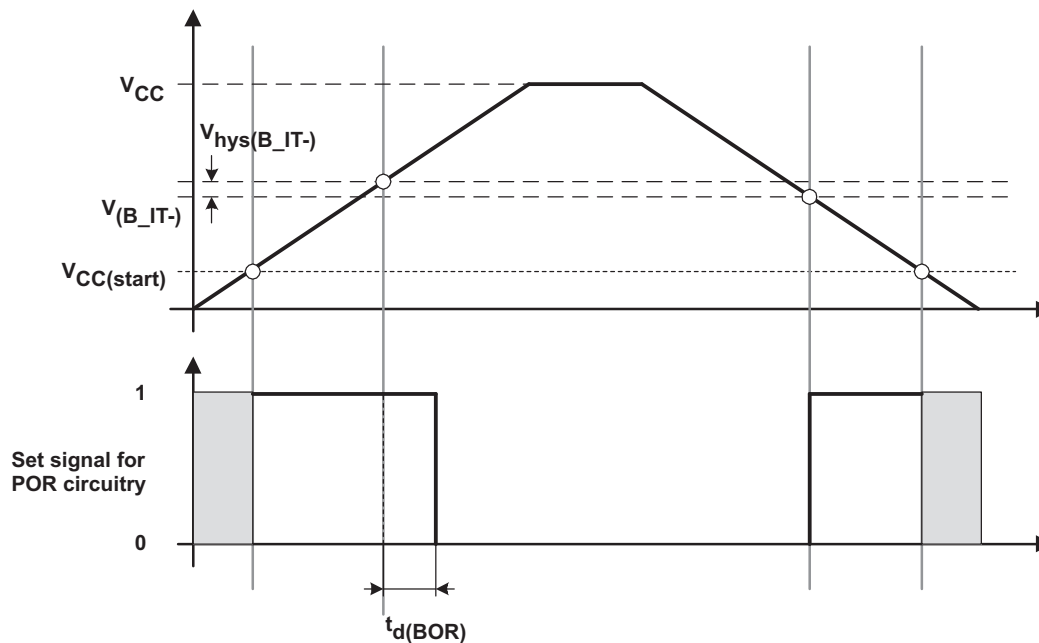**Figure 4. POR/Brownout Reset (BOR) vs Supply Voltage**

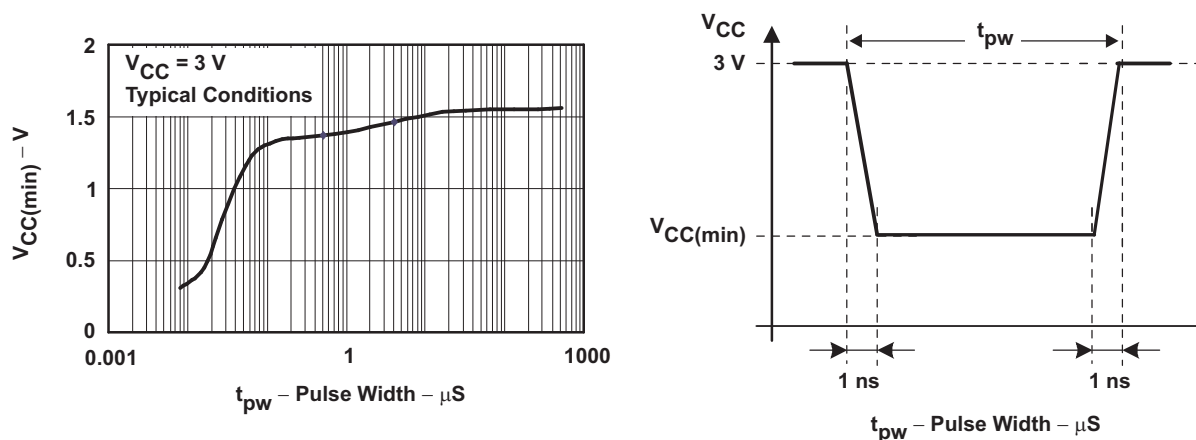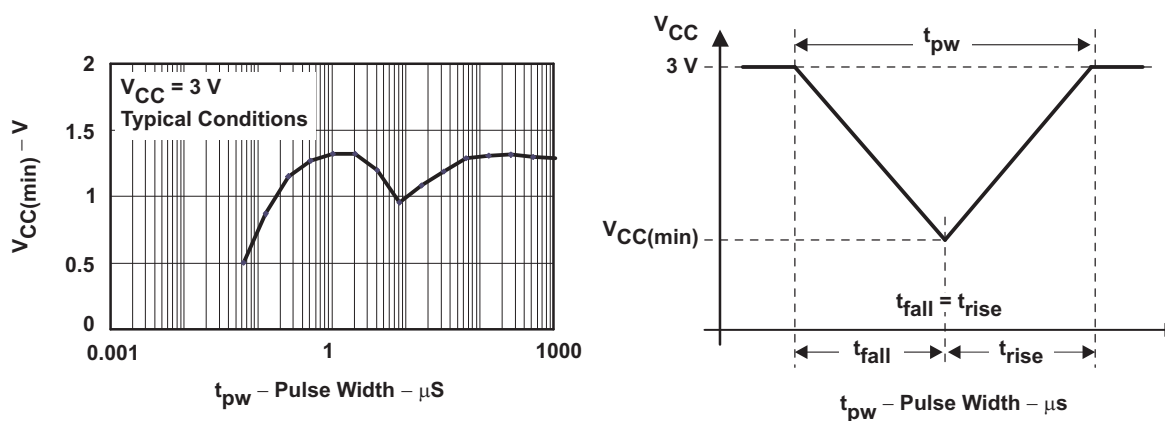**Figure 5. V<sub>CC(min)</sub> Level With a Square Voltage Drop to Generate a POR/Brownout Signal**

**Figure 6. V<sub>CC(min)</sub> Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal**

**PRODUCT PREVIEW**

## I²C TIMING

The UCD9080 supports the same timing parameters as "Standard-Mode" I²C. See the timing diagram and timing parameters below for more information.
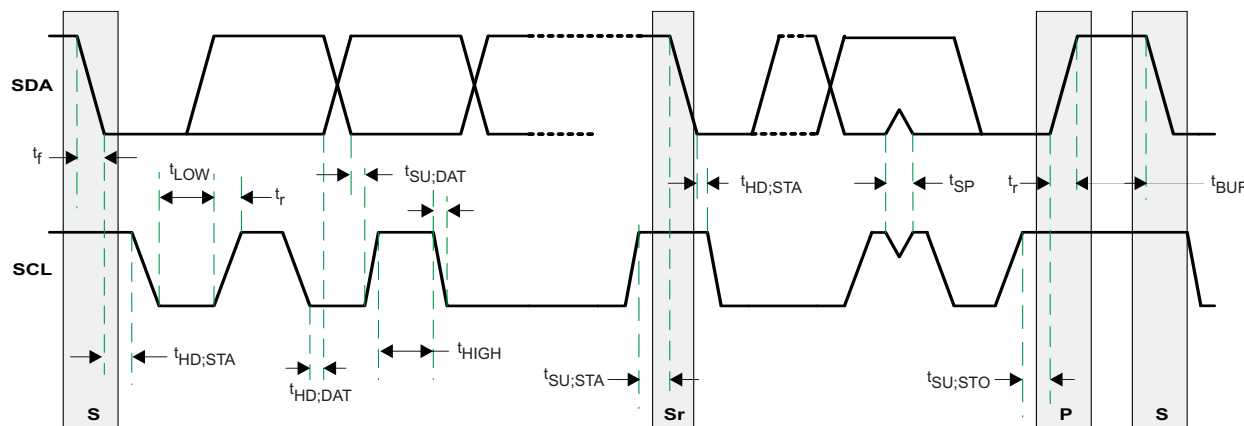
**Figure 7. Timing Diagram for I²C Interface**

## TIMING PARAMETERS FOR I$^2$C INTERFACE

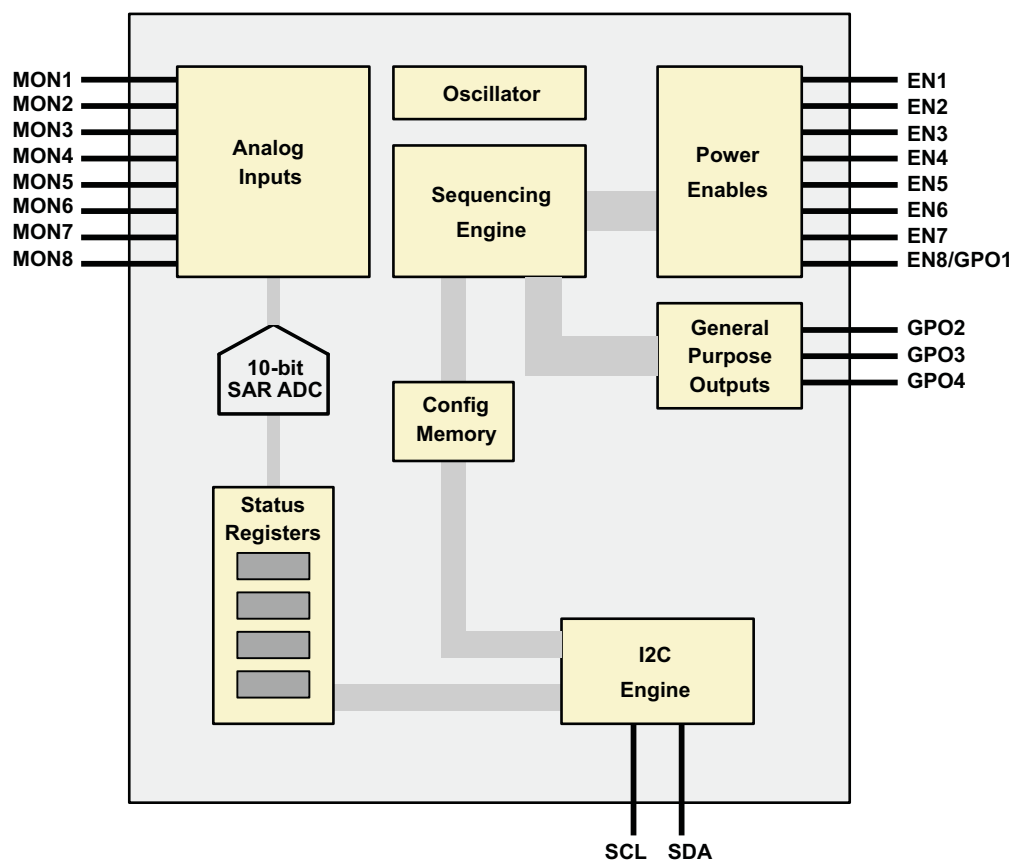| | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{of}$ | Output fall time from $V_{OH}$ to $V_{OL}$ [1] with a bus capacitance from 10 pF to 400 pF. | | 250[2] | ns |
| $C_I$ | Capacitance for each pin. | | 10 | pF |
| $f_{SCL}$ | SCL Clock Frequency | 10 | 100 | kHz |
| $t_{HD;STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4 | | µs |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | 4 | | µs |
| $t_{SU;STA}$ | Set-up time for repeated start condition | 4.7 | | µs |
| $t_{SU;DAT}$ | Data set-up time | 250 | | ns |
| $t_r$ | Rise time of both SDA and SCL signals | | 1000 | ns |
| $t_f$ | Fall time of both SDA and SCL signals | | 300 | ns |
| $t_{SU;STO}$ | Set-up time for STOP condition | 4 | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | | µs |
| $C_{(b)}$ | Capacitive load for each bus line | | 400 | pF |
| $V_{nL}$ | Noise margin at the LOW level for each connected device (including hysteresis) | 0.1 VDD | | V |
| $V_{nH}$ | Noise margin at the HIGH level for each connected device (including hysteresis) | 0.2 VDD | | V |

(1)  See the *Electrical Characteristics* section of this data sheet.
(2)  The maximum $t_f$ for the SDA and SCL bus lines (300 ns) is longer than the specified maximum $t_{of}$ for the output stages (250 ns). This allows series protection resistors ($R_s$) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_f$.

**RHB PACKAGE
(TOP VIEW)**

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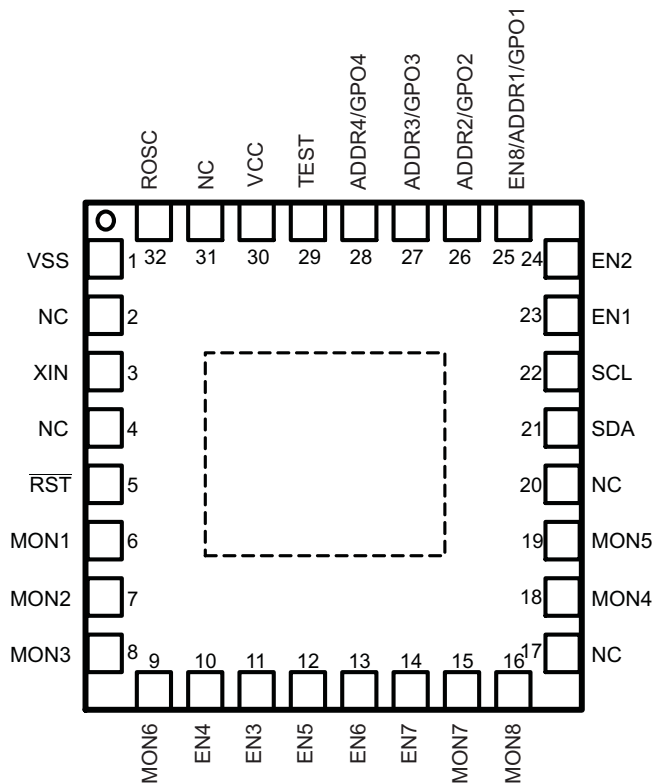
## TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| **NAME** | **NO.** | | |
| VSS | 1 | | Ground reference |
| NC | 2, 4,17, 20, 31 | | Not connected internally. Connect to VSS. |
| XIN | 3 | | Connect to VCC |
| $\overline{\text{RST}}$ | 5 | I | Reset input. |
| MON1 | 6 | I | Analog input for voltage rail 1. |
| MON2 | 7 | I | Analog input for voltage rail 2. |
| MON3 | 8 | I | Analog input for voltage rail 3. |
| MON6 | 9 | I | Analog input for voltage rail 6. |
| EN4 | 10 | O | Voltage rail 4 enable (digital output). |
| EN3 | 11 | O | Voltage rail 3 enable (digital output). |
| EN5 | 12 | O | Voltage rail 5 enable (digital output). |
| EN6 | 13 | O | Voltage rail 6 enable (digital output). |
| EN7 | 14 | O | Voltage rail 7 enable (digital output). |
| MON7 | 15 | I | Analog input for voltage rail 7. |
| MON8 | 16 | I | Analog input for voltage rail 8. |
| MON4 | 18 | I | Analog input for voltage rail 4. |
| MON5 | 19 | I | Analog input for voltage rail 5. |
| SDA | 21 | I/O | I$^2$C data (bi-directional). Must pull-up to 3.3 V. |
| SCL | 22 | I | I$^2$C clock. Must pull-up to 3.3 V. |
| EN1 | 23 | O | Voltage rail 1 enable (digital output). |
| EN2 | 24 | O | Voltage rail 2 enable (digital output). |
| EN8 /ADDR1/ GPO1 | 25 | I/O | Voltage rail 8 enable (digital output), I$^2$C address select 1, general-purpose digital output 1 |
| ADDR2/GPO2 | 26 | I/O | I$^2$C address select 2, general-purpose digital output 2. |
| ADDR3/GPO3 | 27 | I/O | I$^2$C address select 3, general-purpose digital output 3. |
| ADDR4/GPO4 | 28 | I/O | I$^2$C address select 4, general-purpose digital output 4. |
| TEST | 29 | I | Connect to VSS |
| VCC | 30 | | Supply voltage. |
| ROSC | 32 | | Internal oscillator frequency adjust. Must use 100 K pull-up to VCC for minimum drift and maximum frequency when sampling voltage rails. |

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# FUNCTIONAL BLOCK DIAGRAM

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MON1
MON2
MON3
MON4
MON5
MON6
MON7
MON8

**Analog Inputs**

**Oscillator**

**Sequencing Engine**

**Power Enables**

EN1
EN2
EN3
EN4
EN5
EN6
EN7
EN8/GPO1

**General Purpose Outputs**

GPO2
GPO3
GPO4

**10-bit SAR ADC**

**Config Memory**

**Status Registers**

**I2C Engine**

SCL   SDA

## FUNCTIONAL DESCRIPTION

### POWER SUPPLY SEQUENCING

The UCD9080 can be configured to sequence the power rails using the enable signals or the general-purpose outputs in one of three ways:

The first way is to specify a delay time after a sequence event. A sequence event includes a device reset (including power-on-reset), a RESET command, or a resequence action. The enable/GPO is asserted after the sequence event plus specified delay.

The second way is to specify a delay time after another (parent) rail has achieved regulation (Vrail is within specified under and overvoltage settings). The enable/GPO is asserted after the (parent) rail is in regulation plus specified delay.

The third way is to specify a (parent) rail voltage. The enable/GPO is asserted after the (parent) rail voltage is greater than or equal to the specified voltage.

Of course, a rail does not have to be sequenced. This could be used in the case of a backplane voltage which is not under the control of the UCD9080, but is being monitored.

### POWER SUPPLY ENABLES

The UCD9080 can sequence and enable/disable up to 8 power supplies through the ENx (EN1 to EN8) signals on the device. These signals can be configured for either active high or active low, to support power supplies that use either polarity.

The enable signals for up to 8 power supplies can be sequenced by the UCD9080 as described below. Note that the EN8 is used for $I^2C$ address selection, General-purpose output as well as the enable signal for the voltage rail 8. This means that this signal is unavailable until the UCD9080 has selected its $I^2C$ address. If the system requires the GPO1 signal, then this signal is not available for power supply enable sequencing.

The enable signals on the UCD9080 are not intended to drive the gate of N-channel MOSFET. These pins are LVCMOS level only, providing the capability of driving either logic high or low (3.3 V or 0 V).

Note that while the UCD9080 is not operating, the state of the enable signals is not defined. If these signals need to be defaulted to the disabled state, according to the power supply definition, then they should be pulled up or down accordingly on the board.

### VOLTAGE REFERENCE

The UCD9080 has a voltage reference that is selectable via the $I^2C$ interface and parameter configuration section. The voltage reference can either be an internally generated 2.5-V reference or an external 3.3-V reference. If the external voltage reference is selected, then the 3.3-V reference is from the $V_{CC}$ supply to the UCD9080.

Depending on the voltage reference that is being used, the accuracy of reading voltages is affected. The internal reference is not as accurate as the external reference and affects the accuracy of the sampled voltages of the monitored rails. See the *Electrical Characteristics* for information on voltage reading accuracy for use with each of the references.

The section on *Configuring the UCD9080* details how to select the internal or external voltage reference.

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## FUNCTIONAL DESCRIPTION (continued)

### GENERAL-PURPOSE OUTPUTS

The UCD9080 can control up to 4 general-purpose digital outputs through the same sequencing mechanisms as described below. These general-purpose outputs (referred to as GPO1–GPO4) can be used for digital signals such as RESET signals or LEDs on a board. Note that these signals are multiplexed with other functions (primarily $I^2C$ address selection) so be sure to consult the pin functions section to make sure that these are used properly by the application. Also note that the GPO1 signal is multiplexed with EN8, so both of these cannot be used at the same time.

### BROWNOUT

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

### $I^2C$ INTERFACE

The UCD9080 Power Supply Sequencer has an $I^2C$ slave interface for communication with an $I^2C$ master for configuration and monitoring of the power supply sequencer and rails. The UCD9080 supports slave-mode operation for a 100 kHz $I^2C$ bus. This interface is used for configuring the UCD9080 as well as monitoring each of the voltage rails and reporting the voltage of each independently

### $I^2C$ Address Selection

The UCD9080 supports 7-bit $I^2C$ addressing. The UCD9080 supports selection of an $I^2C$ address by sampling of 4 digital inputs to the device (ADDR1–ADDR4) and selecting an $I^2C$ address, based on the digital state of each of these signals. When the UCD9080 is released from reset, these four signals are sampled. Based on the state of these four signals, the $I^2C$ slave address is assigned to the UCD9080 as shown in Figure 8.

| A7 = 1 | A6 = 1 | A5 = 0 | A4 = ADDR4/GPO4 | A3 =ADDR3/GPO3 | A2 = ADDR2/GPO2 | A1 = EN8/ADDR1/GPO1 |
|--------|--------|--------|-----------------|----------------|-----------------|---------------------|

**Figure 8. $I^2C$ ADDRESS = 0x60–0x6F**

External pull-up/pull-down resistors are required to configure the $I^2C$ address; the UCD9080 does not have internal bias resistors. Note that the 7-bit $I^2C$ address refers to the address bits only, not the read/write (8th) bit in the first byte of the $I^2C$ protocol. The base $I^2C$ address is 0x60 and the $I^2C$ general call address (0x00) is not supported.

After the initialization process of the UCD9080 is complete, these four digital signals can be used for general-purpose outputs of the sequencer. They can be programmed and sequenced as described later in this document.

### $I^2C$ Transactions

The UCD9080 can be configured and monitored via $I^2C$ memory-mapped registers. Registers that are configurable (can be written) via an $I^2C$ write operation are implemented using an $I^2C$ unidirectional data transfer, from the master to slave, with a stop bit between transactions

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## I²C Unidirectional Transfer

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | R/$\overline{W}$ | A | REGISTER ADDRESS | A | DATA | A/$\overline{A}$ | P |

'0' (write)

Data transferred (n bytes + acknowledge)

From master to slave

From slave to master

A = acknowledge (SDA low)

$\overline{A}$ = Not acknowledge (SDA high)

S = START condition

P = STOP condition
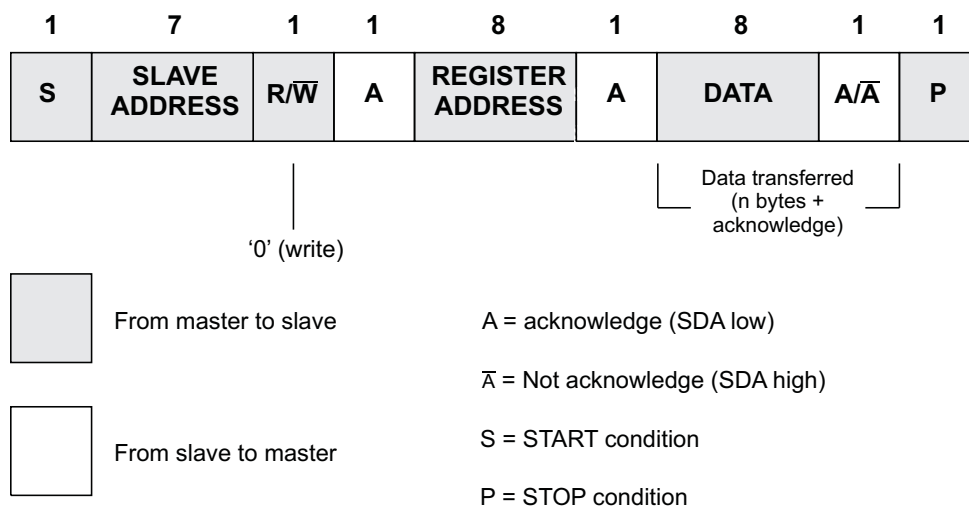
**Figure 9. I²C Register Access With START/STOP**

Registers that can be read are implemented using an I²C read operation, which uses the I²C combined format that changes data direction during the transaction. This transaction uses an I²C restart during the direction change.

## I²C Combined Format

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | R/$\overline{W}$ | A | REGISTER ADDRESS | A | Sr | SLAVE ADDRESS | R/$\overline{W}$ | A | DATA | A/$\overline{A}$ | P |

'0' (write)

'1' (read)

(n bytes + ack)

From master to slave

From slave to master

A = acknowledge (SDA low)

$\overline{A}$ = Not acknowledge (SDA high)

S = START condition

P = STOP condition

Sr = Repeated START
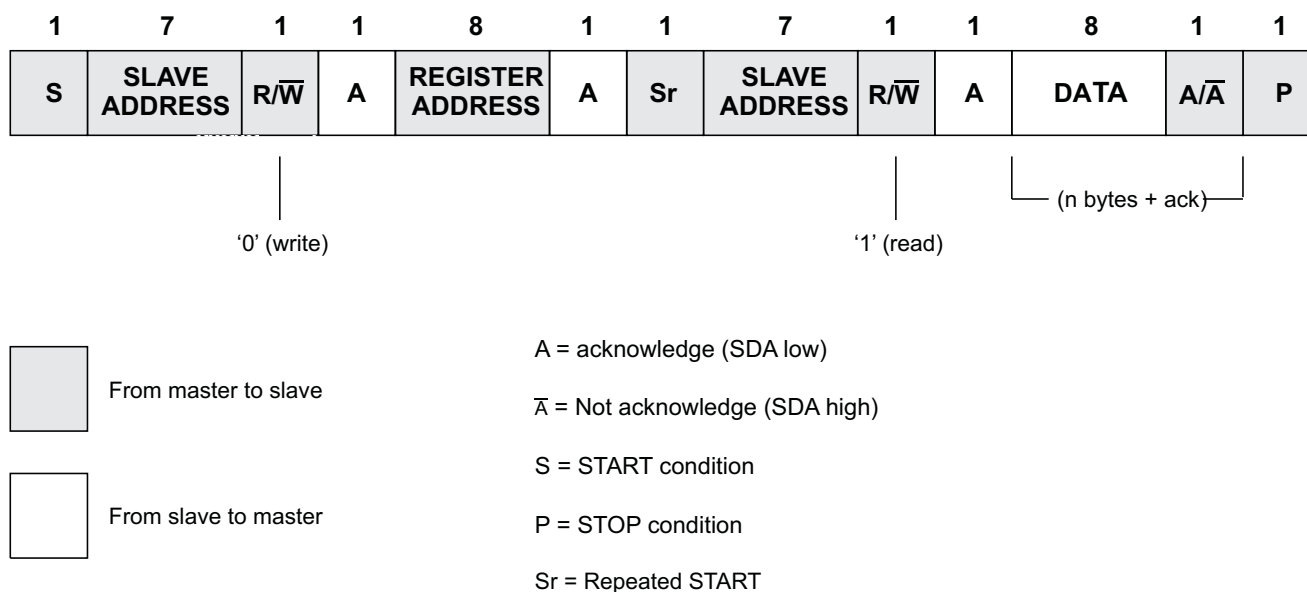
**Figure 10. I²C Register Access with RESTART**

The UCD9080 also supports a feature that auto-increments the register address pointer for increased efficiency when accessing sequential blocks of data. It is not necessary to issue separate I²C transactions..

## CONFIGURING AND MONITORING THE UCD9080

The UCD9080 supports both configuration and monitoring using its I$^2$C slave interface.

For monitoring of the sequencer, there is an I$^2$C memory map that is used that allows an I$^2$C host to perform memory mapped reads (and in some cases writes) that reports status information from the UCD9080. For instance, all rails can report their voltage through the I$^2$C memory map. For information on which parameters are available via the I$^2$C memory map, see the *Monitoring the UCD9080* section.

To change configuration parameters of the sequencer, a different mechanism is used. The entire set of configuration parameters must be written at one time to the device as one large transaction over the I$^2$C interface. This ensures that the configuration of the device is consistent at any given time. The process for configuring the UCD9080 is described below in the section titled *Configuring the UCD9080* section.

## MONITORING THE UCD9080

### Register Map

The UCD9080 allows all monitoring of the system through the I$^2$C interface on the device. The following is the memory map of the supported registers in the system. The detail of each of these registers is given in the next section as well.

Note that the UCD9080 supports functionality to automatically increment the I$^2$C register address value when a register is being accessed, to more efficiently access blocks of like registers. The table below also shows the amount that the register address is incremented for each register access.

| REGISTER NAME | ADDRESS | ACCESS | ADJUSTMENT AFTER ACCESS |
|---|---|---|---|
| RAIL1H | 0x00 | r | +1 (0x01) |
| RAIL1L | 0x01 | r | +1 (0x02) |
| RAIL2H | 0x02 | r | +1 (0x03) |
| RAIL2L | 0x03 | r | +1 (0x04) |
| RAIL3H | 0x04 | r | +1 (0x05) |
| RAIL3L | 0x05 | r | +1 (0x06) |
| RAIL4H | 0x06 | r | +1 (0x07) |
| RAIL4L | 0x07 | r | +1 (0x08) |
| RAIL5H | 0x08 | r | +1 (0x09) |
| RAIL5L | 0x09 | r | +1 (0x0A) |
| RAIL6H | 0x0A | r | +1 (0x0B) |
| RAIL6L | 0x0B | r | +1 (0x0C) |
| RAIL7H | 0x0C | r | +1 (0x0D) |
| RAIL7L | 0x0D | r | +1 (0x0E) |
| RAIL8H | 0x0E | r | +1 (0x0F) |
| RAIL8L | 0x0F | r | −15 (0x00) |
| ERROR1 | 0x20 | r | +1 (0x21) |
| ERROR2 | 0x21 | r | +1 (0x22) |
| ERROR3 | 0x22 | r | +1 (0x23) |
| ERROR4 | 0x23 | r | +1 (0x24) |
| ERROR5 | 0x24 | r | +1 (0x25) |
| ERROR6 | 0x25 | r | −5 (0x20) |
| STATUS | 0x26 | r | +0 (0x26) |
| RAILSTATUS1 | 0x28 | r | +1 (0x29) |
| RAILSTATUS2 | 0x29 | r | −1 (0x28) |
| FLASHLOCK | 0x2E | rw | 0 (0x2E) |
| RESTART | 0x2F | w | +0 (0x2F) |

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| REGISTER NAME | ADDRESS | ACCESS | ADJUSTMENT AFTER ACCESS |
|---|---|---|---|
| WADDR1 | 0x30 | rw | +1 (0x31) |
| WADDR2 | 0x31 | rw | − 1 (0x30) |
| WDATA1 | 0x32 | w | +1 (0x33) |
| WDATA2 | 0x33 | w | −1 (0x32) |

### Register Descriptions

The following are the detailed descriptions of each of the UCD9080 I$^2$C registers.

The register bit conventions below are used. Each register is shown with a key indicating the accessibility of each bit, and the initial condition after device initialization.

| KEY | ACCESS |
|---|---|
| rw | Read/Write |
| r | Read only |
| r0 | Read as 0 |
| r1 | Read as 1 |
| w | Write only |
| w0 | Write as 0 |
| w1 | Write as 1 |
| rc | Read clears bit after read |
| rs | Read sets bit after read |
| −0, −1 | Condition after initialization |

### RAIL

Each of the 8 voltage rails that the UCD9080 supports has two registers that contains the rolling average voltage for the associated rail as measured by the device. This average voltage is maintained in real-time by the UCD9080 and is calculated as the output of a 4-TAP FIR filter. There are two registers for each voltage rail. One holds the least-significant 8 bits of the voltage and the other the most-significant 2 bits of the voltage. This is shown below.

| Register Name | Address | Register Contents |
|---|---|---|
| RAIL1H | 0x00 | RAIL1 Voltage, bits 9:8 |
| RAIL1L | 0x01 | RAIL1 Voltage, bits 7:0 |
| RAIL2H | 0x02 | RAIL2 Voltage, bits 9:8 |
| RAIL2L | 0x03 | RAIL2 Voltage, bits 7:0 |
| RAIL3H | 0x04 | RAIL3 Voltage, bits 9:8 |
| RAIL3L | 0x05 | RAIL3 Voltage, bits 7:0 |
| RAIL4H | 0x06 | RAIL4 Voltage, bits 9:8 |
| RAIL4L | 0x07 | RAIL4 Voltage, bits 7:0 |
| RAIL5H | 0x08 | RAIL5 Voltage, bits 9:8 |
| RAIL5L | 0x09 | RAIL5 Voltage, bits 7:0 |
| RAIL6H | 0x0A | RAIL6 Voltage, bits 9:8 |
| RAIL6L | 0x0B | RAIL6 Voltage, bits 7:0 |
| RAIL7H | 0x0C | RAIL7 Voltage, bits 9:8 |
| RAIL7L | 0x0D | RAIL7 Voltage, bits 7:0 |
| RAIL8H | 0x0E | RAIL8 Voltage, bits 9:8 |
| RAIL8L | 0x0F | RAIL8 Voltage, bits 7:0 |

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A rail voltage is read with a 16b access. The auto-increment feature of the UCD9080 allows multiple rail voltages to be read with a single access.

A rail voltage is provided as a 10-bit binary value in an un-signed format, as shown below.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | RAILVn | | | | | | | | | |
| r0 | r0 | r0 | r0 | r0 | r0 | r | r | r | r | r | r | r | r | r | r |
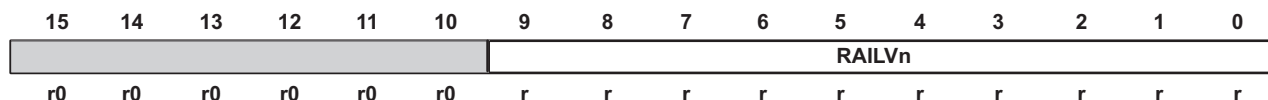
The following formulas can be used to calculate the actual measured rail voltage:

Without external voltage divider:

$$V_{RAILn} = \frac{RAILVn}{1024} \times V_{REF}$$

(1)

With external voltage divider:

$$V_{RAILn} = \frac{RAILVn}{1024} \times V_{REF} \times \frac{R_{PULLDOWN} + R_{PULLUP}}{R_{PULLDOWN}}$$

(2)

## ERROR

Error conditions are logged by the UCD9080 and are accessible to the user via reading the ERROR registers. This is a 6-byte register and it has the following format:

| 0x20 | | | | | | | | 0x21 | | | | | | | |
|------|---|---|---|---|---|---|---|------|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Error Code | | | RAIL | | | Data (dependent on error code) | | | | | | | | | |
| r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r |
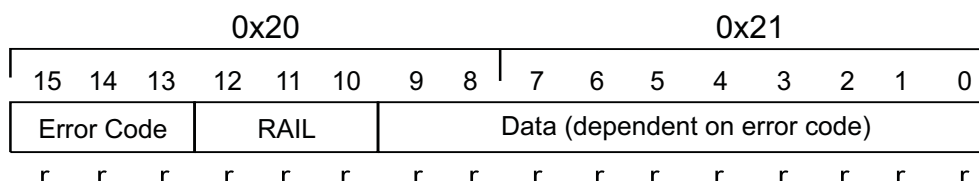
**RAIL**: Rail #(n) - 1, RAIL = 0 through 7

| Error Code | | | Meaning | Data |
|---|---|---|---|---|
| 0 | 0 | 0 | Null Alarm | 0x0000 |
| 0 | 0 | 1 | Supply did not start | Average voltage on Rail |
| 0 | 1 | 0 | Sustained overvoltage detected | Average voltage on Rail |
| 0 | 1 | 1 | Sustained undervoltage detected | Average voltage on Rail |
| 1 | 0 | 0 | Overvoltage glitch detected | Glitch voltage level on Rail |
| 1 | 0 | 1 | Undervoltage glitch detected | Glitch voltage level on Rail |
| 1 | 1 | 0 | Reserved | Reserved |
| 1 | 1 | 1 | Reserved | Reserved |

| 0x22 | | | | | | | | 0x23 | | | | | | | |
|------|---|---|---|---|---|---|---|------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Hour | | | | | | | | Minutes | | | | | | | |
| r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r |

| 0x24 | | | | | | | | 0x25 | | | | | | | |
|------|---|---|---|---|---|---|---|------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Seconds | | | | | | | | Milliseconds | | | | | | | |
| r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r |

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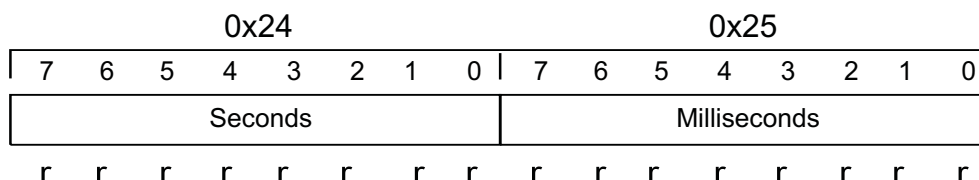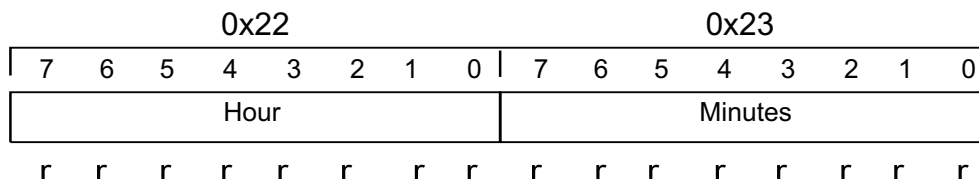
Error conditions encountered during processing will post error logs to this register. There are some exceptions. This register is internally managed as a FIFO where errors are posted to the FIFO as they occur and read out of the FIFO via I²C accesses. The FIFO is only posted to by the UCD9080 if it has room to write, due to the unknown latency of the system reading out of this FIFO. Note that there is no real-time impact to the processing of the UCD9080 if this FIFO is full and cannot be posted to.

The device time is reset by the following conditions:

1. Device Reset
2. A restart command issued to the device by the host via I2C.
3. A Resequence action is taken.

## STATUS

The STATUS is an 8-bit read-only register. This register provides real-time status information about the state of the UCD9080. The following bits are defined.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IIC Error | RAIL error | NVERRLOG | | | | Register Status | |
| rc-0 | rc-0 | r | r-0 | r-0 | r-0 | rc-0 | |

| IIC Error | Meaning |
|---|---|
| 0 | No I2C PHY layer error |
| 1 | I2C PHY layer error |

| RAIL Error | Meaning |
|---|---|
| 0 | No RAIL error pending |
| 1 | RAIL error pending |

| NVERRLOG | Meaning |
|---|---|
| 0 | ERROR points to run-time logs |
| 1 | ERROR points to non-volatile logs |

| Register Status | Meaning |
|---|---|
| 00 | No Error |
| 01 | Invalid Address |
| 10 | Read Access Error |
| 11 | Write Access Error |

Reading of the STATUS register clears the register except for the NVERRLOG bit, which is maintained until the device is reset. Descriptions of the different errors are below.

The IICERROR bit is set when an I²C access fails. This is most often a case where the user has accessed an invalid address, or performed an illegal number of operations for a given register (for example, reading 3 bytes of a 2-byte register). In the event of an I²C error when the I2CERROR is set, bits 1:0 of the STATUS register further define the nature of the error as shown above.

The RAIL error bit is set to alert the user to an issue with one of the voltage rails. When this bit is set, the user is advised to then query the RAILSTATUS register to further ascertain which RAIL input(s) have an issue. The user may then query the ERROR<n> registers to get further information about the nature of the error condition.

The NVERRLOG bit is set to 1 upon device initialization if the UCD9080 was restarted from a shutdown sequence of a RAIL declared as critical. The purpose of this bit is to allow the user to differentiate between stored error logs and real time error logs, and is useful for a post-mortem debug. Note that this bit is the only bit that is not automatically cleared by a read of the STATUS register; this bit is only cleared at device reset if the non-volatile error logs are empty.

When the IICERROR bit is set, the Register Status bits provide further information about the type of I²C error that has been detected, as indicated above.

## RAILSTATUS

The RAILSTATUS1 and RAILSTATUS2 registers are two 8-bit read-only registers that provide a bit-mask that represent the error status of the rails as indicated in the diagram below.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | RAIL8 | RAIL7 | RAIL6 | RAIL5 | RAIL4 | RAIL3 | RAIL2 | RAIL1 |
| rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 | rc-0 |

**RAILn Meaning**
**0 => No Alarm Pending for RAILn**
**1 => Alarm Pending for RAILn**

Bits 15:8 are RAILSTATUS1 and bits 7:0 are RAILSTATUS2. These are read as two 8-bit registers or as a single 16-bit register.

If a bit is set in these registers, then the ERROR register is read to further ascertain the specific error. Bits in the RAILSTATUS1 and RAILSTATUS2 registers are cleared when read.

## FLASHLOCK

The FLASHLOCK I²C command is used to lock and unlock the configuration memory on the UCD9080 when updating the configuration. The section below (Configuring the UCD9080) details this process.

The format for the FLASHLOCK command is as follows:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | FLASHLOCK | | | | |
| rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 | rw-0 |

**FLASHLOCK**
0x00    FLASH is locked (default)
0x01    FLASH is being updated
0x02    Unlock flash (before configuration)
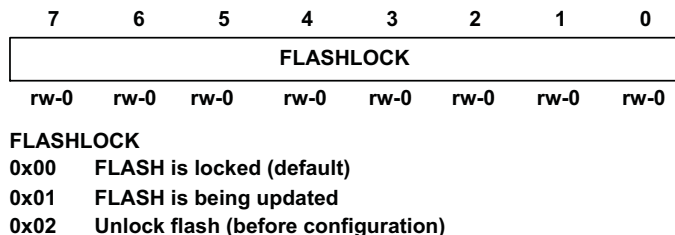
## RESTART

The RESTART register provides the capability for the I²C host to force a re-initialization and restart of the UCD9080. This is an 8-bit register and when written to with a 0, the UCD9080 is restarted and the rails are resequenced. This is useful for restarting the sequencer after the configuration for the system is changed. In order to properly restart the system, this register must be written to a 0.

Note that in order to respond to this I²C request properly, there is a 50-µs delay before the system is restarted, so that the I²C ACK can take place.

## WADDR and WDATA

In order to update the configuration on the UCD9080, two primitive commands are provided in the I²C memory map, WADDR and WDATA (see NOTE). Each of these registers are 8-bits and there are two of each (e.g., WADDR1, WADDR2 and WDATA1, WDATA2) to be able to write addresses and data of up to 16b.

**NOTE:**

In addition to updating the WADDR and WDATA commands, users can use the FLASHLOCK command to perform configuration updates to the UCD9080.

The format for the WADDR command is as follows:

| 15 | 8 | 7 | 0 |
|---|---|---|---|
| | Address | | |
| rw-0x00 | | rw-0x00 | |
| WADDR2 (0x31) | | WADDR1 (0x30) | |
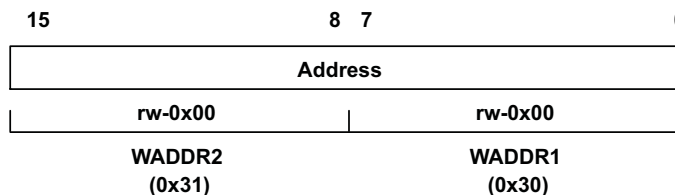
To set the address in the UCD9080 to write, write the LSB of the address to the WADDR1 register and the MSB of the address to the WADDR2 register. For example, to write the address 0x1234 to the device, set WADDR1 = 0x34 and WADDR2 = 0x12. Note that since these addresses support the auto-increment feature, the user can perform a single 16b write to WADDR1 to write the entire address.

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The format for the WDATA command is as follows:

| 15 | | 8 | 7 | | 0 |
|---|---|---|---|---|---|
| | | **Data** | | | |
| | **w** | | | **w** | |
| | **WDATA2**<br>**(0x33)** | | | **WDATA1**<br>**(0x32)** | |
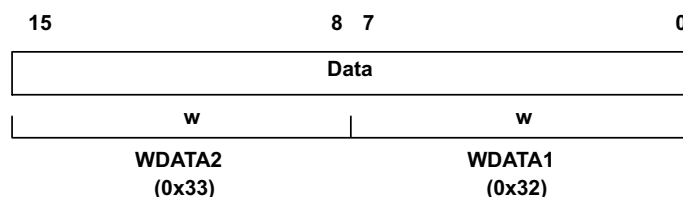
To set the data in the UCD9080 to write, write the LSB of the data to the WDATA1 register and the MSB of the data to the WDATA2 register. For example, to write the data 0xBEEF to the device, set WDATA1 = 0xEF and WDATA2 = 0xBE. Note that since these addresses support the auto-increment feature, the user can perform a single 16b write to WDATA1 to write the entire data.

These two commands are used for updating the UCD9080 configuration, explained in the next section (Configuring the UCD9080).

## RESETTING THE FLASH ERROR LOGS

The UCD9080 can be configured to log critical errors on a voltage rail to flash. This can be configured via the *SaveRailLog* register, described later in this document. If the *SaveRailLog* bit is set for a voltage rail and an error is detected on that voltage rail, then the error logs for that rail are written to flash memory instead of operating memory. This mechanism permits the error logs to be read after the device has been reset and operating memory cleared.

Once the system is in the state where the error logs are pointing to flash, the NVERRLOG bit in the STATUS register is set to a 1 when it is read from the I²C interface. To clear this condition, take the following steps:

- Write FLASHLOCK register to a value of 0x02
- Write WADDR register to a value of 0x1000
- Write WDATA register to a value of 0xBADC
- Write WADDR register to a value of 0x107E
- Write WDATA register to a value of 0xBADC
- Write FLASHLOCK register to a value of 0x00
- Write RESTART register to a value of 0x00

This points the error logs back to operating memory, and restarts the sequencer.

## CONFIGURING THE UCD9080

The UCD9080 has many different configurable parameters such as sequencing policies, shutdown policies and dependency masks. The UCD9080 can configure all of its parameters via the I²C interface while the device is operational; however sequencing, shutdown and rail monitoring is not performed during this time.

The configuration information can not be read from the device.

**NOTE:**

During runtime, if the UCD9080 is configured, there is a delay in voltage monitoring while the new configuration parameters are applied to the device.

To configure the UCD9080, a large block of configuration information is sent to the device via the I²C interface. This block is 512 bytes and contains all the configuration information that the device requires for any function of the UCD9080.

This 512 byte block of configuration information is sent to the device in multiple segments. The segment size can range from 2 to 32 bytes at one time, and must be a multiple of 2 bytes. That is, a master can send 256 2-byte segments or 32 16-byte segments, and so on. All the segments must be sent back-to-back in the proper sequence and this operation must be completed by sending the last segment so that the last byte of the 512 byte block is written. If this is not done, the UCD9080 is in an unknown state and does not function as designed.

## CONFIGURING THE UCD9080 (continued)

The process for sending the configuration information to the UCD9080 is as shown in Figure 11:
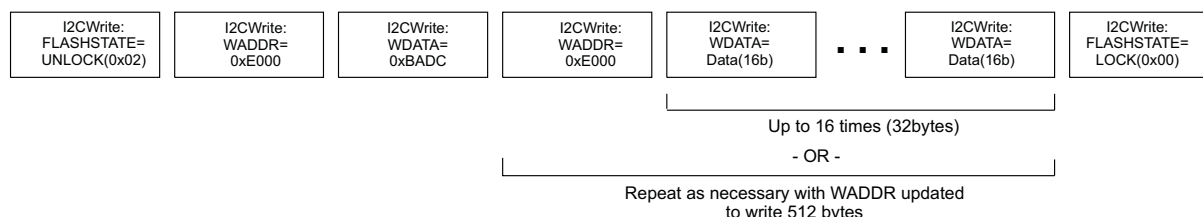


**Figure 11. Configuration Information**

As shown in Figure 11, the process for updating the configuration of the UCD9080 is as follows:

1. Unlock flash memory by sending the UNLOCK command (FLASHSTATE = 0x02)
2. Write the address of the configuration section of memory (WADDR = 0xE000)
3. Write the constant 0xBADC to update memory (WDATA = 0xBADC)
4. Write the address of the configuration section of memory again (WADDR = 0xE000)
5. Write the data (WDATA = <varies>). Repeat steps 4 and 5 as necessary, depending on the data segment size used to write 512 bytes. Increment the address as necessary.
6. Lock flash memory after the last byte of the last segment is written (FLASHSTATE = 0x00)

At the conclusion of this process, the configuration of the UCD9080 is updated with the configuration changes, as represented by the values from the data segments. The sequencer can then be reset using the RESTART $I^2C$ command, and then the application restarts.

The memory map for the 512 byte configuration segment is defined in the section below.

### Configuration Parameters Memory Map

Table 1 shows the 512 byte configuration parameters memory map. Each of the fields at each of the addresses in this memory map either represents a configuration parameter for the UCD9080 that is changed by changing its value, or it must be hard-coded to the given literal value.

**Table 1. Configuration Parameters Memory Map**

| ADDRESS | +0 | +1 | +2 | +3 | +4 | +5 | +6 | +7 |
|---|---|---|---|---|---|---|---|---|
| 0xE000 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE008 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE010 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE018 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE020 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE028 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE030 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE038 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE040 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE048 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE050 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE058 | 0xFF | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0xC0 | 0x02 |
| 0xE060 | 0x00 | 0x00 | 0x00 | 0xF0 | 0x01 | 0x02 | 0x00 | 0x02 |
| 0xE068 | 0x7F | 0x0E | 0x00 | 0x50 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE070 | 0x00 | 0x00 | 0xC0 | 0x20 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE078 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0xA8 | 0xDC | 0xBA |
| 0xE080 | SequenceEventParameters | | | | | | | |
| 0xE088 | SequenceEventParameters (continued) | | | | SequenceEventLink | | | |

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# CONFIGURING THE UCD9080 (continued)

## Table 1. Configuration Parameters Memory Map (continued)

| ADDRESS | +0 | +1 | +2 | +3 | +4 | +5 | +6 | +7 |
|---------|----|----|----|----|----|----|----|----|
| 0xE090 | SequenceEventLink (continued) | | | | | | | |
| 0xE098 | SequenceEventData | | | | | | | |
| 0xE0A0 | | | | | | | | |
| 0xE0A8 | | | | | | | | |
| 0xE0B0 | 0xFF | 0x7F | 0xFF | 0x7F | 0xFF | 0x7F | 0xFF | 0x7F |
| 0xE0B8 | 0xFF | 0x7F | 0xFF | 0x7F | 0xFF | 0x7F | 0xFF | 0x7F |
| 0xE0C0 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE0C8 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE0D0 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE0D8 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE0E0 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE0E8 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE0F0 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE0F8 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE100 | DependencyMasks | | | | | | | |
| 0xE108 | | | | | | | | |
| 0xE110 | UnderVoltageThreholds | | | | | | | |
| 0xE118 | | | | | | | | |
| 0xE120 | OverVoltageThresholds | | | | | | | |
| 0xE128 | | | | | | | | |
| 0xE130 | RampTime | | | | | | | |
| 0xE138 | | | | | | | | |
| 0xE140 | OutOfRegulationWidth | | | | | | | |
| 0xE148 | | | | | | | | |
| 0xE150 | UnsequenceTime | | | | | | | |
| 0xE158 | | | | | | | | |
| 0xE160 | | | | | | | | |
| 0xE168 | EnablePolarity | | | | | | | |
| 0xE170 | | | | | | | | |
| 0xE178 | | | | | | | | |
| 0xE180 | SaveRailLog | | 0xF9 | 0x00 | 0x94 | 0x02 | ReferenceSelect | |
| 0xE188 | 0x10 | 0x07 | 0x05 | 0xC0 | 0x32 | 0x00 | LastUnusedSeq | |
| 0xE190 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE198 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE1A0 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE1A8 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE1B0 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE1B8 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE1C0 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE1C8 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE1D0 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE1D8 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE1E0 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE1E8 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE1F0 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0xE1F8 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |

PRODUCT PREVIEW

## CONFIGURATION PARAMETERS DETAIL

The following section details the format and meaning of the configuration parameters from the configuration parameters memory map (Table 1).

### SequenceEventParameters

The SequenceEventParameters field in the configuration parameters specifies the rail identification, monitoring status and sequencing options for each rail. The address map for all these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION |
|---------|------|---------------|-------------|
| 0xE080 | 1 | 0x50 | Rail 1 identification, monitoring status and sequencing options. |
| 0xE081 | 1 | 0x51 | Rail 2 identification, monitoring status and sequencing options. |
| 0xE082 | 1 | 0x52 | Rail 3 identification, monitoring status and sequencing options. |
| 0xE083 | 1 | 0x53 | Rail 4 identification, monitoring status and sequencing options. |
| 0xE084 | 1 | 0x54 | Rail 5 identification, monitoring status and sequencing options. |
| 0xEx85 | 1 | 0x55 | Rail 6 identification, monitoring status and sequencing options. |
| 0xE086 | 1 | 0x56 | Rail 7 identification, monitoring status and sequencing options. |
| 0xE087 | 1 | 0x07 | Rail 8 identification, monitoring status and sequencing options. |
| 0xE088 | 1 | 0x08 | GPO1 identification, sequencing options. |
| 0xE089 | 1 | 0x49 | GPO2 identification, sequencing options. |
| 0xE08A | 1 | 0x4A | GPO3 identification, sequencing options. |
| 0xE08B | 1 | 0x4B | GPO4 identification, sequencing options. |

The format of each register is as follows:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ENABLE | | 0 | MON | RAIL/GPO | | | |

**RAIL**

Rail #(n) - 1, RAIL = 0 through 7

**GPO**

GPO # (n) + 7, GPO = 8, 9, 0xA, 0xB

| MON | Meaning |
|-----|---------|
| 0 | Do not monitor rail status (for event sequencing of GPOs) |
| 1 | Monitor rail status |

| ENABLE | Meaning |
|--------|---------|
| 00 | Sequence is disabled |
| 01 | Sequence is triggered after delay after sequence event |
| 10 | Sequence is triggered after parent rails achieves voltage level |
| 11 | Sequence is triggered after delay after parent rail achieves voltage regulation |

**PRODUCT PREVIEW**

### SequenceEventLink

The SequenceEventLink field in the configuration parameters specifies each rail's parent rail as well as whether or not to sequence it after shutdown. The address map for all these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION |
|---------|------|---------------|-------------|
| 0xE08C | 1 | 0x01 | Rail 1 parent identifier and resequence indicator. |
| 0xE08D | 1 | 0x00 | Rail 2 parent identifier and resequence indicator. |
| 0xE08E | 1 | 0x01 | Rail 3 parent identifier and resequence indicator. |
| 0xE08F | 1 | 0x04 | Rail 4 parent identifier and resequence indicator. |
| 0xE090 | 1 | 0x01 | Rail 5 parent identifier and resequence indicator. |
| 0xE091 | 1 | 0x04 | Rail 6 parent identifier and resequence indicator. |
| 0xE092 | 1 | 0x05 | Rail 7 parent identifier and resequence indicator. |
| 0xE093 | 1 | 0x06 | Rail 8 parent identifier and resequence indicator. |
| 0xE094 | 1 | 0x00 | GPO1 parent rail identifier and resequence indicator. |
| 0xE095 | 1 | 0x00 | GPO2 parent rail identifier and resequence indicator. |
| 0xE096 | 1 | 0x00 | GPO3 parent rail identifier and resequence indicator. |
| 0xE097 | 1 | 0x00 | GPO4 parent rail identifier and resequence indicator. |

The format of each register is as follows:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | RESEQ | 0 | 0 | PARENTRAIL | | | |

| RESEQ | Meaning |
|-------|---------|
| 0 | Do not resequence after shutdown |
| 1 | Resequence after shutdown |

| PARENTRAIL | Meaning |
|------------|---------|
| 0x0000 | Sequence is dependent on RAIL1 achieving the specified event |
| 0x0001 | Sequence is dependent on RAIL2 achieving the specified event |
| 0x0010 | Sequence is dependent on RAIL3 achieving the specified event |
| 0x0011 | Sequence is dependent on RAIL4 achieving the specified event |
| 0x0100 | Sequence is dependent on RAIL5 achieving the specified event |
| 0x0101 | Sequence is dependent on RAIL6 achieving the specified event |
| 0x0110 | Sequence is dependent on RAIL7 achieving the specified event |
| 0x0111 | Sequence is dependent on RAIL8 achieving the specified event |

**PRODUCT PREVIEW**

**SequenceEventData**

The SequenceEventData field in the configuration parameters specifies each rail's sequencing parameters. The address map for all these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION |
|---|---|---|---|
| 0xE098 | 2 | 0xE005 | Rail 1 sequencing and shutdown parameters. |
| 0xE09A | 2 | 0xA005 | Rail 2 sequencing and shutdown parameters. |
| 0xE09C | 2 | 0xE032 | Rail 3 sequencing and shutdown parameters. |
| 0xE09E | 2 | 0xE033 | Rail 4 sequencing and shutdown parameters. |
| 0xE0A0 | 2 | 0xE033 | Rail 5 sequencing and shutdown parameters. |
| 0xE0A2 | 2 | 0xE035 | Rail 6 sequencing and shutdown parameters. |
| 0xE0A4 | 2 | 0xE035 | Rail 7 sequencing and shutdown parameters. |
| 0xE0A6 | 2 | 0x0000 | Rail 8 sequencing and shutdown parameters. |
| 0xE0A8 | 2 | 0x0000 | GPO1 sequencing and shutdown parameters. |
| 0xE0AA | 2 | 0x0000 | GPO2 sequencing and shutdown parameters. |
| 0xE0AC | 2 | 0x0000 | GPO3 sequencing and shutdown parameters. |
| 0xE0AE | 2 | 0x0000 | GPO4 sequencing and shutdown parameters. |

The format for each register is as follows:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SEQPARAM | | | RAILDATA | | | | | | | | | | | | |

| SEQPARAM | Meaning |
|---|---|
| 000 | Ignore |
| 001 | Resequence after shutdown |
| 010 | Retry 4 times |
| 011 | Retry 3 times |
| 100 | Retry 2 times |
| 101 | Retry 1 time |
| 110 | Shutdown |
| 111 | Retry forever |

**RAILDATA Meaning**
ENABLE in SequenceEventParameters register

| 01 | Delay (ms) |
|---|---|
| 10 | Volatge (V) |
| 11 | Delay (mS) |

PRODUCT PREVIEW

**PRODUCT PREVIEW**

### DependencyMasks

The DependencyMasks field in the configuration parameters specifies each rail's dependency masks which are used for rail shutdown. This mask represents the set of other rails and GPOs that should be shutdown when this rail shuts down. Note that since only rails are monitored, this table only has entries for rails that are shutdown. In the dependency mask itself, there are bits that allow for the shutting down of a GPO.

The address map for all these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION |
|---------|------|---------------|-------------|
| 0xE100 | 2 | 0x007F | Dependency mask for rail 1. |
| 0xE102 | 2 | 0x0001 | Dependency mask for rail 2. |
| 0xE104 | 2 | 0x0002 | Dependency mask for rail 3. |
| 0xE106 | 2 | 0x0004 | Dependency mask for rail 4. |
| 0xE108 | 2 | 0x0008 | Dependency mask for rail 5. |
| 0xE10A | 2 | 0x0010 | Dependency mask for rail 6. |
| 0xE10C | 2 | 0x0020 | Dependency mask for rail 7. |
| 0xE10E | 2 | 0x0040 | Dependency mask for rail 8. |

The format for each register is as follows:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|------|------|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | 0 | GPO4 | GPO3 | GPO2 | GPO1 | RAIL8 | RAIL7 | RAIL6 | RAIL5 | RAIL4 | RAIL3 | RAIL2 | RAIL1 |

| RAILn or GPOn | Meaning |
|---------------|---------|
| 0 | Shutdown of this rail will not shutdown RAILn or GPOn |
| 1 | Shutdown of this rail will shutdown RAILn or GPOn |

### UnderVoltageThresholds

The UnderVoltageThresholds field in the configuration parameters specifies each rail's undervoltage thresholds that are used when monitoring this rail. The address map for all these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION |
|---------|------|---------------|-------------|
| 0xE110 | 2 | 0x0000 | Undervoltage threshold for rail 8. |
| 0xE112 | 2 | 0x0000 | Undervoltage threshold for rail 7. |
| 0xE114 | 2 | 0x0000 | Undervoltage threshold for rail 6. |
| 0xE116 | 2 | 0x0000 | Undervoltage threshold for rail 5. |
| 0xE118 | 2 | 0x0000 | Undervoltage threshold for rail 4. |
| 0xE11A | 2 | 0x0000 | Undervoltage threshold for rail 3. |
| 0xE11C | 2 | 0x0000 | Undervoltage threshold for rail 2. |
| 0xE11E | 2 | 0x0000 | Undervoltage threshold for rail 1. |

The format for each register is as follows:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Vraw | | | | | | | | | | |

The voltage conversion is dependent upon the configured voltage reference and the pull-up and pull-down resistors used on the board for each rail. The voltage reference is selected as either 2.5 V (internal) or 3.3 V (external via $V_{CC}$). The formula to convert the desired Rail's UnderVoltageThreshold to Vraw follows:

Without external rail voltage divider:

$$Vraw = \frac{1024 \times V_{RAILUV}}{V_{REF}}$$

(3)

With external rail voltage divider:

$$Vraw = \frac{1024 \times V_{RAILUV}}{V_{REF}} \times \frac{R_{PULLDOWN}}{R_{PULLDOWN} + R_{PULLUP}}$$

(4)

**OverVoltageThresholds**

The OverVoltageThreholds field in the configuration parameters specifies each rail's over voltage thresholds that are used when monitoring this rail. The address map for all these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION |
|---------|------|---------------|-------------|
| 0xE120 | 2 | 0x0400 | Overvoltage threshold for rail 8. |
| 0xE122 | 2 | 0x0400 | Overvoltage threshold for rail 7. |
| 0xE124 | 2 | 0x0400 | Overvoltage threshold for rail 6. |
| 0xE126 | 2 | 0x0400 | Overvoltage threshold for rail 5. |
| 0xE128 | 2 | 0x0400 | Overvoltage threshold for rail 4. |
| 0xE12A | 2 | 0x0400 | Overvoltage threshold for rail 3. |
| 0xE12C | 2 | 0x0400 | Overvoltage threshold for rail 2. |
| 0xE12E | 2 | 0x0400 | Overvoltage threshold for rail 1. |

The format for each register is as follows:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Vraw | | | | | | | | | | |

The voltage conversion is dependent upon the configured voltage reference and the pull-up and pull-down resistors used on the board for each rail. The voltage reference is selected as either 2.5 V (internal) or 3.3 V (external via $V_{CC}$). The formula to convert the desired Rail's OverVoltageThreshold to Vraw follows:

Without external rail voltage divider:

$$Vraw = \frac{1024 \times V_{RAILOV}}{V_{REF}}$$

(5)

With external voltage divider:

$$Vraw = \frac{1024 \times V_{RAILOV}}{V_{REF}} \times \frac{R_{PULLDOWN}}{R_{PULLDOWN} + R_{PULLUP}}$$

(6)

**RampTime**

The RampTime field in the configuration parameters specifies the maximum amount of time for each rail to achieve regulation. The address map for all these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION |
|---------|------|---------------|-------------|
| 0xE130 | 2 | 0x0FA0 | Maximum voltage ramp time for rail 1. |
| 0xE132 | 2 | 0x0FA0 | Maximum voltage ramp time for rail 2. |
| 0xE134 | 2 | 0x0FA0 | Maximum voltage ramp time for rail 3. |
| 0xE136 | 2 | 0x0FA0 | Maximum voltage ramp time for rail 4. |
| 0xE138 | 2 | 0x0FA0 | Maximum voltage ramp time for rail 5. |
| 0xE13A | 2 | 0x0FA0 | Maximum voltage ramp time for rail 6. |
| 0xE13C | 2 | 0x0FA0 | Maximum voltage ramp time for rail 7. |
| 0xE13E | 2 | 0x0FA0 | Maximum voltage ramp time for rail 8. |

The 16b value of this register is the number of milliseconds that this rail has to achieve regulation without an error.

**PRODUCT PREVIEW**

### OutOfRegulation Width

The OutOfRegulationWidth field in the configuration parameters specifies the maximum amount of time that the rail is allowed to be out of regulation before an error is declared (glitch width). The address map for all these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION |
|---------|------|---------------|-------------|
| 0xE140 | 2 | 0x0010 | The out of regulation width permissible without flagging error for Rail 1. |
| 0xE142 | 2 | 0x0010 | The out of regulation width permissible without flagging error for Rail 2. |
| 0xE144 | 2 | 0x0010 | The out of regulation width permissible without flagging error for Rail 3. |
| 0xE146 | 2 | 0x0010 | The out of regulation width permissible without flagging error for Rail 4. |
| 0xE148 | 2 | 0x0010 | The out of regulation width permissible without flagging error for Rail 5. |
| 0xE14A | 2 | 0x0010 | The out of regulation width permissible without flagging error for Rail 6. |
| 0xE14C | 2 | 0x0010 | The out of regulation width permissible without flagging error for Rail 7. |
| 0xE14E | 2 | 0x0010 | The out of regulation width permissible without flagging error for Rail 8. |

The contents of this register are as follows:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | OORW | | | | | | | | |

OORW= RAILn Out of regulation glitch width (in units of 1/10 mS)

### UnsequenceTime

The UnsequenceTime field in the configuration parameters specifies the amount of time that each rail should delay before unsequencing. The address map for all these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION |
|---------|------|---------------|-------------|
| 0xE150 | 2 | 0xC0FF | Unsequence delay for Rail 1. |
| 0xE152 | 2 | 0xC1FF | Unsequence delay for Rail 2. |
| 0xE154 | 2 | 0xC2FF | Unsequence delay for Rail 3. |
| 0xE156 | 2 | 0xC3FF | Unsequence delay for Rail 4. |
| 0xE158 | 2 | 0xC4FF | Unsequence delay for Rail 5. |
| 0xE15A | 2 | 0xC5FF | Unsequence delay for Rail 6. |
| 0xE15C | 2 | 0xC6FF | Unsequence delay for Rail 7. |
| 0xE15E | 2 | 0xC7FF | Unsequence delay for Rail 8. |
| 0xE160 | 2 | 0xC000 | Unsequence delay for GPO1. |
| 0xE162 | 2 | 0xC000 | Unsequence delay for GPO2. |
| 0xE164 | 2 | 0xC000 | Unsequence delay for GPO3. |
| 0xE166 | 2 | 0xC000 | Unsequence delay for GPO4. |

The contents of this register are as follows:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | | | | | | USTIME | | | | | | | |

USTIME = RAILn UnsequenceTime (in units of mS).

**PRODUCT PREVIEW**

**EnablePolarity**

The EnablePolarity field in the configuration parameters specifies whether each power supply enable or GPO is to be configured active high or active low.. The address map for all these registers is as follows:

| ADDRESS | SIZE | DEFAULT VALUE | DESCRIPTION |
|---------|------|---------------|-------------|
| 0xE168 | 2 | 0x2004 | Polarity for Rail 1 enable. |
| 0xE16A | 2 | 0x2008 | Polarity for Rail 2 enable. |
| 0xE16C | 2 | 0x1804 | Polarity for Rail 3 enable. |
| 0xE16E | 2 | 0x1802 | Polarity for Rail 4 enable. |
| 0xE170 | 2 | 0x1808 | Polarity for Rail 5 enable. |
| 0xE172 | 2 | 0x1810 | Polarity for Rail 6 enable. |
| 0xE174 | 2 | 0x1820 | Polarity for Rail 7 enable. |
| 0xE176 | 2 | 0x2010 | Polarity for Rail 8 enable. |
| 0xE178 | 2 | 0x1800 | Polarity for GPO1. |
| 0xE17A | 2 | 0x2020 | Polarity for GPO2. |
| 0xE17C | 2 | 0x2040 | Polarity for GPO3. |
| 0xE17E | 2 | 0x2080 | Polarity for GPO4. |

The contents of this register are as follows:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| POL | DEFAULT VALUES as specified above | | | | | | | | | | | | | | |

| POL | Meaning |
|-----|---------|
| 0 | Railn enable or GPOn is active low |
| 1 | Railn enable or GPOn is active high |

**SaveRailLog**

The SaveRailLog field in the configuration parameters specifies whether each rail is marked to write the error log to flash upon rail failure. If the rail is marked this way, then a shutdown of this rail is logged info non-volatile memory.

The contents of this register are as follows:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RAIL8 | RAIL7 | RAIL6 | RAIL5 | RAIL4 | RAIL3 | RAIL2 | RAIL1 |

| RAILn | Meaning |
|-------|---------|
| 0 | Shutdown of this rail will not log this event. |
| 1 | Shutdown of this rail will log this event. |

The default value for this register is 0x0000.

**PRODUCT PREVIEW**

**ReferenceSelect**

The ReferenceSelect field in the configuration parameters specifies which voltage reference is used on the UCD9080. The selected reference can be internal (2.5-V), or external via $V_{CC}$ (3.3 V). The contents of this register are as follows:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| SELREF | | | 0x8F2 | | | | | | | | | | | | |

| SELREF | Meaning |
|--------|---------|
| 000 | External Reference Selected (VCC). |
| 001 | Internal Reference Selected (2.5 V). |

The default value for this register is 0x8F2, which selects the external reference.

**LastUnusedSeq**

The LastUnusedSeq field in the configuration parameters specifies the amount of time for the last rail to be shutdown without creating an error.

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| LUTIME | | | | | | | | | | | | | | | |

LUTIME  = Maximum value USTIME + 255 (in units of mS)

The default value for this register is 0x08FF.

**PRODUCT PREVIEW**

**APPLICATION INFORMATION**

## Typical Application Diagram

Figure 12 illustrates a typical power supply sequencing configuration. Power Supply 1 and Power Supply X require active low enables while Power Supply 2 and Power Supply 3 require active high enables. $V_{OUT1}$ and $V_{OUT3}$ exceed the selected A/D reference voltage so their outputs are divided before being sampled by the MON1 and MON3 inputs. $V_{OUT2}$ and $V_{OUTX}$ are within the selected A/D reference voltage so their outputs can be sampled directly by the MON2 and MON7 inputs. Figure 12 illustrates the use of the GPO digital output pins to provide status and power on reset to other system devices.
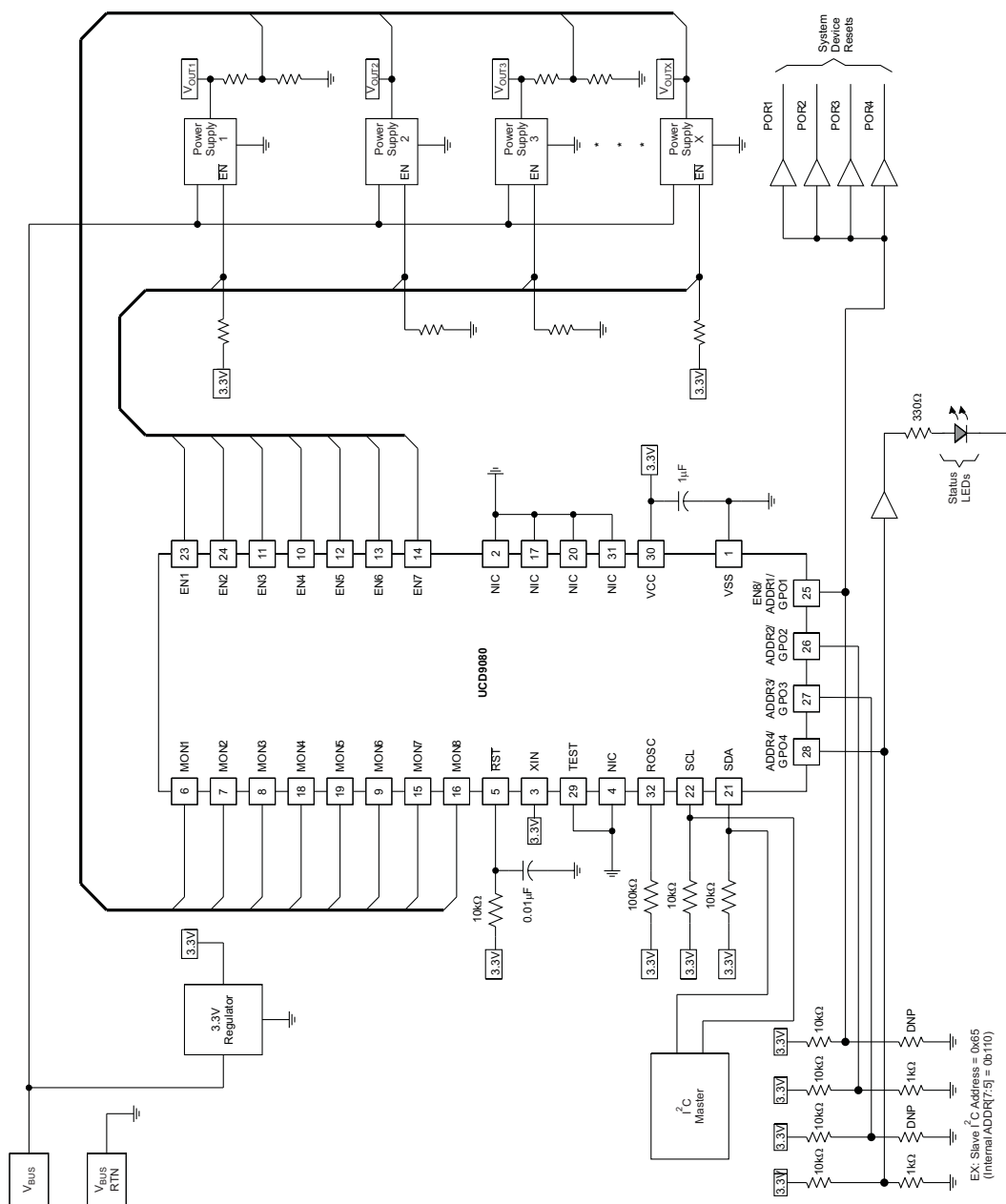


**Figure 12. Typical Power Supply Sequencing Application**

**PRODUCT PREVIEW**

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| UCD9080RHBR | PREVIEW | QFN | RHB | 32 | 3000 | TBD | Call TI | Call TI |
| UCD9080RHBT | PREVIEW | QFN | RHB | 32 | 250 | TBD | Call TI | Call TI |

**[1]** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**[2]** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
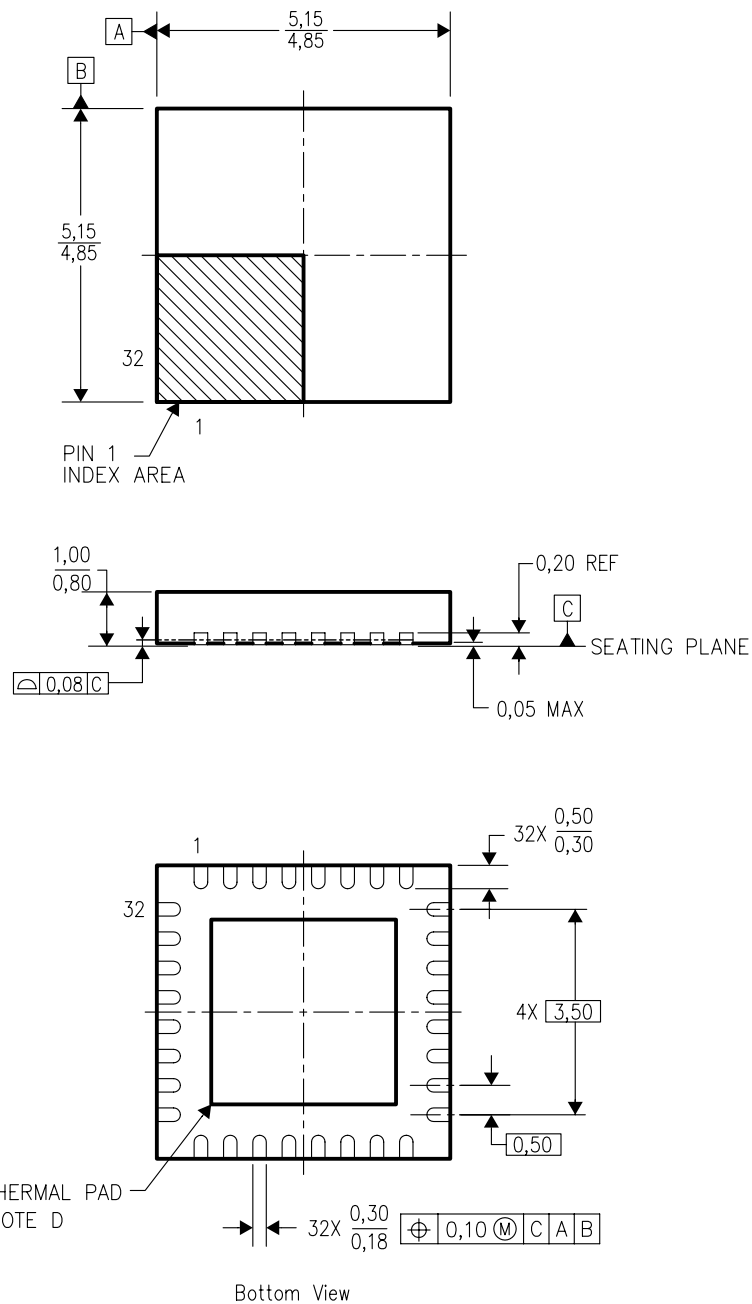
**[3]** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## RHB (S−PQFP−N32)                    PLASTIC QUAD FLATPACK



$\frac{5,15}{4,85}$

A

B

$\frac{5,15}{4,85}$

32

1

PIN 1
INDEX AREA

$\frac{1,00}{0,80}$

0,20 REF

C

SEATING PLANE

0,08 C

0,05 MAX

1

32

$32X \frac{0,50}{0,30}$

$4X \boxed{3,50}$

$\boxed{0,50}$

EXPOSED THERMAL PAD
SEE NOTE D

$32X \frac{0,30}{0,18}$   $\boxed{\oplus\ 0,10\ \text{M}\ C\ A\ B}$

Bottom View

4204326/C  xx/04

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No−Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance.
See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO−220.

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