



MicroConverter[®], Small Package 12-Bit ADC with Embedded FLASH MCU

ADuC814

FEATURES

Analog I/O

- 6-Channel 247 kSPS ADC
- 12-Bit Resolution
- ADC High Speed Data Capture Mode
- Programmable Reference via On-Chip DAC for Low Level Inputs
- ADC Performance Down to V_{REF} of 0.1 V
- Dual-Voltage Output DACs
- 12-Bit Resolution, 15 μ s Settling Time

Memory

- 8 KBytes On-Chip Flash/EE Program Memory
- 640 Bytes On-Chip Flash/EE Data Memory
- Flash/EE, 100-Year Retention, 100 K Cycles Endurance
- Three Levels of Flash/EE Program Memory Security
- In-Circuit Serial Download (No External Hardware Required)
- 256 Bytes On-Chip Data RAM

8051 Based Core

- 8051 Compatible Instruction Set
- 32 kHz External Crystal
- On-Chip Programmable PLL (16.78 MHz Max)
- Three 16-Bit Timer/Counters
- 11 Programmable I/O Lines
- 11 Interrupt Sources, Two Priority Levels

Power

- Specified for 3 V and 5 V Operation
- Normal: 3 mA @ 3 V (Core CLK = 2.1 MHz)
- Power-Down: 15 μ A at 3 V (32 kHz Running)

On-Chip Peripherals

- Power-On Reset Circuit (No Need for External POR Device)
- Temperature Monitor ($\pm 1.5^{\circ}\text{C}$)
- Precision Voltage Reference
- Time Interval Counter (Wake-Up/RTC Timer)
- UART Serial I/O
- SPI[®]/I²C[®] Compatible Serial I/O
- Watchdog Timer (WDT) and Power Supply Monitor (PSM)

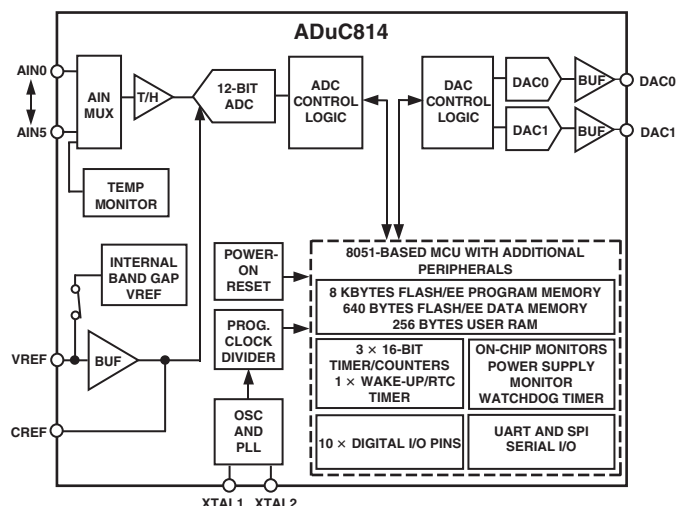
Package and Temperature Range

- 28-Lead TSSOP 4.4 mm $\times$ 9.7 mm Body Package
- Fully Specified for -40°C to $+125^{\circ}\text{C}$ Operation

APPLICATIONS

- Optical Networking—Laser Power Control
- Base Station Systems—Power Amplifier Bias Control
- Precision Instruments and Smart Sensors
- Battery-Powered Systems and General Precision System Monitors

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADuC814 is a fully integrated 247 kSPS 12-bit data acquisition system incorporating a high performance multichannel ADC, an 8-bit MCU, and program/data Flash/EE memory on a single chip.

This low power device operates from a 32 kHz crystal with an on-chip PLL generating a high frequency clock of 16.78 MHz. This clock is in turn routed through a programmable clock divider from which the MCU core clock operating frequency is generated.

The microcontroller core is an 8052 and is therefore 8051-instruction-set compatible. 8 Kbytes of nonvolatile Flash/EE program memory are provided on-chip. 640 bytes of nonvolatile Flash/EE data memory and 256 bytes of RAM are also integrated on-chip.

The ADuC814 also incorporates additional analog functionality with dual 12-bit DACs, a power supply monitor, and a band gap reference.

On-chip factory firmware supports in-circuit serial download and debug modes (via UART), as well as the single-pin emulation mode via the DLOAD pin. The ADuC814 is supported by a QuickStart[™] development system. This is a full featured low cost system, consisting of PC-based (Windows[®] compatible) hardware and software development tools.

The part operates from a single 3 V or 5 V supply over the extended temperature range -40°C to $+125^{\circ}\text{C}$. When operating from 3 V supplies, the power dissipation for the part is below 10 mW. The ADuC814 is housed in a 28-lead TSSOP package.

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SPI is a registered trademark of Motorola Inc.

I²C is a registered trademark of Phillips Corporation.

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Windows is a registered trademark of Microsoft Corporation.

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ADuC814—SPECIFICATIONS¹

($V_{DD} = DV_{DD} = 2.7\text{ V to }3.3\text{ V or }4.5\text{ V to }5.5\text{ V}$. $V_{REF} = 2.5\text{ V}$ Internal Reference.
XTAL1/XTAL2 = 32.768 kHz Crystal. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.)

Parameter	$V_{DD} = 5\text{ V}$	$V_{DD} = 3\text{ V}$	Unit	Test Conditions
ADC CHANNEL SPECIFICATIONS				
A GRADE				
DC ACCURACY ^{2, 3}				$f_{SAMPLE} = 147\text{ kHz}$
Resolution	12	12	Bits	
Integral Nonlinearity	± 2	± 2	LSB max	2.5 V Internal Reference
	± 1	± 1	LSB typ	
Differential Nonlinearity	± 4	± 4	LSB max	2.5 V Internal Reference
	± 2	± 2	LSB typ	
Integral Nonlinearity	± 2.5	± 2.5	LSB typ	1 V External Reference
Differential Nonlinearity	± 5	± 5	LSB typ	1 V External Reference
CALIBRATED ENDPOINT ERRORS ^{4, 5}				
Offset Error	± 5	± 5	LSB max	
Offset Error Match	± 1	± 1	LSB typ	
Gain Error	± 5	± 5	LSB max	
Gain Error Match	± 1	± 1	LSB typ	
DYNAMIC PERFORMANCE				$f_{IN} = 10\text{ kHz}$ Sine Wave $f_{SAMPLE} = 147\text{ kHz}$
Signal-to-Noise Ratio (SNR) ⁶	62.5	62.5	dB typ	
Total Harmonic Distortion (THD)	-65	-65	dB typ	
Peak Harmonic or Spurious Noise	-65	-65	dB typ	
Channel-to-Channel Crosstalk ⁷	-80	-80	dB typ	
B GRADE				
DC ACCURACY ^{2, 3}				$f_{SAMPLE} = 147\text{ kHz}$
Resolution	12	12	Bits	
Integral Nonlinearity	± 1	± 1	LSB max	2.5 V Internal Reference
	± 0.3	± 0.3	LSB typ	
Differential Nonlinearity	± 0.9	± 0.9	LSB max	2.5 V Internal Reference
	± 0.25	± 0.25	LSB typ	
Integral Nonlinearity ¹³	± 1.5	± 1.5	LSB max	1 V External Reference
Differential Nonlinearity ¹³	+1.5/-0.9	+1.5/-0.9	LSB max	1 V External Reference
Code Distribution	1	1	LSB typ	ADC Input Is a DC Voltage
CALIBRATED ENDPOINT ERRORS ^{4, 5}				
Offset Error	± 2	± 3	LSB max	
Offset Error Match	± 1	± 1	LSB typ	
Gain Error	± 2	± 3	LSB max	
Gain Error Match	± 1	± 1	LSB typ	
DYNAMIC PERFORMANCE				$f_{IN} = 10\text{ kHz}$ Sine Wave $f_{SAMPLE} = 147\text{ kHz}$
Signal-to-Noise Ratio (SNR) ⁶	71	71	dB typ	
Total Harmonic Distortion (THD)	-85	-85	dB typ	
Peak Harmonic or Spurious Noise	-85	-85	dB typ	
Channel-to-Channel Crosstalk ⁷	-80	-80	dB typ	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	V	
Leakage Current	± 1	± 1	μA max	
Input Capacitance	32	32	pF typ	
TEMPERATURE MONITOR ⁸				
Voltage Output at 25°C	650	650	mV typ	
Voltage TC	-2	-2	mV/°C typ	
Accuracy	± 3	± 3	°C typ	Internal 2.5 V V_{REF}
Accuracy	± 1.5	± 1.5	°C typ	External 2.5 V V_{REF}

Parameter	V _{DD} = 5 V	V _{DD} = 3 V	Unit	Test Conditions
DAC CHANNEL SPECIFICATIONS				DAC Load to AGND R _L = 10 kΩ, C _L = 100 pF
DC ACCURACY ⁹				
Resolution	12	12	Bits	Guaranteed Monotonic
Relative Accuracy	±3	±3	LSB typ	
Differential Nonlinearity ¹⁰	-1	-1	LSB max	
	±1/2	±1/2	LSB typ	
Offset Error	±50	±50	mV max	V _{REF} Range
Gain Error	±1	±1	% max	V _{REF} Range
	±1	±1	% typ	AV _{DD} Range
Gain Error Mismatch	0.5	0.5	% typ	Of Full Scale on DAC1
ANALOG OUTPUTS				
Voltage Range_0	0 to V _{REF}	0 to V _{REF}	V	DAC V _{REF} = 2.5 V
Voltage Range_1	0 to V _{DD}	0 to V _{DD}	V	DAC V _{REF} = V _{DD}
Output Impedance	0.5	0.5	Ω typ	
I _{SINK}	50	50	μA typ	
DAC AC SPECIFICATIONS				
Voltage Output Settling Time	15	15	μs typ	Full-Scale Settling Time to within 1/2 LSB of Final Value
Digital-to-Analog Glitch Energy	10	10	nVs typ	1 LSB Change at Major Carry
REFERENCE INPUT/OUTPUT				
REFERENCE OUTPUT ¹¹				
Output Voltage (V _{REF})	2.5	2.5	V	Of V _{REF} Measured at the CREF Pin
Accuracy	±2.5	±2.5	% max	
Power Supply Rejection	47	57	dB typ	
Reference Temperature Coefficient	±100	±100	ppm/°C typ	
Internal V _{REF} Power-On Time	80	80	ms typ	
EXTERNAL REFERENCE INPUT ¹²				
Voltage Range (V _{REF}) ¹³	0.1	0.1	V min	Internal Band Gap Deselected via ADCCON2.6
	V _{DD}	V _{DD}	V max	
Input Impedance	20	20	kΩ typ	
Input Leakage	10	10	μA max	
POWER SUPPLY MONITOR (PSM)				
V _{DD} Trip Point Selection Range	2.63	2.63	V	Four Trip Points Selectable in this Range Programmed via TP1-0 in PSMCON
	2.93	2.93	V	
	3.08	3.08	V	
	4.63	4.63	V	
V _{DD} Power Supply Trip Point Accuracy	±3.5	±3.5	% max	
WATCHDOG TIMER (WDT) ¹³				
Time-Out Period	0	0	ms min	Nine Time-Out Periods Selectable in this Range Programmed via PRE3-0 in WDCON
	2000	2000	ms max	
LOGIC INPUTS ¹³				
All Inputs Except SCLOCK, RESET, and XTAL1				
V _{INL} , Input Low Voltage	0.8	0.4	V max	
V _{INH} , Input High Voltage	2.0	2.0	V min	

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SPECIFICATIONS (continued)

Parameter	V _{DD} = 5 V	V _{DD} = 3 V	Unit	Test Conditions
SCLOCK and RESET Only ¹³ (Schmitt-Triggered Inputs)				
V _{T+}	1.3	0.95	V min	
	3.0	2.5	V max	
V _{T-}	0.8	0.4	V min	
	1.4	1.1	V max	
V _{T+} – V _{T-}	0.3	0.3	V min	
	0.85	0.85	V max	
INPUT CURRENTS				
P1.2–P1.7, DLOAD	±10	±10	µA max	V _{IN} = 0 V or V _{DD}
SCLOCK ¹⁴	–10	–3	µA min	V _{IN} = 0 V, Internal Pull-Up
	–40	–15	µA max	V _{IN} = 0 V, Internal Pull-Up
	±10	±10	µA max	V _{IN} = V _{DD}
RESET	±10	±10	µA max	V _{IN} = 0 V
	20	10	µA min	V _{IN} = 5 V, 3 V Internal Pull-Down
	105	35	µA max	V _{IN} = 5 V, 3 V Internal Pull-Down
P1.0, P1.1, Port 3 (includes MISO, MOSI/SDATA, and $\overline{SS}$)	±10	±10	µA max	V _{IN} = 5 V, 3 V
	±1	±1	µA typ	
	–180	–70	µA min	V _{IN} = 2 V, V _{DD} = 5 V, 3 V
	–660	–200	µA max	
	–360	–100	µA typ	
	–20	–5	µA min	V _{IN} = 450 mV, V _{DD} = 5 V, 3 V
	–75	–25	µA max	
	–38	–12	µA typ	
INPUT CAPACITANCE	5	5	pF typ	All Digital Inputs
CRYSTAL OSCILLATOR (XTAL1 AND XTAL2)				
Logic Inputs, XTAL1 Only				
V _{INL} , Input Low Voltage	0.8	0.4	V typ	
V _{INH} , Input High Voltage	3.5	2.5	V typ	
XTAL1 Input Capacitance	18	18	pF typ	
XTAL2 Output Capacitance	18	18	pF typ	
DIGITAL OUTPUTS				
Output High Voltage (V _{OH})	2.4	2.4	V min	I _{SOURCE} = 1.6 mA
Output Low Voltage (V _{OL})				
P1.0 and P1.1	0.4	0.4	V max	I _{SINK} = 10 mA, T _{MAX} = 85°C
P1.0 and P1.1	0.4	0.4	V max	I _{SINK} = 8 mA, T _{MAX} = 125°C
SCLOCK, MISO, MOSI	0.4	0.4	V max	I _{SINK} = 4 mA
All Other Outputs	0.4	0.4	V max	I _{SINK} = 1.6 mA
MCU CORE CLOCK				
MCU Clock Rate	131.1 16.78	131.1 16.78	kHz MHz	Clock Rate Generated via On-Chip PLL, Programmable via CD2-0 in PLLCON
START-UP TIME				
At Power-On	500	500	ms typ	
From Idle Mode	100	100	µs typ	
From Power-Down Mode				OSC_PD Bit = 0 in PLLCON SFR
Oscillator Running				
Wake-Up with $\overline{INT0}$ Interrupt	100	100	µs typ	
Wake-Up with SPI/I ² C Interrupt	100	100	µs typ	
Wake-Up with TIC Interrupt	100	100	µs typ	
Wake-Up with External RESET	3	3	ms typ	

Parameter	V _{DD} = 5 V	V _{DD} = 3 V	Unit	Test Conditions
START-UP TIME (continued)				
Oscillator Powered Down ¹⁵				OSC_PD Bit = 1 in PLLCON
Wake-Up with SPI/I ² C Interrupt	150	400	ms typ	
Wake-Up with TIC Interrupt	150	400	ms typ	
Wake-Up with External RESET	150	400	ms typ	
After External RESET in Normal Mode	3	3	ms typ	
After WDT Reset in Normal Mode	3	3	ms typ	Controlled via WDCON
FLASH/EE MEMORY RELIABILITY CHARACTERISTICS ¹⁶				
Endurance ¹⁷	100,000	100,000	cycles min	
Data Retention ¹⁸	100	100	years min	
POWER REQUIREMENTS ^{19, 20}				
Power Supply Voltages				
AV _{DD} /DV _{DD} – AGND		2.7	V min	AV _{DD} /DV _{DD} = 3 V Nominal
		3.3	V max	
	4.5		V min	AV _{DD} /DV _{DD} = 5 V Nominal
	5.5		V max	
Power Supply Currents – Normal Mode				
DV _{DD} Current ¹³	5	2.5	mA max	Core CLK = 2.097 MHz (CD Bits in PLLCON = 3)
	4	2	mA typ	
AV _{DD} Current ¹³	1.7	1.7	mA max	
DV _{DD} Current	20	10	mA max	Core CLK = 16.78 MHz (max)
	16	8	mA typ	(CD Bits in PLLCON = 0)
AV _{DD} Current	1.7	1.7	mA max	
DV _{DD} Current ¹³	3.5	1.5	mA max	Core CLK = 131.2 kHz (min)
	2.8	1.2	mA typ	(CD Bits in PLLCON = 7)
AV _{DD} Current	1.7	1.7	mA max	
Power Supply Currents – Idle Mode				
DV _{DD} Current ¹³	1.7	1.2	mA max	Core CLK = 2.097 MHz (CD Bits in PLLCON = 3)
	1.5	1	mA typ	
AV _{DD} Current ¹³	0.15	0.15	mA max	
DV _{DD} Current ¹³	6	3	mA max	Core CLK = 16.78 MHz (max)
	4	2.5	mA typ	(CD Bits in PLLCON = 0)
AV _{DD} Current ¹³	0.15	0.15	mA max	
DV _{DD} Current ¹³	1.25	1	mA max	Core CLK = 131 kHz (min)
	1.1	0.7	mA typ	(CD Bits in PLLCON = 7)
AV _{DD} Current ¹³	0.15	0.15	mA max	
Power Supply Currents – Power-Down Mode				
				Core CLK = 2.097 MHz or 16.78 MHz
DV _{DD} Current ¹³		20	μA max	(CD Bits in PLLCON = 3 or 0)
	40	14	μA typ	Oscillator ON
AV _{DD} Current	1	1	μA typ	
DV _{DD} Current		15	μA max	Oscillator OFF
	20	10	μA typ	
AV _{DD} Current	1	1	μA typ	
Typical Additional Power Supply Currents				Core CLK = 2.097 MHz, (CD Bits in PLLCON = 3)
				AV _{DD} = DV _{DD} = 5 V
PSM Peripheral	50		μA typ	
ADC	1.5		mA typ	
DAC	150		μA typ	

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SPECIFICATIONS (continued)

NOTES

- ¹Temperature range -40°C to $+125^{\circ}\text{C}$.
- ²ADC linearity is guaranteed when operating in nonpipelined mode, i.e., ADC conversion followed sequentially by a read of the ADC result. ADC linearity is also guaranteed during normal MicroConverter core operation.
- ³ADC LSB size = $V_{\text{REF}}/2^{12}$, i.e., for 2.5 V, 1 LSB = 610 μV and for External $V_{\text{REF}} = 1\text{ V}$, 1 LSB = 244 μV .
- ⁴Offset and gain error and offset and gain error match are measured after factory calibration.
- ⁵Based on external ADC system components, the user may need to execute a system calibration to remove additional external channel errors and achieve these specifications.
- ⁶SNR calculation includes distortion and noise components.
- ⁷Channel-to-channel crosstalk is measured on adjacent channels.
- ⁸The temperature monitor will give a measure of the die temperature directly; air temperature can be inferred from this result.
- ⁹DAC linearity is calculated using:
- Reduced Code Range of 48 to 4095, 0 to V_{REF} Range.
 - Reduced Code Range of 48 to 3950, 0 to V_{DD} Range.
 - DAC output load = 10 k Ω and 100 pF.
- ¹⁰DAC differential nonlinearity specified on 0 to V_{REF} and 0 to V_{DD} ranges.
- ¹¹Power-up time for the internal reference will be determined by the value of the decoupling capacitor chosen for both the VREF and CREF pins.
- ¹²When using an external reference device, the internal band gap reference input can be bypassed by setting the ADCCON1.6 bit. In this mode, the VREF and CREF pins need to be shorted together for correct operation.
- ¹³These numbers are not production tested but are guaranteed by design and/or characterization data on production release.
- ¹⁴Pins configured in I²C compatible mode or SPI mode; pins configured as digital inputs during this test.
- ¹⁵These typical specifications assume no loading on the XTAL2 pin. Any additional loading on the XTAL2 pin will increase the power-on times.
- ¹⁶Flash/EE memory reliability characteristics apply to both the Flash/EE program memory and the Flash/EE data memory.
- ¹⁷Endurance is qualified to 100 Kcycles as per JEDEC STD. 22 method A117 and measured at -40°C , $+25^{\circ}\text{C}$, and $+125^{\circ}\text{C}$; typical endurance at $+25^{\circ}\text{C}$ is 700 Kcycles.
- ¹⁸Retention lifetime equivalent at junction temperature (T_j) = 55°C as per JEDEC STD. 22 method A117. Retention lifetime based on an activation energy of 0.6e V will derate with junction temperature.
- ¹⁹Power supply current consumption is measured in normal, idle, and power-down modes under the following conditions:
- Normal Mode: Reset and all digital I/O pins = open circuit, core clk changed via CD Bits in PLLCON, and core executing internal software loop.
 - Idle Mode: Reset and all digital I/O pins = open circuit, core clk changed via CD Bits in PLLCON, PCON.0 = 1, and core execution suspended in idle mode.
 - Power-Down Mode: Reset and all other digital I/O pins = open circuit, core clk changed via CD Bits in PLLCON, PCON.1 = 1, core execution suspended in Power-Down Mode, and OSC turned ON or OFF via OSC_PD Bit (PLLCON.7) in PLLCON SFR.
- ²⁰DV_{DD} power supply current will increase typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

Specifications subject to change without notice.

Purchase of licensed I²C components of Analog Devices or one of its sublicensed associated companies conveys a license for the purchaser under the Phillips I²C Patent Rights to use the ADuC814 in an I²C system, provided that the system conforms to the I²C standard specifications as defined by Phillips.

TIMING SPECIFICATIONS^{1, 2, 3} ($AV_{DD} = 2.7\text{ V to }3.6\text{ V or }4.75\text{ V to }5.25\text{ V}$, $DV_{DD} = 2.7\text{ V to }3.6\text{ V or }4.75\text{ V to }5.25\text{ V}$; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.)

Parameter		32.768 kHz External Crystal			Unit	Figure
		Min	Typ	Max		
CLOCK INPUT (External Clock Driven XTAL1)						
t _{CK}	XTAL1 Period		30.52		μs	1
t _{CKL}	XTAL1 Width Low		15.16		μs	1
t _{CKH}	XTAL1 Width High		15.16		μs	1
t _{CKR}	XTAL1 Rise Time		20		ns	1
t _{CKF}	XTAL1 Fall Time		20		ns	1
1/t _{CORE}	ADuC814 Core Clock Frequency ⁴	0.131		16.78	MHz	
t _{CORE}	ADuC814 Core Clock Period ⁵		0.476		μs	
t _{CYC}	ADuC814 Machine Cycle Time ⁶	0.72	5.7	91.55	μs	

NOTES

¹AC inputs during testing are driven at $DV_{DD} - 0.5\text{ V}$ for a Logic 1 and 0.45 V for a Logic 0. Timing measurements are made at V_{IH} min for a Logic 1, and V_{IL} max for a Logic 0, as shown in Figure 2.

²For timing purposes, a port pin is no longer floating when a 100 mV change from the load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs, as shown in Figure 2.

³CLOAD for all outputs = 80 pF , unless otherwise noted.

⁴ADuC814 internal PLL locks onto a multiple 512 times the external crystal frequency of 32.768 kHz to provide a stable 16.777216 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core_CLK, selected via the PLLCON SFR.

⁵This number is measured at the default Core_CLK operating frequency of 2.09 MHz .

⁶ADuC814 machine cycle time is nominally defined as $12/\text{Core_CLK}$.

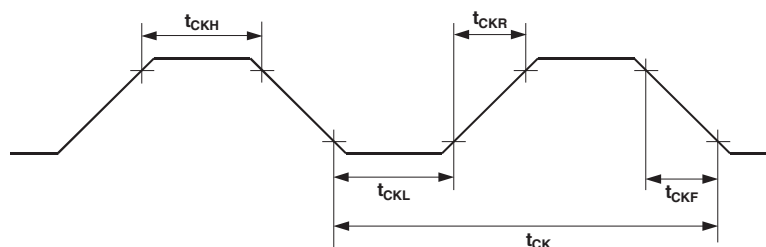


Figure 1. XTAL1 Input

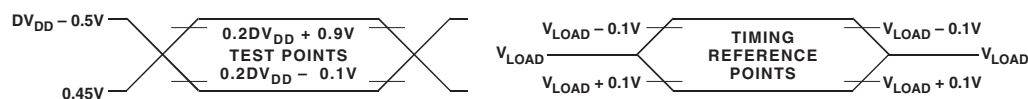


Figure 2. Timing Waveform Characteristics

TIMING SPECIFICATIONS (continued)

Parameter	16.78 MHz Core_CLK			Variable Core_CLK			Unit	Figure
	Min	Typ	Max	Min	Typ	Max		
UART TIMING (Shift Register Mode)								
t _{XLXL}	Serial Port Clock Cycle Time		715	12t _{CORE}			μs	3
t _{QVXH}	Output Data Setup to Clock		463	10t _{CORE} – 133			ns	3
t _{DVXH}	Input Data Setup to Clock		252	2t _{CORE} + 133			ns	3
t _{XHDX}	Input Data Hold after Clock		0	0			ns	3
t _{XHQX}	Output Data Hold after Clock		22	2t _{CORE} – 117			ns	3

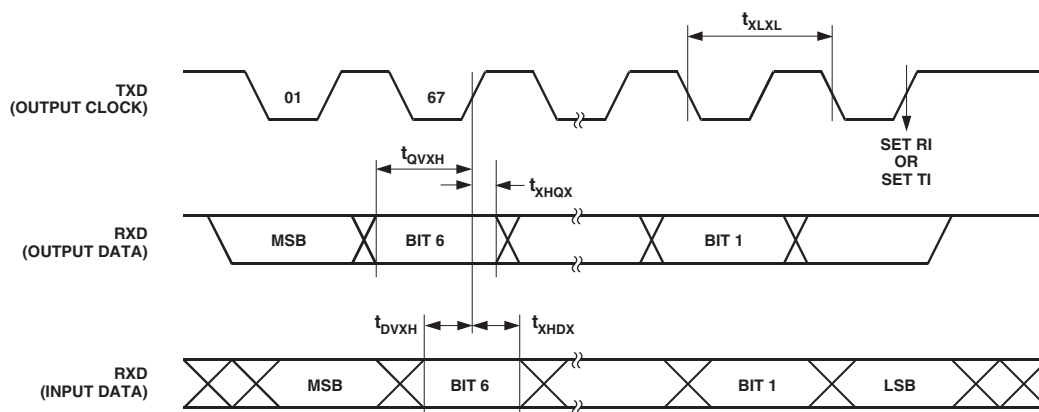


Figure 3. UART Timing in Shift Register Mode

Parameter	Min	Typ	Max	Unit	Figure
SPI MASTER MODE TIMING (CPHA = 1)					
t_{SL} SCLOCK Low Pulsewidth*		630		ns	4
t_{SH} SCLOCK High Pulsewidth*		630		ns	4
t_{DAV} Data Output Valid after SCLOCK Edge			50	ns	4
t_{DSU} Data Input Setup Time before SCLOCK Edge	100			ns	4
t_{DHD} Data Input Hold Time after SCLOCK Edge	100			ns	4
t_{DF} Data Output Fall Time		10	25	ns	4
t_{DR} Data Output Rise Time		10	25	ns	4
t_{SR} SCLOCK Rise Time		10	25	ns	4
t_{SF} SCLOCK Fall Time		10	25	ns	4

*Characterized under the following conditions:

- Core clock divider Bits CD2, CD1, and CD0 in PLLCON SFR set to 0, 1, and 1, respectively, i.e., core clock frequency = 2.09 MHz.
- SPI bit rate selection Bits SPR1 and SPR0 in SPICON SFR set to 0 and 0, respectively.

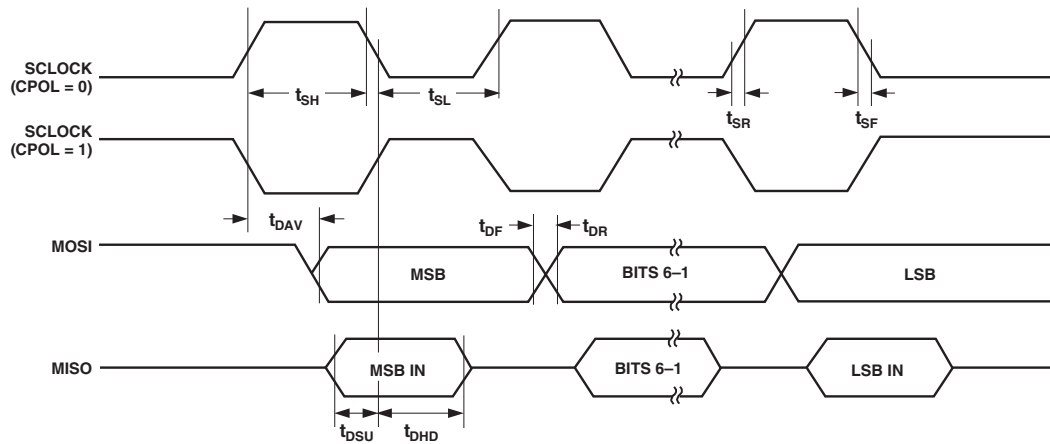


Figure 4. SPI Master Mode Timing (CPHA = 1)

TIMING SPECIFICATIONS (continued)

Parameter	Min	Typ	Max	Unit	Figure
SPI MASTER MODE TIMING (CPHA = 0)					
t_{SL} SCLOCK Low Pulsewidth*		630		ns	5
t_{SH} SCLOCK High Pulsewidth*		630		ns	5
t_{DAV} Data Output Valid after SCLOCK Edge			50	ns	5
t_{DOSU} Data Output Setup before SCLOCK Edge			150	ns	5
t_{DSU} Data Input Setup Time before SCLOCK Edge	100			ns	5
t_{DHD} Data Input Hold Time after SCLOCK Edge	100			ns	5
t_{DF} Data Output Fall Time		10	25	ns	5
t_{DR} Data Output Rise Time		10	25	ns	5
t_{SR} SCLOCK Rise Time		10	25	ns	5
t_{SF} SCLOCK Fall Time		10	25	ns	5

*Characterized under the following conditions:

- Core clock divider Bits CD2, CD1, and CD0 in PLLCON SFR set to 0, 1, and 1, respectively, i.e., core clock frequency = 2.09 MHz.
- SPI bit rate selection Bits SPR1 and SPR0 in SPICON SFR set to 0 and 0, respectively.

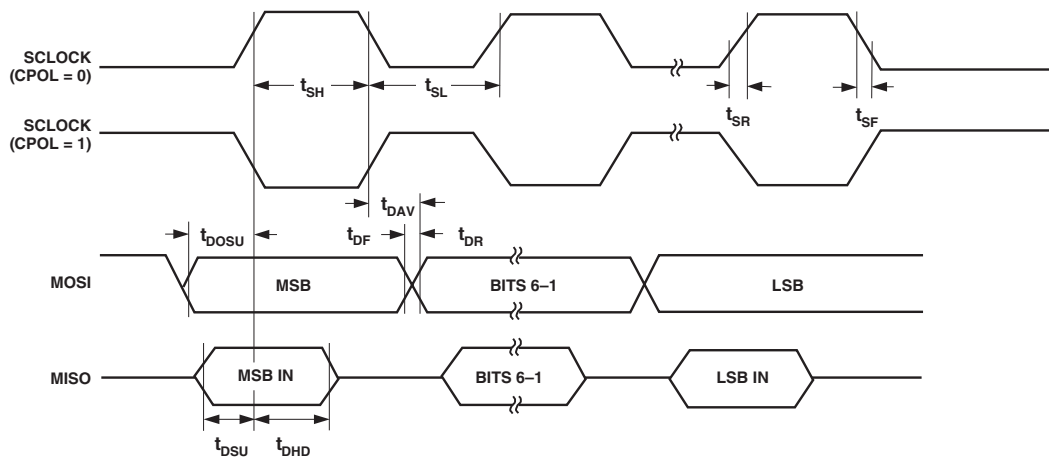


Figure 5. SPI Master Mode Timing (CPHA = 0)

Parameter	Min	Typ	Max	Unit	Figure
SPI SLAVE MODE TIMING (CPHA = 1)					
t_{SS} $\overline{SS}$ to SCLOCK Edge	0			ns	6
t_{SL} SCLOCK Low Pulsewidth		330		ns	6
t_{SH} SCLOCK High Pulsewidth		330		ns	6
t_{DAV} Data Output Valid after SCLOCK Edge			50	ns	6
t_{DSU} Data Input Setup Time before SCLOCK Edge	100			ns	6
t_{DHD} Data Input Hold Time after SCLOCK Edge	100			ns	6
t_{DF} Data Output Fall Time		10	25	ns	6
t_{DR} Data Output Rise Time		10	25	ns	6
t_{SR} SCLOCK Rise Time		10	25	ns	6
t_{SF} SCLOCK Fall Time		10	25	ns	6
t_{SFS} $\overline{SS}$ High after SCLOCK Edge	0			ns	6

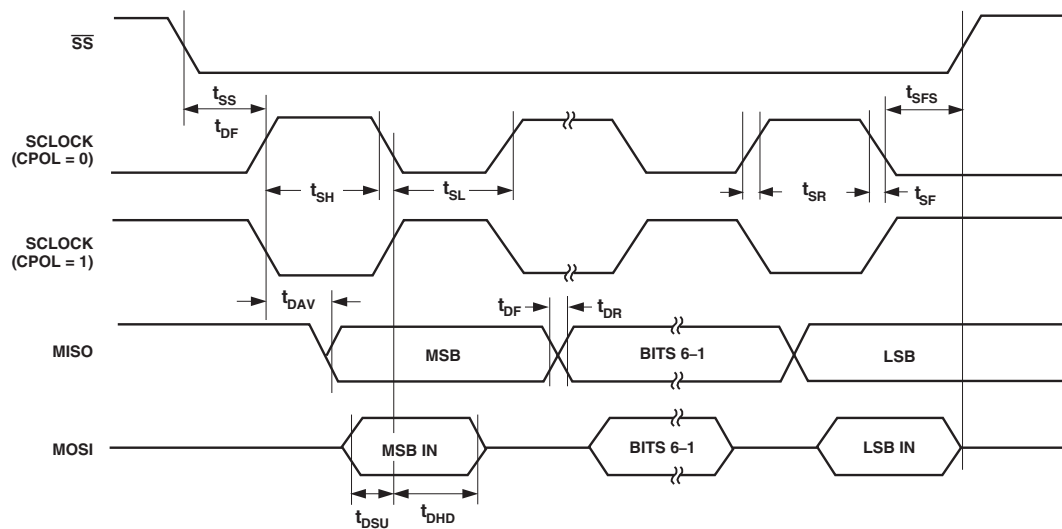


Figure 6. SPI Slave Mode Timing (CPHA = 1)

Parameter	Min	Typ	Max	Unit	Figure
SPI SLAVE MODE TIMING (CPHA = 0)					
t_{SS} $\overline{SS}$ to SCLOCK Edge	0			ns	7
t_{SL} SCLOCK Low Pulsewidth		330		ns	7
t_{SH} SCLOCK High Pulsewidth		330		ns	7
t_{DAV} Data Output Valid after SCLOCK Edge			50	ns	7
t_{DSU} Data Input Setup Time before SCLOCK Edge		100		ns	7
t_{DHD} Data Input Hold Time after SCLOCK Edge	100			ns	7
t_{DF} Data Output Fall Time		10	25	ns	7
t_{DR} Data Output Rise Time		10	25	ns	7
t_{SR} SCLOCK Rise Time		10	25	ns	7
t_{SF} SCLOCK Fall Time		10	25	ns	7
t_{SSR} $\overline{SS}$ to SCLOCK Edge			50	ns	7
t_{DOSS} Data Output Valid after $\overline{SS}$ Edge			20	ns	7
t_{SFS} $\overline{SS}$ High after SCLOCK Edge	0			ns	7

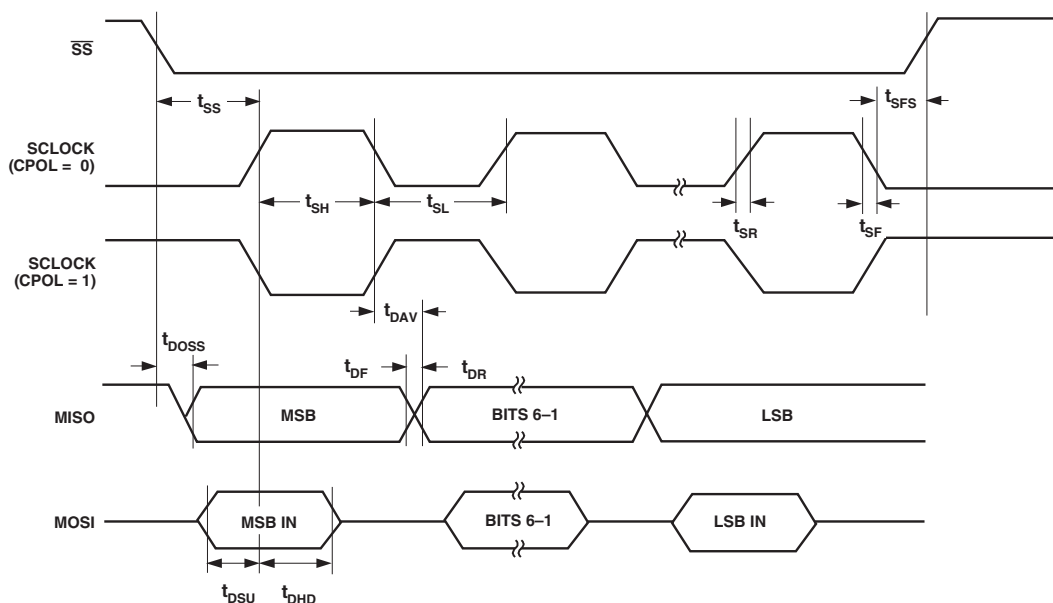


Figure 7. SPI Slave Mode Timing (CPHA = 0)

ABSOLUTE MAXIMUM RATINGS¹(T_A = 25°C, unless otherwise noted.)

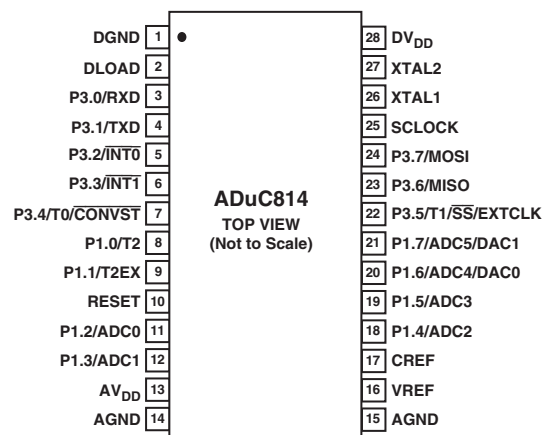
AV _{DD} to AGND	−0.3 V to +7 V
DV _{DD} to AGND	−0.3 V to +7 V
AV _{DD} to DV _{DD}	−0.3 V to +0.3 V
AGND to DGND ²	−0.3 V to +0.3 V
Analog Input Voltage to AGND ³	−0.3 V to AV _{DD} + 0.3 V
Reference Input Voltage to AGND	−0.3 V to AV _{DD} + 0.3 V
Analog Input Current (Indefinite)	30 mA
Reference Input Current (Indefinite)	30 mA
Digital Input Voltage to DGND	−0.3 V to DV _{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DV _{DD} + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ _{JA} Thermal Impedance	97.9°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²AGND and DGND are shorted internally on the ADuC814.

³Applies to P1.2 to P1.7 pins operating in analog or digital input modes.

**PIN CONFIGURATION
28-Lead TSSOP****ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option
ADuC814ARU	−40°C to +125°C	Thin Shrink Small Outline Package	RU-28
ADuC814BRU	−40°C to +125°C	Thin Shrink Small Outline Package	RU-28

QuickStart Development System Model	Description
EVAL-ADuC814QS	Development System for the ADuC814 MicroConverter Contains: • Evaluation Board • Serial Port Cable • Windows Serial Downloader (WSD) • Windows Debugger (DeBug) • Windows ADuC814 Simulator (ADSIM) • Windows ADC Analysis Software Program (WASP) • 8051 Assembler (Metalink) • Example Code • Documentation

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADuC814 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type*	Function
1	DGND	S	Digital Ground. Ground reference point for the digital circuitry.
2	DLOAD	I	Enables Debug/Serial Download Mode when pulled high through a resistor on power-on or RESET. In this mode, DLOAD may also be used as an external emulation I/O pin, and therefore, the voltage level at this pin must not be changed during this mode of operation since it may cause an emulation interrupt that will halt code execution. User code is executed when this pin is pulled low on power-on or RESET.
3-7	P3.0–P3.4	I/O	P3.0–P3.4 are bidirectional port pins with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state, can be used as inputs. As inputs, Port 3 pins being pulled externally low will source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active during S1 of the instruction cycle. Port 3 pins also have various secondary functions that are described below.
3	P3.0/RXD	I/O	Receiver Data Input (Asynchronous) or Data Input/Output (Synchronous) in Serial (UART) Mode
4	P3.1/TXD	I/O	Transmitter Data Output (Asynchronous) or Clock Output (Synchronous) in Serial (UART) Mode
5	P3.2/ $\overline{\text{INT0}}$	I/O	Interrupt 0 programmable edge or level triggered interrupt input, that can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 0.
6	P3.3/ $\overline{\text{INT1}}$	I/O	Interrupt 1 programmable edge or level triggered interrupt input, that can be programmed to one of two priority levels. This pin can also be used as a gate control input to Timer 1.
7	P3.4/T0/ $\overline{\text{CONVST}}$	I/O	Timer/Counter 0 Input and External Trigger Input for ADC Conversion Start
8-9	P1.0–P1.1	I/O	P1.0–P1.1 are bidirectional port pins with internal pull-up resistors. Port 1 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state, can be used as inputs. As inputs, Port 1 pins being pulled externally low will source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active during S1 of the instruction cycle. Port 1 pins also have various secondary functions that are described below.
8	P1.0/T2	I/O	Timer 2 Digital Input. Input to Timer/Counter 2. When enabled, Counter 2 is incremented in response to a 1 to 0 transition of the T2 input.
9	P1.1/T2EX	I/O	Digital Input. Capture/reload trigger for Counter 2.
10	RESET	I	Reset Input. A high level on this pin while the oscillator is running resets the device. There is an internal weak pull-down and a Schmitt trigger input stage on this pin.
11-12	P1.2–P1.3	I	These pins have no digital output drivers, i.e., they can only function as digital inputs, for which 0 must be written to the Port Bit. These port pins also have the following analog functionality.
11	P1.2/ADC0	I	ADC Input Channel 0, Selected via ADCCON2 SFR
12	P1.3/ADC1	I	ADC Input Channel 1, Selected via ADCCON2 SFR
13	AV _{DD}	S	Analog Positive Supply Voltage, 3 V or 5 V
14, 15	AGND	G	Analog Ground. Ground reference point for the analog circuitry.

Pin No.	Mnemonic	Type*	Function
16	VREF	I/O	Reference Input/Output. This pin is connected to the internal reference through a switch and is the reference source for the analog-to-digital converter. The nominal internal reference voltage is 2.5 V, which appears at the pin. This pin can be used to connect an external reference to the analog-to-digital converter by setting ADCCON1.6 to 1.0. Connect 0.1 μ F between this pin and AGND.
17	CREF	I	Decoupling input for on-chip reference. Connect 0.1 μ F between this pin and AGND.
18-21	P1.4–P1.7	I	These pins have no digital output drivers, i.e., they can only function as digital inputs, for which 0 must be written to the Port Bit. These port pins also have the following analog functionality.
18	P1.4/ADC2	I	ADC Input Channel 2, Selected via ADCCON2 SFR
19	P1.5/ADC3	I	ADC Input Channel 2, Selected via ADCCON2 SFR
20	P1.6/ADC4/DAC0	I/O	ADC Input Channel 4, Selected via ADCCON2 SFR. The voltage DAC Channel 0 can also be configured to appear on P1.6
21	P1.7/ADC5/DAC1	I/O	ADC Input Channel 5, Selected via ADCCON2 SFR. The voltage DAC Channel 1 can also be configured to appear on P1.7
22-24	P3.5–P3.7	I/O	P3.5–P3.7 are bidirectional port pins with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state, can be used as inputs. As inputs, Port 3 pins being pulled externally low will source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active during S1 of the instruction cycle. Port 3 pins also have various secondary functions that are described below.
22	P3.5/T1	I/O	Timer/Counter 1 Input. P3.5–P3.7 pins also have SPI interface functions. To enable these functions, Bit 0 of the CFG814 SFR must be set to 1.
22	P3.5/ $\overline{SS}$ /EXTCLK	I/O	This pin also functions as the slave select input for the SPI interface when the device is operated in Slave Mode. P3.5 can also function as an input for an external clock. This clock effectively bypasses the PLL. This function is enabled by setting Bit 1 of the CFG814 SFR.
23	P3.6/MISO	I/O	SPI Master Input/Slave Output Data Input/Output Pin
24	P3.7/MOSI	I/O	SPI Master Output/Slave Input Data Input/Output Pin
25	SCLOCK	I/O	Serial Clock Pin for SPI Serial Interface Clock
26	XTAL1	I	Input to the Crystal Oscillator Inverter
27	XTAL2	O	Output from the Crystal Oscillator Inverter
28	DV _{DD}	S	Analog Positive Supply Voltage, 3 V or 5 V

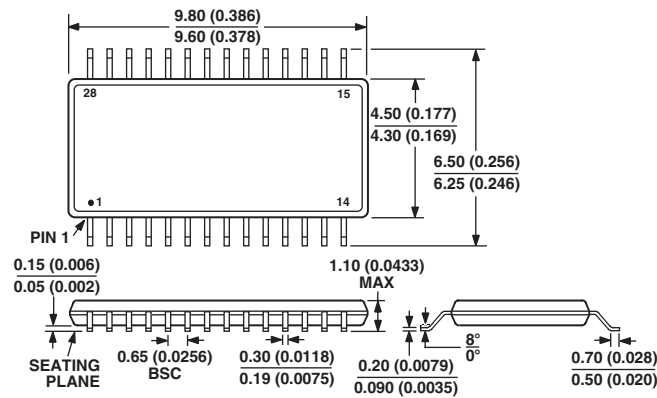
*I = Input, O = Output, I/O = Input and Output, and S = Supply.

NOTES

1. SET implies a Logic 1 state and CLEARED implies a Logic 0 state, unless otherwise stated.
2. SET and CLEARED also imply that the bit is set or automatically cleared by the ADuC814 hardware, unless otherwise stated.
3. User software should not write 1s to Reserved or Unimplemented Bits as they may be used in future products.

OUTLINE DIMENSIONS
28-Lead TSSOP Package
(RU-28)

Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE
ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE
FOR USE IN DESIGN