Document Title

512K x 32 x 4Banks Low Power SDRAM Specificaton

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	Apr 7 , 2006	Draft
0.1	DC parameter values are changed	Jul 21 , 2006	Advanced
0.2	DC parameter values are changed. Wafer spec & PAD allocation are attached. PAD coordinates are not fixed (TBD). Special MRS mode (Wrap off) supported.	Sep 2 , 2006	Advanced
0.3	Pad allocation changed. (NC Pad added to right bottom)	Sep 21 , 2006	Advanced
0.4	Pad coordinates are updated.	Dec 6 , 2006	Advanced
0.5	Pad allocation changed. (BA0,BA1)	Dec 19 , 2006	Advanced
0.6	DC parameter values are revised.	Sep 10 , 2007	

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512K x 32Bit x 4 Banks Low Power SDRAM

FEATURES

- 1.8V power supply.
- LVCMOS compatible with multiplexed address.
- Four banks operation.
- MRS cycle with address key programs.
  - -. CAS latency (1, 2 & 3).
  - -. Burst length(1, 2, 4, 8 & Full page).
  - -. Burst type (Sequential & Interleave).
- EMRS cycle with address key programs.
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation.
- Special Function Support.
  - -. PASR(Partial Array Self Refresh).
  - -. Internal auto TCSR (Temperature Compensated Self Refresh)
  - -. DS (Driver Strength)
  - -. Deep power down
- DQM for masking.
- Auto refresh.
- 64㎳ refresh period (4K cycle).
- Commercial Temperature Operation (-0℃ ~ 70℃)
  Extended Temperature Operation (-25℃ ~ 85℃)

GENERAL DESCRIPTION

The EMLS232UA series is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 534,288 words by 32 bits, fabricated with Ramsway's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
EMLS232UAW-6(E)	133㎒(CL3), 100㎒(CL2)	LVCMOS	Wafer Biz.

NOTE :

1. In case of 40㎒ Frequency, CL1 can be supported.
2. Ramsway are not designed or manufactured for use in a device or system that is used under circumstance in which human life is potentially at stake. Please contact to the memory marketing team in ramsway when considering the use of a product contained herein for any specific purpose, such as medical,aerospace, nuclear, military, vehicular or undersea repeater use.

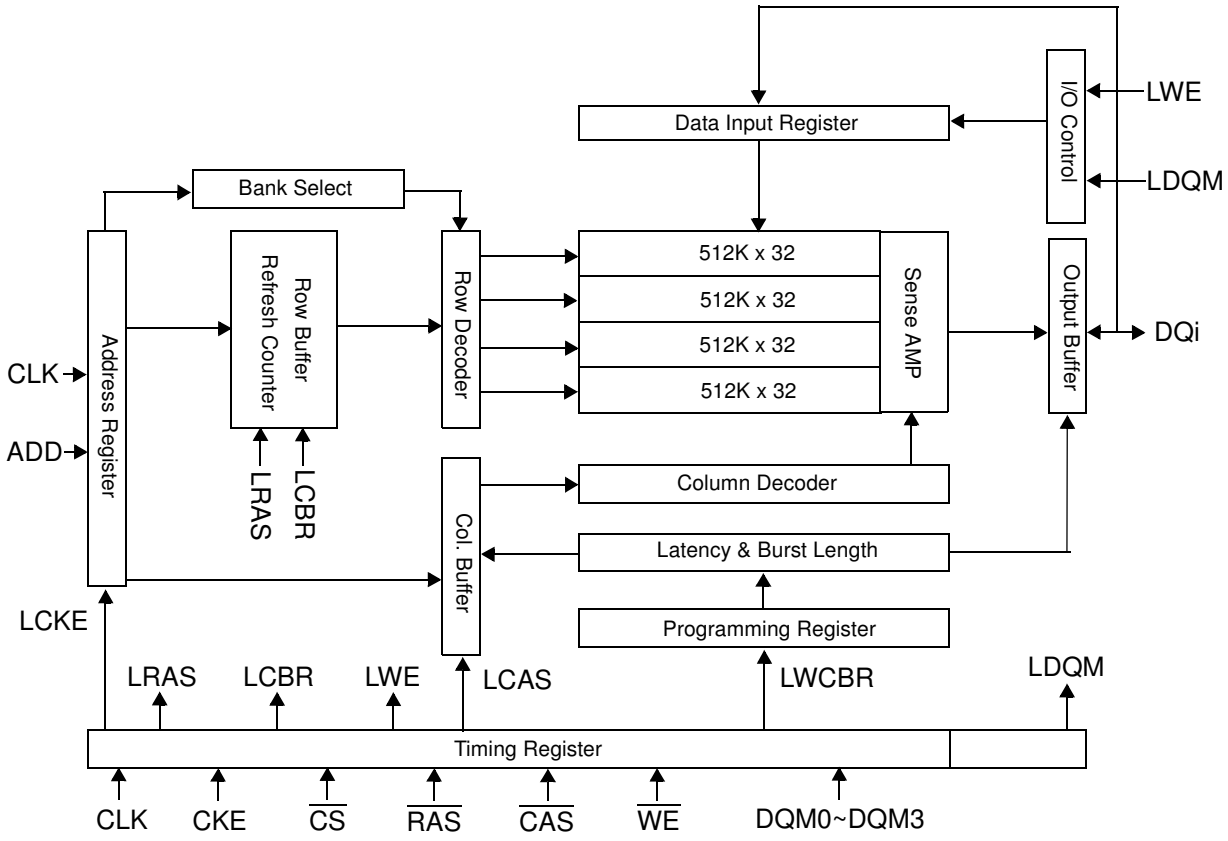
General Wafer Specifications

- Process Technology : 0.125um Trench DRAM Process
- Wafer thickness : 725 +/- 25um
- Typical Pad Open Size : 70.2um x 70.2um
- Minimum Pad Pitch : 93.6um
- Wafer Diameter : 8-inch

PAD FUNCTION DESCRIPTION

Pad	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
$\overline{CS}$	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{10}	Address	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, Column address : CA_0 ~ CA_7
BA_0 ~ BA_1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0~DQM3	Data input/output mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
$DQ_{0 \sim n}$	Data input/output	Data inputs/outputs are multiplexed on the same pins.: $DQ_{0 \sim 31}$
V_{DD}/V_{SS}	Power supply/ground	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	Data output power/ground	Isolated power supply and ground for the output buffers to provide improved noise immunity
N.C/RFU	No connection /reserved for future use	This pin is recommended to be left No Connection on the device.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 ~ 2.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 2.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	㎃

NOTE :
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25°C~ 85°C for Extended, 0°C~ 70°C for Commercial)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	1.7	1.8	1.95	V	1
	V_{DDQ}	1.7	1.8	1.95	V	1
Input logic high voltage	V_{IH}	0.8 x V_{DDQ}	1.8	V_{DDQ} + 0.3	V	2
Input logic low voltage	V_{IL}	-0.3	0	0.3	V	3
Output logic high voltage	V_{OH}	0.9 x V_{DDQ}	-	-	V	I_{OH} = -0.1㎃
Output logic low voltage	V_{OL}	-	-	0.2	V	I_{OL} = 0.1㎃
Input leakage current	I_{LI}	-2	-	2	㎂	4

NOTE :
1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2.V_{IH} (max) = 2.2V AC. The overshoot voltage duration is ≤ 3㎱
3.V_{IL} (min) = -1.0V AC. The undershoot voltage duration is ≤ 3㎱.
4.Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.
5.Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE

(V_{DD} = 1.8V, T_A = 23℃, f=1㎒, V_{REF} =0.9V ± 50 ㎷)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	1.5	3.5	pF	
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM0~DQM3	C_{IN}	1.5	3.0	pF	
Address	C_{ADD}	1.5	3.0	pF	
DQ_0 ~ DQ_{31}	C_{OUT}	2.0	4.5	pF	

DC CHARACTERISRICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0°C~ 70°C for Extended, -25°C~ 85°C for Commercial)

Parameter	Symbol	Test Condition		Version				Unit	Note
				133MHz					
Operating Current (One Bank Active)	I_{CC1}	Active mode; Burst length = 2; Read or Write; $t_{RC} \geq t_{RC}$(min); CL=3; t_{CC}=10ns; I_O= 0 mA		65				mA	1
Precharge Standby Current in power-down mode	$I_{CC2}P$	CKE ≤ V_{IL}(max), t_{CC}=10ns		0.15				mA	
	$I_{CC2}PS$	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		0.15					
Precharge Standby Current in non power-down mode	$I_{CC2}N$	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns; Input signals are changed one time during 20ns		15				mA	
	$I_{CC2}NS$	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞; Input signals are stable		2					
Active Standby Current in power-down mode	$I_{CC3}P$	CKE ≤ V_{IL}(max), t_{CC} = 10ns		0.5				mA	
	$I_{CC3}PS$	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		0.5					
Active Standby Current in non power-down mode (One Bank Active)	$I_{CC3}N$	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns; Input signals are changed one time during 20ns		20				mA	
	$I_{CC3}NS$	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞; Input signals are stable		10				mA	
Operating Current (Burst Mode)	I_{CC4}	I_O = 0mA; Page burst, CL=3, Read or Write, t_{CC} = 10ns; 4Banks Activated		75				mA	1
Refresh Current	I_{CC5}	$t_{ARFC} \geq t_{ARFC}$(min), t_{CC} = 10ns		80				mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	**Internal Auto TCSR**	**Max 15**	**Max 45**	**Max 70**	**Max 85**	℃	
			4 Banks	210	220	230	250	μA	
			2 Banks	160	170	180	190		
			1 Bank	130	135	140	150		
Deep Power Down mode current	I_{CC7}			10				μA	

NOTE :

1.Measured with outputs open.
2.Refresh period is 64ms.
3.Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

AC OPERATING TEST CONDITIONS

(V_{DD} = 1.7V ~ 1.95V, T_A = 0℃ ~ 70℃ for Commercial, -25℃ ~85℃ for Extendedl)

Parameter	Value	Unit
AC input levels(Vih/Vil)	0.9 × V_{DDQ} / 0.2	V
Input timing measurement reference level	0.5 × V_{DDQ}	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	0.5 × V_{DDQ}	V
Output load condition	See Figure 2	

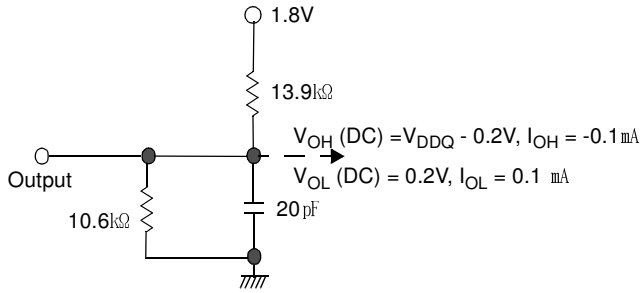


Figure 1. DC Output Load Circuit

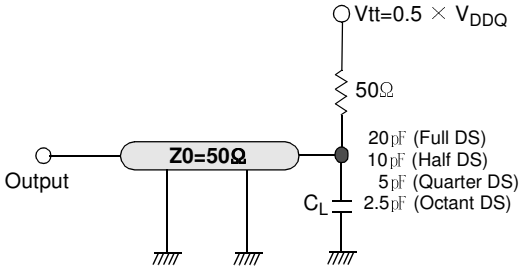


Figure 2. AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Value	Unit	Note
Row active to row active delay		t_{RRD}(min)	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}(min)	22.5	ns	1
Row precharge time		t_{RP}(min)	22.5	ns	1
Row active time		t_{RAS}(min)	45	ns	1
		t_{RAS}(max)	70,000	ns	
Row cycle time		t_{RC}(min)	67.5	ns	1
Last data in to row precharge		t_{RDL}(min)	15	ns	2
Last data in to Active delay		t_{DAL}(min)	t_{RDL} + t_{RP}	-	
Last data in to new col. address delay		t_{CDL}(min)	1	CLK	2
Last data in to burst stop		t_{BDL}(min)	1	CLK	2
Auto refresh cycle time		t_{ARFC}(min)	80	ns	3
Exit self refresh to active command		t_{SRFX}(min)	120	ns	
Col. address to col. address delay		t_{CCD}(min)	1	CLK	4
Number of valid output data	CAS latency=3		2	ea	5
Number of valid output data	CAS latency=2		1		
Number of valid output data	CAS latency=1		-		

NOTE :

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum dealy is required to complete write.
3. Maximum burst refresh cycle: 8
4. All parts allow every cycle column address change.
5. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	7.5	1000	ns	1
	CAS latency=2	t_{CC}	10			
	CAS latency=1	t_{CC}	-			
CLK to valid output delay	CAS latency=3	t_{AC}		6	ns	1,2,3
	CAS latency=2	t_{AC}		7		
	CAS latency=1	t_{AC}		-		
Output data hold time	CAS latency=3	t_{OH}	2.5		ns	2
	CAS latency=2	t_{OH}	2.5			
	CAS latency=1	t_{OH}	-			
CLK high pulse width		t_{CH}	2.5		ns	4
CLK low pulse width		t_{CL}	2.5		ns	4
Input setup time		t_{SS}	2.0		ns	4
Input hold time		t_{SH}	1		ns	4
CLK to output in Low-Z		t_{SLZ}	1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		6	ns	
	CAS latency=2			7		
	CAS latency=1			-		

NOTE :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1㎱, (tr/2-0.5)㎱ should be added to the parameter.
3. t_{AC}(max) value is measured at the low Vdd(1.7V) and cold temperature(-25℃).
   t_{AC} is measured in the device with half driver strength(C_L=10pF) and under the AC output load condition.
4. Assumed input rise and fall time (tr & tf) = 1㎱.
   If tr & tf is longer than 1㎱, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]㎱ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0, 1	A10/AP	A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Pre-charge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
Deep Power Down		Entry	H	L	L	H	H	L	X	X			
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X =Don't care, H=Logic High, L=Logic Low)

NOTE :

1. OP Code : Operand Code
   A0 ~ A10 & BA0 ~ BA1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS
3. Auto refresh functions are the same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
   Partial self refresh can be issued only after setting partial self refresh mode of EMRS.
4. BA0 ~BA1 : Bank select addresses.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation, it makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).

A. MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with Normal MRS

Address	BA0 ~ BA1	A10/AP[*1]	A9[*3]	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	"**0**" Setting for Normal MRS	Wrap Mode **0**: Wrap on **1**: Wrap off	W.B.L	Test Mode		CAS Latency			BT	Burst Length		

Normal MRS Mode

Test Mode			CAS Latency				Burst Type			Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type		A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential		0	0	0	1	1
0	1	Reserved	0	0	1	1	1	Interleave		0	0	1	2	2
1	0	Reserved	0	1	0	2	Mode Select			0	1	0	4	4
1	1	Reserved	0	1	1	3	BA1	BA0	Mode	0	1	1	8	8
Write Burst Length			1	0	0	Reserved	0	0	setting for Normal MRS	1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved				1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved				1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved				1	1	1	Full Page	Reserved

Full Page Length x32 : 64Mb(256)

Register Programmed with Extended MRS

Address	BA1	BA0	A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	Mode Select		RFU[*2]				DS		RFU[*2]		PASR		

EMRS for PASR(Partial Array Self Ref.) & DS(Driver Strength)

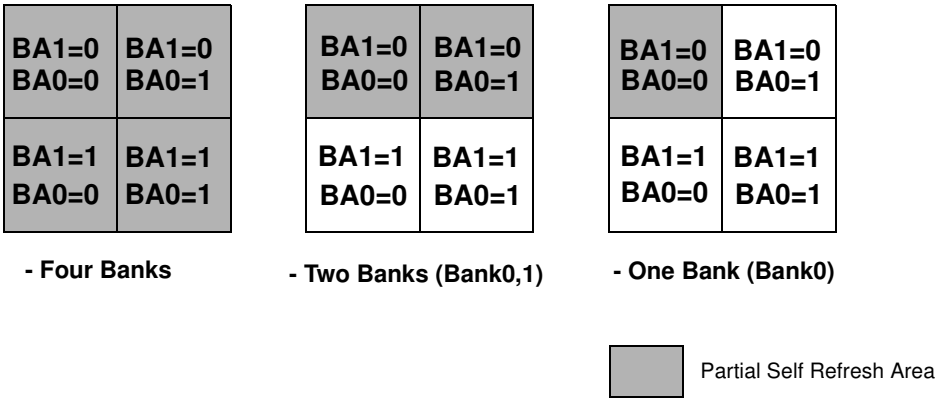
Mode Select			Driver Strength			PASR			
BA1	BA0	MODE	A6	A5	Driver Strength	A2	A1	A0	Size of Refreshed Array
0	0	Normal MRS	0	0	Full	0	0	0	Full Banks (default)
0	1	Reserved	0	1	1/2 (default)	0	0	1	Two Banks (Bank 0,1)
1	0	EMRS for Low Power SDRAM	1	0	1/4	0	1	0	One Bank (Bank 0)
1	1	Reserved	1	1	1/8	0	1	1	Reserved
Reserved Address						1	0	0	Reserved
A10/AP	A9	A8	A7	A4	A3	1	0	1	Reserved
0	0	0	0	0	0	1	1	0	Reserved
						1	1	1	Reserved

NOTE :

1. If A10/AP is high during MRS cycle, “Wrap off mode” function will be enabled. This mode support only sequential burst type.
2. RFU(Reserved for future use) should stay “0” during MRS cycle.
3. If A9 is high during MRS cycle, “Burst Read Single Bit Write” function will be enabled.

Partial Array Self Refresh

1. In order to save power consumption, Low Power SDRAM has PASR option.
2. Low Power SDRAM supports 3 kinds of PASR in self refresh mode : Four banks, Two banks and One bank.



Internal Temperature Compensated Self Refresh (TCSR)

NOTE :

1. In order to save power consumption,Low power SDRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically according to the two temperature range : Max 85℃, Max 70℃, Max 45℃, Max 15℃
2. If the EMRS for exteranl TCSR is issued by the controller, this EMRS code for TCRS is ignored.
3. It has +/- 5℃ tolerance.

Temperature Range	Self Refresh Current (Icc6)			Unit
	Full Array	1/2 of Full Array	1/4 of Full Array	
Max 85℃	250	190	150	μA
Max 70℃	230	180	140	
Max. 45℃[3]	220	170	135	
Max 15℃	210	160	130	

B. POWER UP SEQUENCE

1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
   -Apply V_{DD} before or at the same time as V_{DDQ}.
2. Maintain stable power, stable clock and NOP input condition for a mininmun of 200μs.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
6. Issue a extended mode register set command to define DS or PASR operating type of the device after normal MRS.

EMRS cycle is not mandatory and the EMRS command needs to be issued only when DS or PASR is used.
The default state without EMRS command issued is half driver strength and full array refreshed.
The device is now ready for the operation selected by EMRS.
For operating with DS or PASR, set DS or PASR mode in EMRS setting stage.
In order to adjust another mode in the state of DS or PASR mode, additional EMRS set is required but power up sequence is not needed again at this time. In that case, all banks have to be in idle state prior to adjusting EMRS set.

C. BURST SEQUENCE (Wrap on mode)

1. BURST LENGTH = 4

Initial Address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

2. BURST LENGTH = 8

Initial Address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0