Features

- **Digital Self-supervising Watchdog with Hysteresis**
- **One 250-mA Output Driver for Relay**
- **Enable Output Open Collector 8 mA**
- **Over/Undervoltage Detection**
- **ENABLE and RELAY Outputs Protected Against Standard Transients and 40V Load Dump**
- **ESD Protection According to MIL-STD-883 D Test Method 3015.7**
  - **Human Body Model: ±2 kV (100 pF, 1.5 kΩ)**
  - **Machine Model: ±200 V (200 pF, 0Ω)**

Pb Lead Free

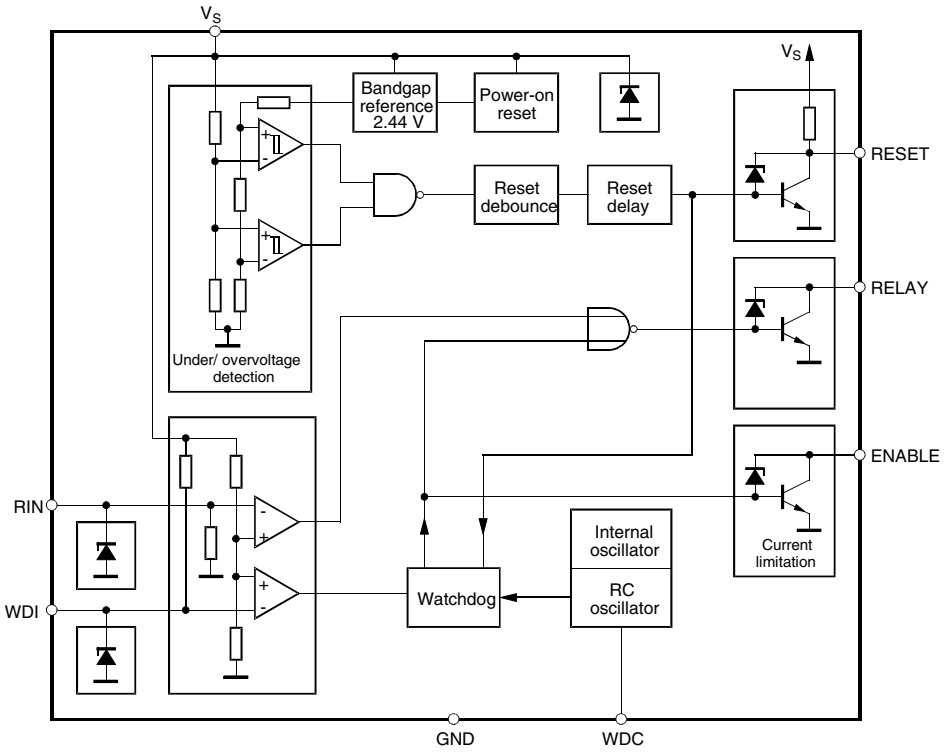
Special Fail-safe IC

U6808B

1. Description

The U6808B is designed to support the fail-safe function of a safety critical system (e.g., ABS). It includes a relay driver, a watchdog controlled by an external R/C-network and a reset circuit initiated by an over and undervoltage condition of the 5-V supply providing a low-level reset signal.

Figure 1-1. Block Diagram



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2. Pin Configuration

Figure 2-1. Pinning SO8

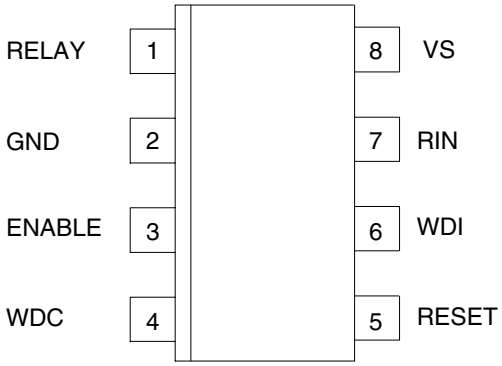


Table 2-1. Pin Description

Pin	Symbol	Type	Function	Logic
1	RELAY	Open collector driver output	Fail-safe relay driver	No signal: driver off Low: driver on
2	GND	Supply	Standard ground	No signal
3	ENABLE	Digital output	Negative reset signal	Low: reset
4	WDC	Analog input	External RC for watchdog timer	No signal
5	RESET	Digital output	Negative reset signal	Low: reset
6	WDI	Digital input	Watchdog trigger signal	Pulse sequence
7	RIN	Digital input	Activation of relay driver	High: driver on Low: driver off
8	VS	Supply	5-V supply	–

3. Fail-safe Functions

A fail-safe IC has to maintain its monitoring function even if there is a fault condition at one of the pins (e.g., short circuit). This ensures that a microcontroller system is not brought into a critical status. A critical status is reached if the system is not able to switch off the relay and to give a signal to the microcontroller via the ENABLE and RESET outputs. The following table shows the fault conditions for the pins.

Table 3-1. Table of Fault Conditions

Pin	Function	Short to V_S	Short to V_{Bat}	Short to GND	Open Circuit
RIN	Digital input to activate the fail-safe relay	Relay on	Relay on	Relay off	Relay off
WDI	Watchdog trigger input	Watchdog reset	Watchdog reset	Watchdog reset	Watchdog reset
OSC	Capacitor and resistor of watchdog	Watchdog reset	Watchdog reset	Watchdog reset	Watchdog reset
RELAY	Driver of the fail-safe relay			Relay on	Relay off

4. Truth Tables

Table 4-1. Truth Table for Over and Undervoltage Conditions

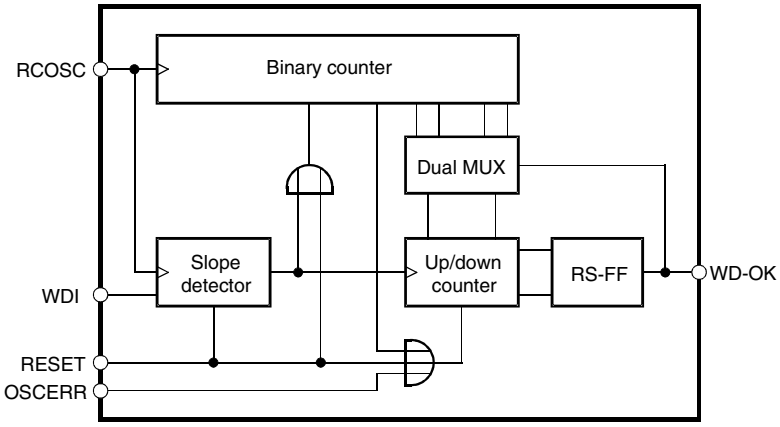
Supply Voltage (V_S)	Relay Input (RIN)	Relay Output Driver (RELAY)	RESET Output (RESET)	Enable Output Driver (ENABLE)
Normal	Low	Off	High	Off
	High	On	High	Off
Too low	Low	Off	Low	On
	High	Off	Low	On
Too high	Low	Off	Low	On
	High	Off	Low	On

Table 4-2. Truth Table for Watchdog Failures (Reset Output Do Not Care)

Watchdog Input (WDI)	Relay Input (RIN)	Relay Output Driver (RELAY)	Enable Output Driver (ENABLE)
Normal	Low	Off	Off
	High	On	Off
Too slow	Low	Off	On
	High	Off	On
Too fast	Low	Off	On
	High	Off	On

5. Description of the Watchdog

Figure 5-1. Watchdog Block Diagram



5.1 Abstract

The microcontroller is monitored by a digital window watchdog which accepts an incoming trigger signal of a constant frequency for correct operation. The frequency of the trigger signal can be varied in a broad range as the watchdog's time window is determined by external R/C components. The following description refers to the block diagram, see Figure 5-1.

5.2 WDI Input

The microcontroller has to provide a trigger signal with the frequency f_{WDI} which is fed to the WDI input. A positive edge of f_{WDI} detected by a slope detector resets the binary counter and clocks the up/down counter additionally. The latter one counts only from 0 to 3 or reverse. Each correct trigger increments the up/down counter by 1, each wrong trigger decrements it by 1. As soon as the counter reaches status 3 the RS flip-flop is set (see Figure 5-2). A missing incoming trigger signal is detected after 250 clocks of the internal watchdog frequency f_{RC} (see section “WD-OK Output”) and resets the up/down counter directly.

5.3 RCOSC Input

With an external R/C circuitry the IC generates a time base (frequency f_{WDC}) independent from the microcontroller. The watchdog's time window refers to a frequency of

$$f_{WDC} = 100 \times f_{WDI}$$

5.4 OSCERR Input

A smart watchdog has to ensure that internal problems with its own time base are detected and do not lead to an undesired status of the complete system. If the RC oscillator stops oscillating a signal is fed to the OSCERR input after a time-out delay. It resets the up/down counter and disables the WD-OK output.

Without this reset function the watchdog would freeze in its current status when f_{RC} stops.

5.5 RESET Input

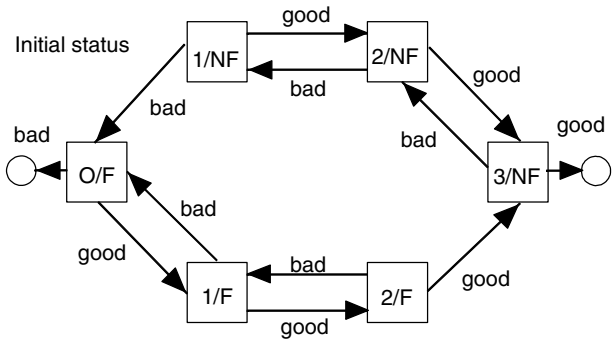
During power-on and under/overvoltage detection a reset signal is fed to this pin. It resets the watchdog timer and sets the initial state.

5.6 WD-OK Output

After the up/down counter is incremented to status 3 (see Figure 5-2) the RS flip-flop is set and the WD-OK output becomes logic 1. This information is available for the microcontroller at the open-collector output ENABLE. If on the other hand the up/down counter is decremented to 0 the RS flip-flop is reset, the WD-OK output and the ENABLE output are disabled. The WD-OK output also controls a dual MUX stage which shifts the time window by one clock after a successful trigger, thus forming a hysteresis to provide stable conditions for the evaluation of the trigger signal good or false. The WD-OK signal is also reset in case the watchdog counter is not reset after 250 clocks (missing trigger signal).

5.7 Watchdog State Diagram

Figure 5-2. Watchdog State Diagram



5.8 Explanation

In each block, the first character represents the state of the counter. The second notation indicates the fault status of the counter. A fault status is indicated by an F and a no fault status is indicated by an NF. When the watchdog is powered up initially, the counter starts out at the 0/F block (initial state). Good indicates that a pulse has been received whose width resides within the timing window. Bad indicates that a pulse has been received whose width is either too short or too long.

5.9 Watchdog Window Calculation

5.9.1 Example with Recommended Values

C_{osc} = 3.3 nF (should be preferably 10%, NPO)

R_{osc} = 39 kΩ (may be 5%, R_{osc} < 100 kΩ due to leakage current and humidity)

5.9.2 RC Oscillator

$$t_{WDC}(s) = 10^{-3} \times [C_{osc}\,(nF) \times [(0.00078 \times R_{osc}\,(k\Omega)) + 0.0005]]$$

$$f_{WDC}(Hz) = 1/(t_{WDC})$$

5.9.3 Watchdog WDI

$$f_{WDI}(Hz) = 0.01 \times f_{WDC}$$

t_{WDC} = 100 µs → f_{WDC} = 10 kHz

f_{WDI} = 100 Hz → t_{WDI} = 10 ms

5.9.3.1 WDI Pulse Width for Fault Detection after 3 Pulses

Upper watchdog window

Minimum: $169/f_{WDC}$ = 16.9 ms → $f_{WDC}/169$ = 59.1 Hz
Maximum: $170/f_{WDC}$ = 17.0 ms → $f_{WDC}/170$ = 58.8 Hz

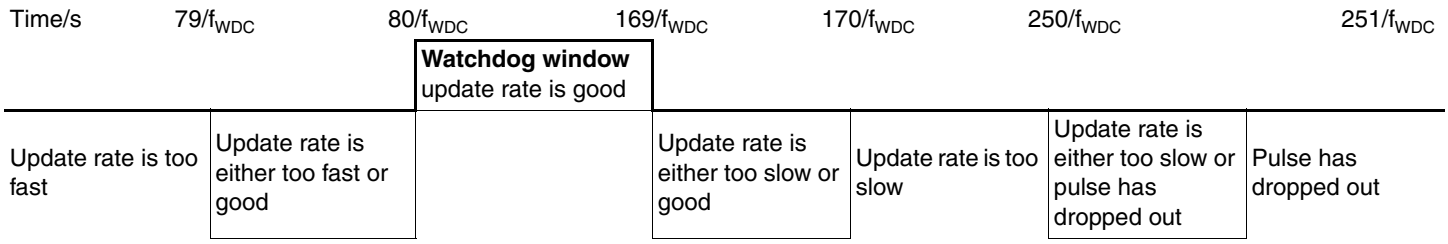
Lower watchdog window

Minimum: $79/f_{WDC}$ = 7.9 ms → $f_{WDC}/79$ = 126.6 Hz
Maximum: $80/f_{WDC}$ = 8.0 ms → $f_{WDC}/80$ = 125.0 Hz

5.9.3.2 WDI Dropouts for Immediate Fault Detection

Minimum: $250/f_{WDC}$ = 25 ms
Maximum: $251/f_{WDC}$ = 25.1 ms

Figure 5-3. Watchdog Timing Diagram with Tolerances



5.9.3.3 Reset Delay

The duration of the over or undervoltage pulses determines the enable and reset output. A pulse duration shorter than the debounce time has no effect on the outputs. A pulse longer than the debounce time results in the first reset delay. If a pulse appears during this delay, a second delay time is triggered. Therefore, the total reset delay time can be longer than specified in the data sheet.

6. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Supply-voltage range	V_S	–0.2 to +16	V
Power dissipation V_S = 5V, T_{amb} = –40°C V_S = 5V, T_{amb} = +125°C	 P_{tot} P_{tot}	 250 150	 mW mW
Thermal resistance	R_{thja}	160	K/W
Junction temperature	T_j	150	°C
Ambient temperature range	T_{amb}	–40 to +125	°C
Storage temperature range	T_{stg}	–55 to +155	°C

7. Electrical Characteristics

V_S = 5V, T_{amb} = –40 to +125°C, reference pin is GND, f_{intern} = 100 kHz + 50% – 45%, f_{WDC} = 10 kHz ±10%, f_{WDI} = 100 Hz

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage						
Operation range general		V_S	4.5		5.5	V
Operation range reset		V_S	1.2		16.0	V
Supply Current						
Relay off	T_{amb} = –40°C T_{amb} = +125°C				6	mA
Relay on	T_{amb} = –40°C T_{amb} = +125°C				15	mA
Digital Input WDI						
Detection low			–0.2		$0.2 \times V_S$	V
Detection high			$0.7 \times V_S$		V_S + 0.5V	V
Resistance to V_S			10		40	kΩ
Input current low	Input voltage = 0V		100		550	µA
Input current high	Input voltage = V_S		–5		+5	µA
Zener clamping voltage		V_{ZWDI}	20		24	V
Digital Input RIN						
Detection low			–0.2		$0.2 \times V_S$	V
Detection high			$0.7 \times V_S$		V_S + 0.5 V	V
Resistance to GND			10		40	kΩ
Input current low	Input voltage = 0V		–5		+5	µA
Input current high	Input voltage = V_S		100		550	µA
Zener clamping voltage		V_{ZRIN}	20		24	V

7. Electrical Characteristics (Continued)

V_S = 5V, T_{amb} = –40 to +125°C, reference pin is GND, f_{intern} = 100 kHz + 50% – 45%, f_{WDC} = 10 kHz ±10%, f_{WDI} = 100 Hz

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Digital Output RESET with Internal Pull-up						
Voltage high	Pull-up = 6 kΩ		0.7 × V_S + 0.1		V_S	V
Voltage low	I ≤ 1 mA 1.2V < V_S < 16V		0		0.3	V
Zener clamping voltage		V_{ZRESET}	26		30	V
Reset debounce time	Switch to low	t_{deb}	120	320	500	µs
Reset delay time	Switch back to high	t_{del}		50		ms
Digital Output ENABLE with Open Collector						
Saturation voltage low	I ≤ 8 mA		0.01		0.5	V
Zener clamping voltage		V_{ZEN}	26		30	V
Current limitation		I_{lim}	8			mA
Leakage current	V_{EN} = 5V V_{EN} = 16V V_{EN} = 26V	I_{EN5} I_{EN16} I_{EN26}			20 100 200	µA µA µA
Reset debounce time	Switch to low	t_{deb}	120	320	500	µs
Reset delay time	Switch back to high	t_{del}		85		ms
Relay Driver Output RELAY						
Saturation voltage	I ≤ 250 mA I ≤ 130 mA	V_{Rsat} V_{Rsat}			0.5 0.3	V V
Maximum load current	T_{amb} = –40 to +90°C T_{amb} > 90°C	I_R I_R	250 200			mA mA
Zener clamping voltage		V_{ZR}	26		30	V
Turn-off energy			30			mJ
Leakage current	V_R = 16V V_R = 26V	I_{R16} I_{R26}			20 200	µA µA
Reset and V_S Control						
Lower reset level		V_S	4.5		4.7	V
Upper reset level		V_S	5.35		5.6	V
Hysteresis			25		100	mV
Reset debounce time			120	320	500	µs
Reset delay			20	50	80	ms
RC Oscillator WDC						
Oscillator frequency	R_{OSC} = 39 kΩ, C_{OSC} = 3.3 nF	f_{WDC}	9	10	11	kHz
Watchdog Timing						
Power-on-reset prolongation time		t_{POR}	34.3		103.1	ms
Detection time for RC oscillator fault	V_{RC} = constant	$t_{RCerror}$	81.9		246	ms
Time interval for over-/undervoltage detection		$t_{D,OUV}$	0.16		0.64	ms
Reaction time of RESET output over/undervoltage		$t_{R,OUV}$	0.187		0.72	ms

7. Electrical Characteristics (Continued)

V_S = 5V, T_{amb} = –40 to +125°C, reference pin is GND, f_{intern} = 100 kHz + 50% – 45%, f_{WDC} = 10 kHz ±10%, f_{WDI} = 100 Hz

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Nominal frequency for WDI	$f_{RC} = 100 \times f_{WDI}$	f_{WDI}	10		130	Hz
Nominal frequency for WDC	$f_{WDI} = 1/100 \times f_{WDC}$	f_{WDC}	1		13	kHz
Minimum pulse duration for a securely WDI input pulse detection		$t_{P,WDI}$	182			µs
Frequency range for a correct WDI signal		f_{WDI}	64.7		112.5	Hz
Number of incorrect WDI trigger counts for locking the outputs		n_{lock}		3		
Number of correct WDI trigger counts for releasing the outputs		$n_{release}$		3		
Detection time for a stucked WDI signal	V_{WDI} = constant	$t_{WDIerror}$	24.5		25.5	ms
Watchdog Timing Relative to f_{WDC}						
Minimum pulse duration for a securely WDI input pulse detection				2		Cycles
Frequency range for a correct WDI signal			80		169	Cycles
Hysteresis range at the WDI ok margins				1		Cycle
Detection time for a dropped out WDI signal	V_{WDI} = constant		250		251	Cycles

8. Protection against Transient Voltages According to ISO TR 7637-3 Level 4 (Except Pulse 5)

Pulse	Voltage	Source Resistance[1]	Rise Time	Duration	Amount
1	–110V	10	100V/s	2 ms	15.000
2	+110V	10	100V/s	0.05 ms	15.000
3a	–160V	50	30V/ns	0.1s	1h
3b	+150V	50	20V/ns	0.1s	1h
5	40V	2	10V/ms	250 ms	20

Note: 1. Relay driver: relay coil with R_{min} = 70Ω to be added

9. Timing Diagrams

Figure 9-1. Watchdog in Too-fast Condition

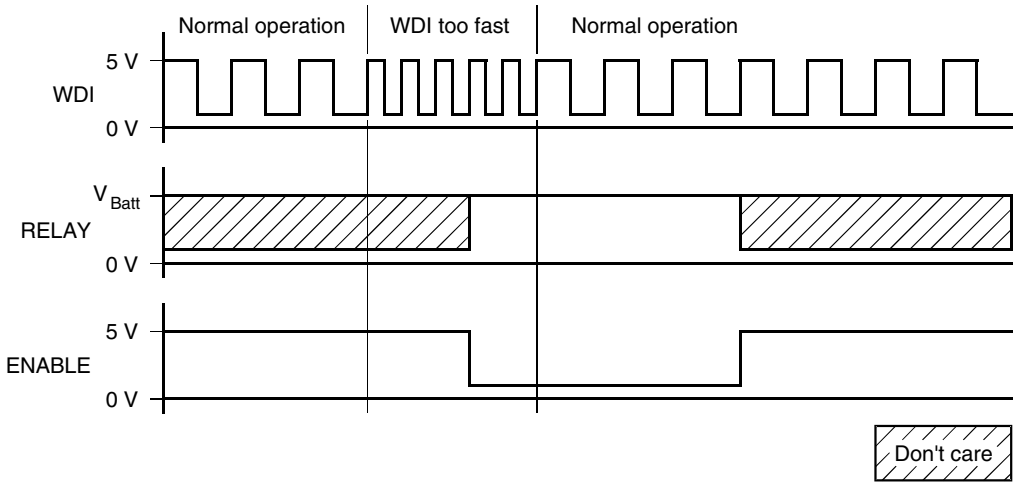


Figure 9-2. Watchdog in Too-slow Condition

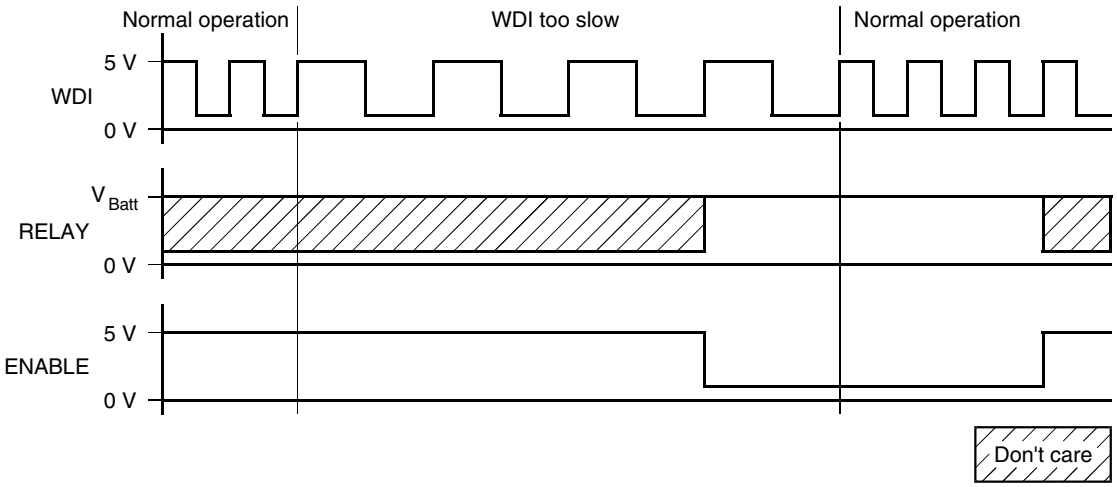


Figure 9-3. Overvoltage Condition

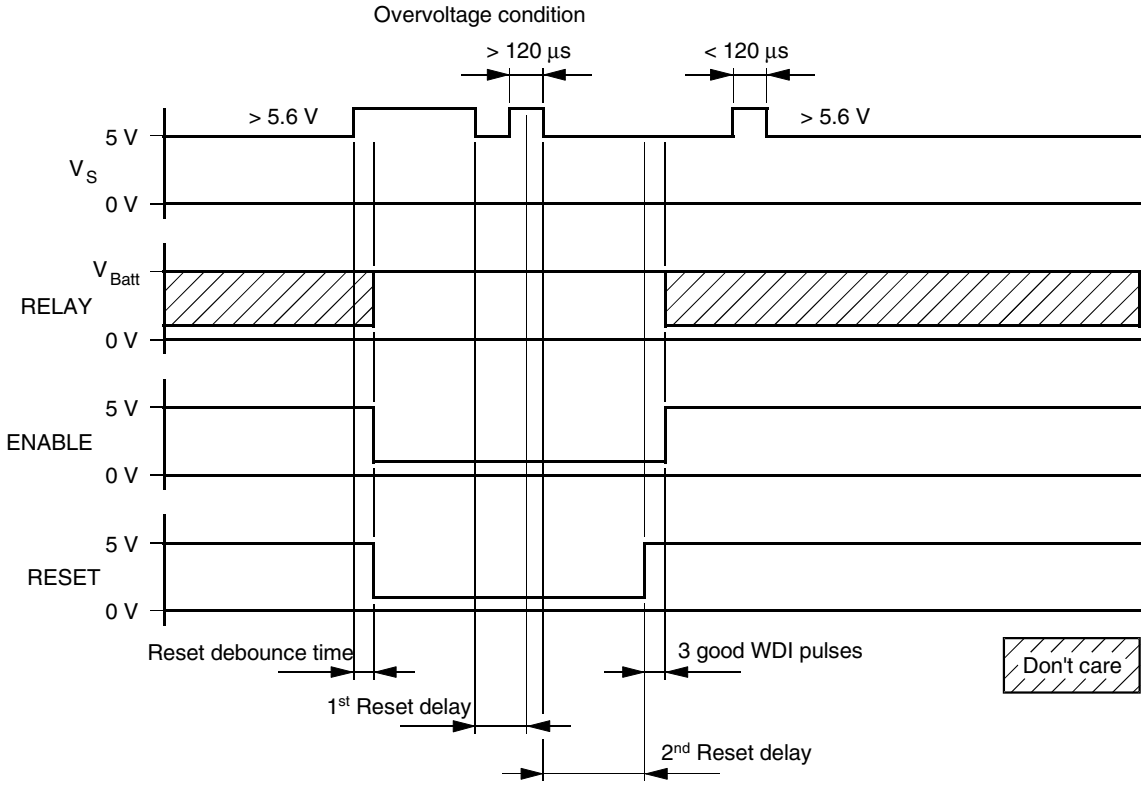


Figure 9-4. Undervoltage Condition

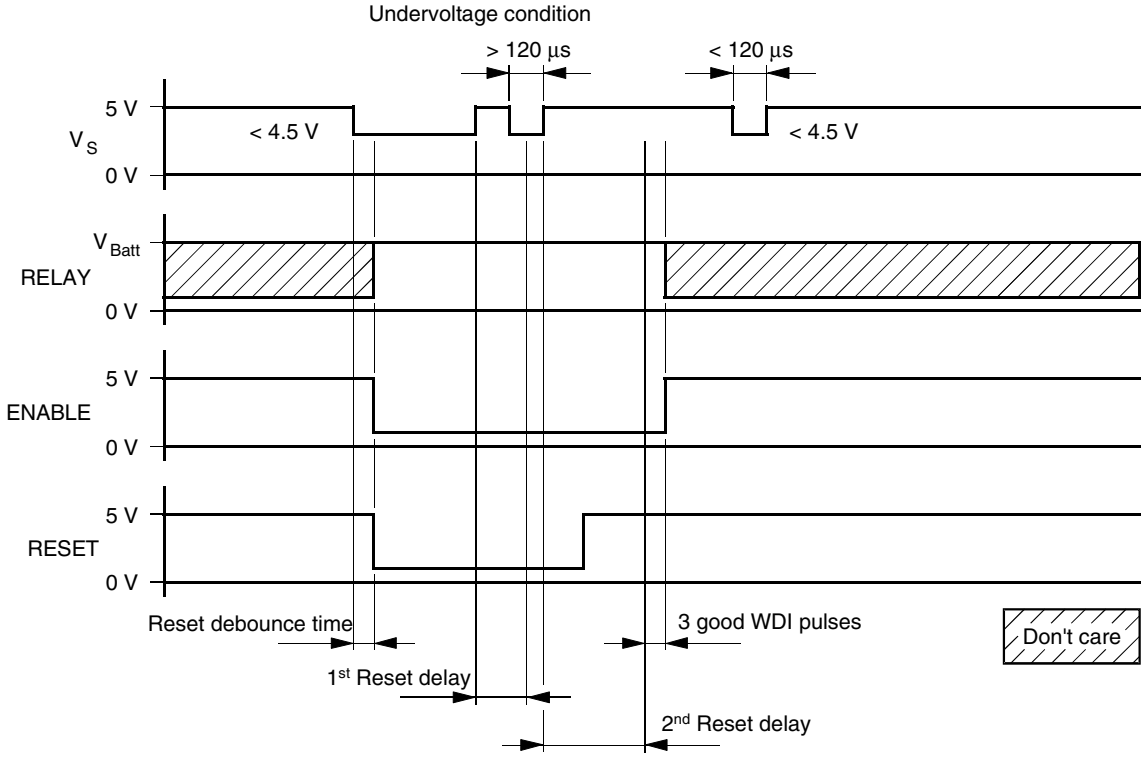
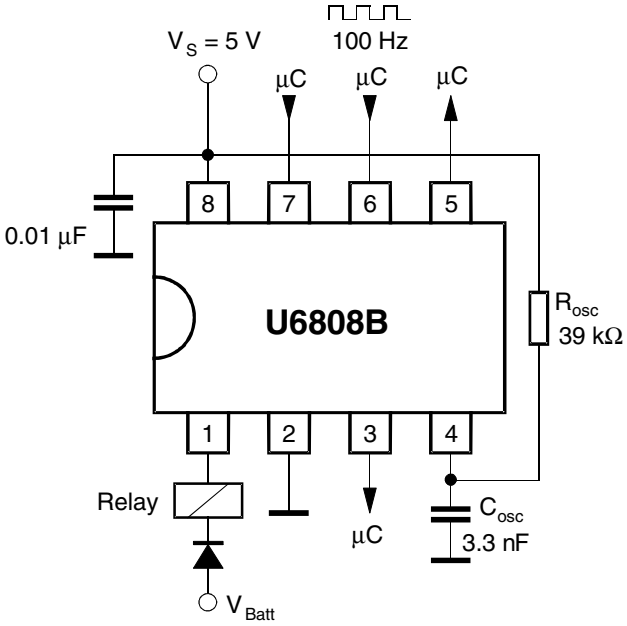


Figure 9-5. Application Circuit



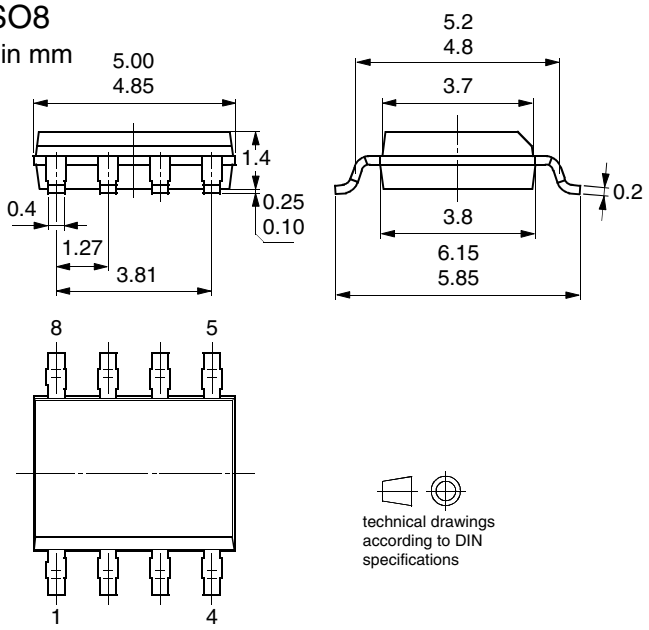
10. Ordering Information

Extended Type Number	Package	Remarks
U6808B-MFPY	SO8	Tube, Pb-free
U6808B-MFPG3Y	SO8	Taped and reeled, Pb-free

11. Package Information

Package SO8

Dimensions in mm



12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4707B-AUTO-10/05	• Put datasheet in a new template • Pb-free logo on page 1 added • New heading rows on Table “Absolute Maximum Ratings” on page 7 added • Table “Ordering Information” on page 13 changed

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