

## **CFK2162-P1**

800 to 900 MHz  
+34 dBm Power GaAs FET



Product Specifications  
July 1997 (1 of 4)

**Features**

- ❑ High Gain
- ❑ +34 dBm Power Output
- ❑ Proprietary Power FET Process
- ❑ >45% Linear Power Added Efficiency
- ❑ +29 dBm with 30 dBc Third Order Products
- ❑ Surface Mount SO-8 Power Package

**Applications**

- ❑ ISM Band Base Stations and Terminals
- ❑ Cellular Base Stations and Terminals
- ❑ Wireless Local Loop

**Description**

The CFK2162-P1 is a high-gain FET intended for driver amplifier applications in high-power systems, and output stage usage in medium power applications at power levels up to +34 dBm. The device is easily matched and provides excellent

**Specifications** (TA = 25°C) The following specifications are guaranteed at room temperature in Celeritek test fixture at 850 MHz.

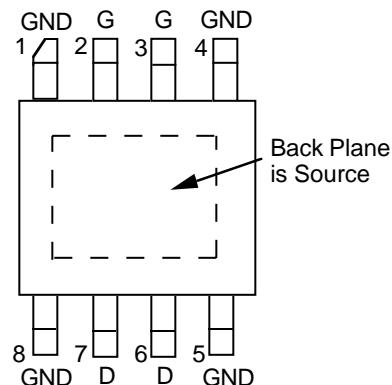
Parameters	Conditions	Min	Typ	Max	Units
<b>V<sub>d</sub> = 8V, I<sub>d</sub> = 800 mA (Quiescent)</b>					
P-1dB		33.0	34.0	—	dBm
SSG		19.0	20.0	—	dB
3rd Order Products <sup>(1)</sup>		26	30	—	dBc
Efficiency	@ P1dB	—	43	—	%
<b>V<sub>d</sub> = 5V, I<sub>d</sub> = 350 mA (Quiescent)</b>					
P-1dB		—	30.0	—	dBm
SSG		—	18.0	—	dB
<b>V<sub>d</sub> = 5V, I<sub>d</sub> = 1200 mA (Quiescent)</b>					
P-1dB		—	33.0	—	dBm
SSG		—	19.0	—	dB

Parameters	Conditions	Min	Typ	Max	Units
g <sub>m</sub>	V <sub>ds</sub> = 2.0V, V <sub>gs</sub> = 0V	—	1700	—	mS
I <sub>dss</sub>	V <sub>ds</sub> = 2.0V, V <sub>gs</sub> = 0V	—	2.8	—	A
V <sub>p</sub>	V <sub>ds</sub> = 3.0V, I <sub>ds</sub> = 65 mA	—	-1.8	—	Volts
BV <sub>GD</sub> <sup>(3)</sup>	I <sub>gd</sub> = 6.5 mA	18	20	—	Volts
θ <sub>JL</sub> <sup>(2)</sup>	@ 150°C TCH	—	10	—	°C/W

**Notes:**

- Sum to two tones with 1 MHz spacing = 29 dBm.
- See thermal considerations information on page 4.
- Max (+V<sub>d</sub>) and (-V<sub>g</sub>) under linear operation. Max potential difference across the device in RF compression (2V<sub>d</sub> + |V<sub>g</sub>|) not to exceed the minimum breakdown voltage (V<sub>br</sub>) of +18V.

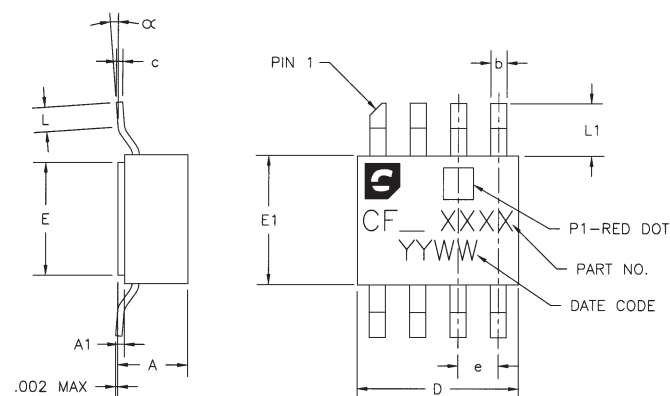
# 800 to 900 MHz +34 dBm Power GaAs FET

**Package Diagram**

linearity at 2 Watts. Manufactured in Celeritek's proprietary power FET process, this device is assembled in an industry standard surface mount SO-8 power package that is compatible with high volume, automated board assembly techniques.

**Absolute Maximum Ratings**

Parameter	Symbol	Rating
Drain-Source Voltage	V <sub>DS</sub>	12V <sup>(3)</sup>
Gate-Source Voltage	V <sub>GS</sub>	-5V
Drain Current	I <sub>DS</sub>	I <sub>dss</sub>
Continuous Dissipation	P <sub>T</sub>	10W
Channel Temperature	T <sub>CH</sub>	175°C
Storage Temperature	T <sub>STG</sub>	-65°C to +175°C

**SO-8 Power Package Physical Dimensions**

DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A		.086[2.184]	.100[2.540]
A1	.005[.1270]	.008[.2032]	.011[.2794]
b	.017[.4318]	.020[.5080]	.023[.5842]
c	.007[.1778]	.008[.2032]	.009[.2286]
D	.195[4.953]	.200[5.080]	.205[5.207]
E	.135[3.429]	.140[3.556]	.145[3.683]
E1	.155[3.937]	.160[4.064]	.165[4.191]
e		.050[1.270]	
L	.020[.5080]		.040[1.016]
L1	.055[1.397]	.065[1.651]	.075[1.905]
α	0°		8°

DIMENSIONS IN INCHES [MILLIMETERS]

## Typical Scattering Parameters

(TA = 25°C, Vds = 5 V, Ids = 350 mA)

Frequency (GHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.6	0.946	-162.45	4.973	86.73	0.017	11.14	0.739	172.95
0.7	0.945	-162.45	4.973	86.73	0.017	11.14	0.739	172.95
0.8	0.946	-171.49	3.657	79.26	0.019	8.47	0.746	170.91
0.9	0.947	-174.16	3.22	76.4	0.018	7.15	0.749	170.28
1.0	0.946	-176.06	2.885	73.75	0.018	9.37	0.748	169.73
1.1	0.946	-177.58	2.623	71.82	0.018	6.8	0.747	169.56
1.2	0.945	-178.58	2.424	69.66	0.019	6.59	0.746	169.16
1.3	0.944	-179.55	2.27	67.7	0.019	6.53	0.742	168.8
1.4	0.942	-179.53	2.154	65.68	0.02	7.04	0.739	168.03
1.5	0.938	-178.31	2.055	63.25	0.02	4.93	0.73	167.15
2.0	0.918	-166.09	1.777	46.63	0.025	-1.23	0.694	155.54
2.5	0.915	-144.67	1.448	24.9	0.025	-19.64	0.703	137.27
3.0	0.941	-132.34	1.033	10.11	0.022	-27.73	0.76	128.69
3.5	0.957	-134.66	0.803	6.12	0.02	-21.78	0.787	132.92
4.0	0.94	-138.76	0.803	1.66	0.023	-20.57	0.74	136.51

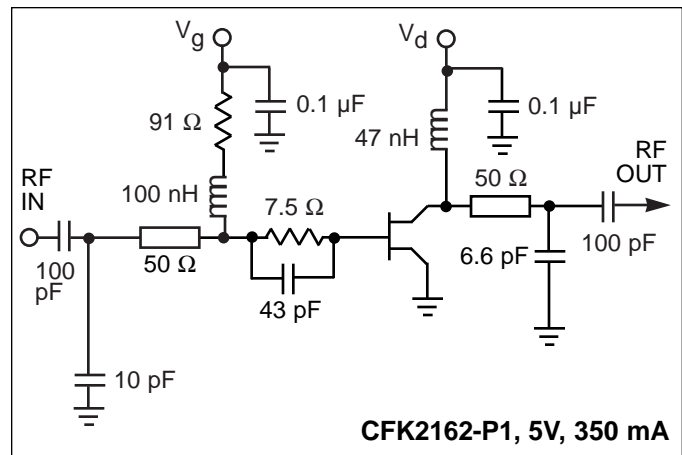
(TA = 25°C, Vds = 5 V, Ids = 1200 mA)

0.6	0.95	-165	5.311	84.94	0.014	13.61	0.747	17.19
0.7	0.951	-169.94	4.491	80.91	0.013	15.25	0.75	170.93
0.8	0.951	-173.53	3.878	77.66	0.014	13.21	0.75	170.03
0.9	0.952	-176.07	3.406	74.74	0.013	13.59	0.75	169.43
1.0	0.951	-177.94	3.044	72.23	0.014	14.39	0.749	168.92
1.1	0.951	-179.34	2.767	70.37	0.014	13.01	0.749	168.72
1.2	0.951	-179.72	2.561	68.34	0.014	14.6	0.745	168.29
1.3	0.951	-178.92	2.391	66.48	0.015	13.62	0.741	167.98
1.4	0.949	-177.92	2.272	64.41	0.015	14.21	0.734	167.24
1.5	0.946	-176.83	2.169	61.99	0.016	14.13	0.728	166.28
2.0	0.929	-165.15	1.88	45.76	0.02	7.43	0.69	154.9
2.5	0.925	-144.23	1.529	24.16	0.022	-7.75	0.698	136.7
3.0	0.947	-131.72	1.09	9.25	0.018	-17.77	0.757	127.79
3.5	0.961	-133.41	0.853	4.59	0.017	-13.03	0.779	131.26
4.0	0.945	-137.83	0.85	0.36	0.021	-8.72	0.73	134.73

(TA = 25°C, Vds = 8 V, Ids = 800 mA)

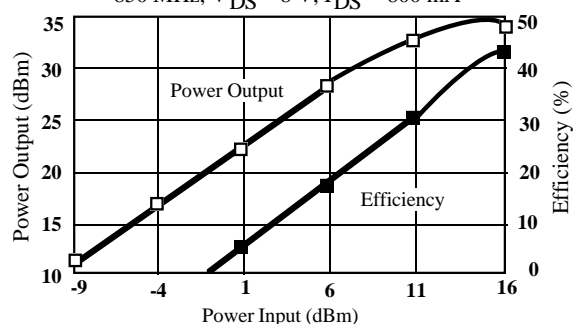
0.6	0.941	-164.65	5.654	83.55	0.015	10.74	0.676	174.61
0.7	0.944	-169.57	4.772	79.47	0.014	10.38	0.682	173.44
0.8	0.946	-172.92	4.131	75.86	0.015	9.99	0.685	172.69
0.9	0.947	-175.57	3.625	72.68	0.014	10.72	0.687	172.32
1.0	0.947	-177.32	3.25	70.11	0.015	8.2	0.688	171.96
1.1	0.946	-178.65	2.944	67.96	0.015	8.47	0.688	172.02
1.2	0.947	-179.63	2.717	65.66	0.015	9.51	0.687	171.82
1.3	0.945	-179.49	2.535	63.48	0.015	7.84	0.684	171.67
1.4	0.944	-178.52	2.397	61.32	0.016	8.5	0.68	171.06
1.5	0.941	-177.34	2.85	58.65	0.016	9.62	0.674	170.41
2.0	0.923	-165.04	12.949	41.52	0.019	-1.07	0.639	159.85
2.5	0.92	-143.82	1.579	19.18	0.02	-12.64	0.653	141.46
3.0	0.944	-131.73	1.116	3.58	0.018	-21.43	0.722	132.33
3.5	0.96	-134.09	0.857	-1.39	0.016	-16.54	0.762	136.36
4.0	0.942	-137.96	0.841	-6.32	0.02	-10.57	0.723	140.71

**RF Match** Data shown in the performance graphs was taken in the test circuits shown at right and on page 3. Layout is important for proper operation. Phase length of input and output 50Ω line varies as a function of exact desired frequency of operation. Output shunt inductor effects output performance. Celeritek recommends the use of a high impedance printed inductor Lambda/4 in length. Please contact the factory for an evaluation board and/or more detailed application support.

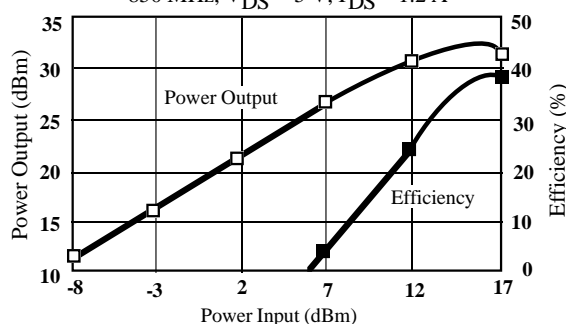


## Typical Performance

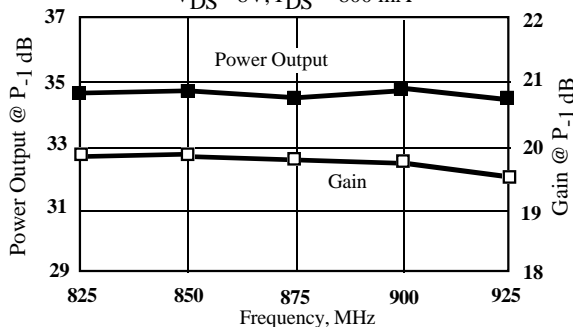
**Power Output & Power Added Efficiency vs Power Input**  
850 MHz,  $V_{DS} = 8\text{ V}$ ,  $I_{DS} = 800\text{ mA}$



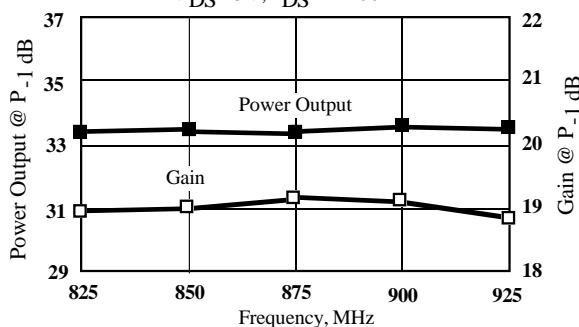
**Power Output & Power Added Efficiency vs Power Input**  
850 MHz,  $V_{DS} = 5\text{ V}$ ,  $I_{DS} = 1.2\text{ A}$



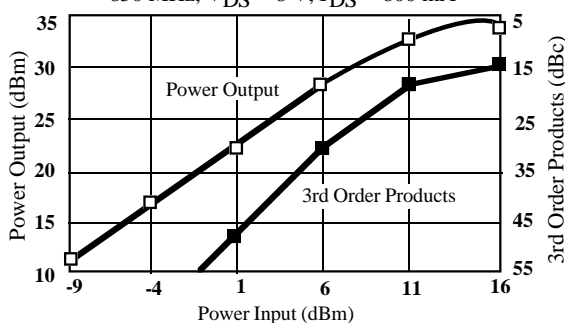
**Power Output and Gain vs Frequency**  
 $V_{DS} = 8\text{ V}$ ,  $I_{DS} = 800\text{ mA}$



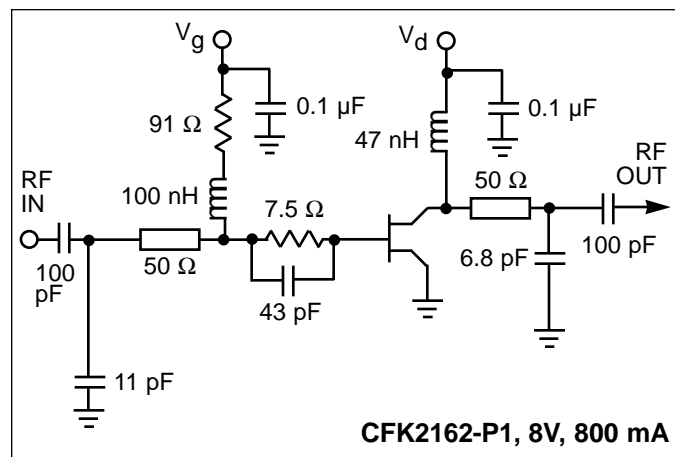
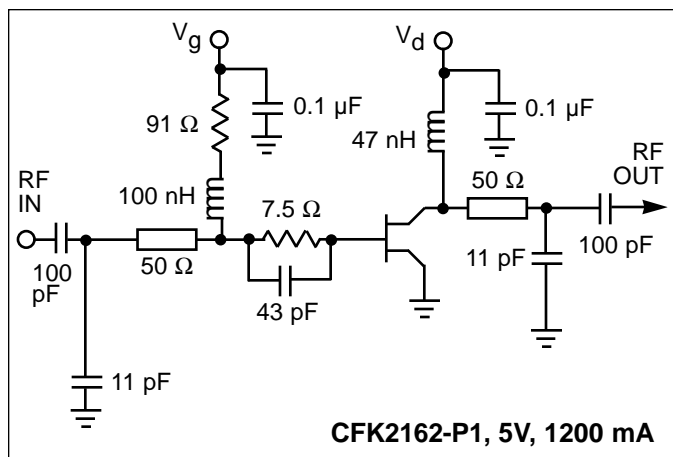
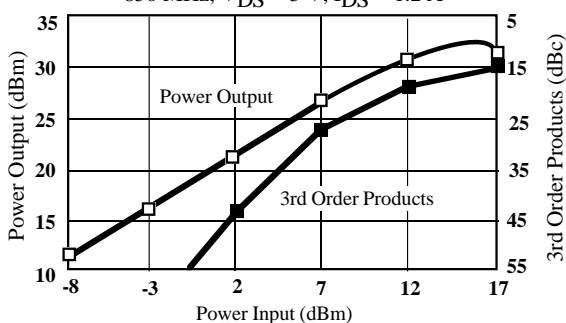
**Power Output and Gain vs Frequency**  
 $V_{DS} = 5\text{ V}$ ,  $I_{DS} = 1200\text{ mA}$



**Power Output & 3rd Order Products vs Power Input**  
850 MHz,  $V_{DS} = 8\text{ V}$ ,  $I_{DS} = 800\text{ mA}$



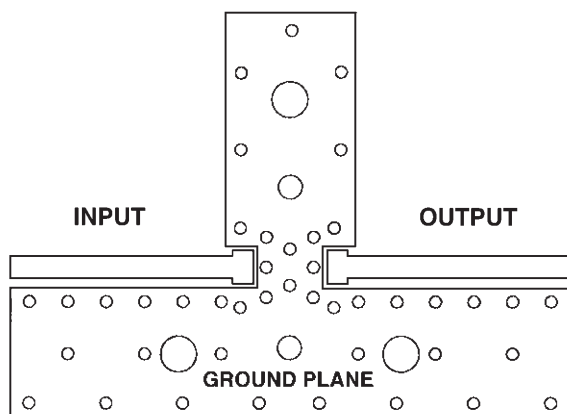
**Power Output & 3rd Order Products vs Power Input**  
850 MHz,  $V_{DS} = 5\text{ V}$ ,  $I_{DS} = 1.2\text{ A}$



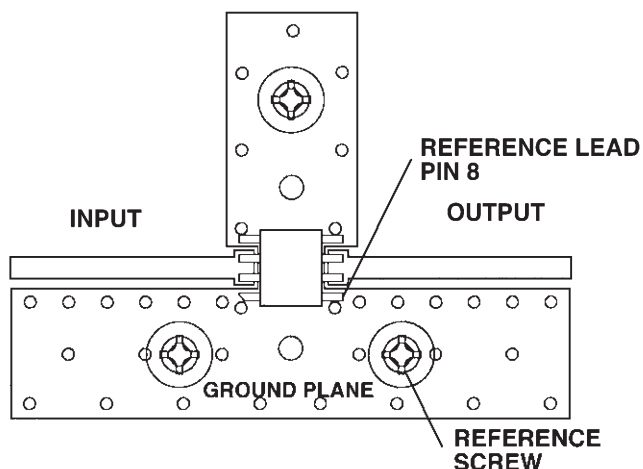
## Thermal Considerations

The data shown was taken on a 31 mil thick FR-4 board with 1 ounce copper on both sides. The board was mounted to a baseplate with 3 screws as shown. The screws bring the top side copper temperature to the same value as the baseplate. The thermal resistance to the indicated reference lead,  $\Theta_{JL}$ , is 10°C/W. The thermal resistance to the reference screw is 12°C/W.

1. Use 1 or 2 ounce copper if possible.
2. Solder all eight leads of the CFK2162-P1 package to the appropriate electrical connection.
3. Solder the copper pad on the backside of the CFK2162-P1 package to the ground plane.
4. Use a large ground pad area with many plated through-holes as shown.
5. If possible, use at least one screw no more than 0.2 inches from the CFK2162-P1 package to provide a low thermal resistance path to the baseplate of the package.



BOARD LAYOUT



THERMAL MOUNTING DIAGRAM

## Ordering Information

The CFK2162-P1 power stage is available in a SO-8 surface mount package. Devices are available in tape and reel. Ordering part numbers are listed.

Part Number for Ordering	Function	Package
CFK2162-P1	800 - 900 MHz Power Stage	SO-8 surface mount power package
CFK2162-P1-000T	800 - 900 MHz Power Stage	SO-8 surface mount power package in tape and reel

Celeritek reserves the right to make changes without further notice to any products herein. Celeritek makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Celeritek assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Celeritek does not convey any license under its patent rights nor the rights of others. Celeritek products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Celeritek product could create a situation where personal injury or death may occur. Should Buyer purchase or use Celeritek products for any such unintended or unauthorized application, Buyer shall indemnify and hold Celeritek and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Celeritek was negligent regarding the design or manufacture of the part. Celeritek is a registered trademark of Celeritek, Inc. Celeritek, Inc. is an Equal Opportunity/Affirmative Action Employer.