

# COic5130A Specifications

*t = 0 to 10, 320Mbs,  
Programmable Reed-Solomon  
Error Correction Encoder and Decoder*

*For information on separate encoder refer to the COic5127A data sheet.*

*For information on separate decoder refer to the COic5128A data sheet.*



## Preliminary Device Specification

### Introduction

The COic5130A contains both a high data rate programmable Reed-Solomon encoder and a separate decoder that will process blocks of up to 255 eight bit symbols to provide corrections (T) of up to 10 errors per code block at data rates up to 320 Mbs. The encoder output code block will contain the unaltered original data symbols followed by the generated parity symbols. The decoder input will contain the received data symbols including errors that may be introduced during transmission. Decoder output will be a completely corrected block or will be marked as non-correctable and the block will be outputted as received without any changes.

The encoder and decoder can be operated independent of each other. Either or both may active at one time. As the devices have separate clocks, the encoder and decoder may operate at different data rates.

The 128-pin mqfp device is manufactured using an 0.5micron CMOS technology by a ISO 9000 certified facility. This part is functionally compatible with the COic5125A, COic5126A, COic5127A and COic5128A and also the AMPEX 1295125-01 and 1295126, but includes features not found in the Ampex devices.



### Encoder Functional Description

The COic5130A contains an encoder that will provide ( N, N-r ) Reed-Solomon forward error correction encoding of blocks of eight bit symbols. The number of parity symbols ( r ) may be from 0 to 20, 0 in Pass Through Mode, and the number of symbols in a block ( N ) from r+1 to 255. At the decoder two parity bytes will be used for each untagged symbol error correction and one parity byte used for a location identified error (erasure) correction. This will provide correction of up to 10 errors ( E ) or up to 20 erasures ( e ) or a combination as long as  $2E + e \leq r$ .

The encoder can encode data at rates from 0 to 40 million symbols per second ( 320 Mbs ) These devices implement the primitive polynomial  $P_x = x^8 + x^4 + x^3 + x^2 + x + 1$  and the generator polynomial

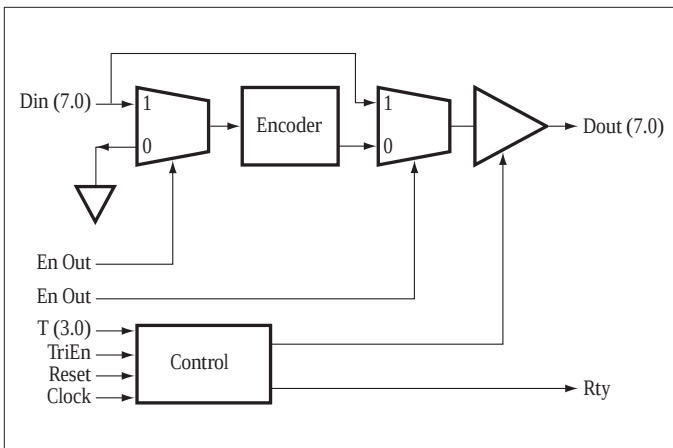
$$G(x) = \prod_{i=0}^{r-1} (x - \alpha^i)$$

which are compatible with SMPTE D-1/D-2, ANSI ID1/ID2, MIL-STD-2179A, DVB, DDS, DAVIC, and DSL standards.

Controls are provided to :

1. tri-state the output data bus
2. disable the input data
3. select the output data source  
(input data bus or parity generator)

### Encoder Functional Block Diagram



### Encoder Features

- Supports 8 bit symbol Reed-Solomon codes ( N, N- r ) with  $0 < r < 20$  and  $r+1 < N < 255$ , N= symbols per block including parity, r = number of parity bytes (NOTE: r is often called 2t)
- Encoding rates from 0 to 320 Mbs with 0 to 40 Mhz symbol clock
- Implements SMPTE D-1/D-2 Digital Video Standards, DVBS Digital Video, ANSI ID-1/ID-2, and Mil -STD-2179A coding polynomials

- Requires only one ( byte ) clock. Input and output data are at one byte per symbol clock for each the encoder and decoder
- Code provides choice of 0 to 20 parity bytes per block
- Provides Pass Through ( no parity ) mode switching on the fly
- Processing latency of only 3 symbol clocks
- Allows code rate changes on the fly
- ISO 9000 certified manufacturing
- 128-pin metal quad flat pack
- Vdd 4.5 to 5.5 volts operation
- - 40 to + 85 degrees C operation

### Encoder Initialization

Before operations the encoder must be initialized to define the number of parity symbols ( r ).

To initialize the binary value of r/2 ( 0 to 10 ) is placed in TA0 - TA3 (TA0 is least significant ) while Reset and EnlnA are held low for four symbol clock periods. Reset is then brought and held high for two symbol clock periods. The inputs on TA0 - TA3 can then be released and the section can start normal operation.

Any TAx pin that is not used must be held low or connected to ground.

### Encoding

To encode a block of symbols the enable in line ( EnlnA ) and enable out line ( EnOutA ) are brought high coincident with the leading edge of first data symbol clock in a new block and remain high until all of the data symbols are clocked into the encoder section and k-3 symbols out onto the Dout bus. There is a processing latency ( delay ) of three clock cycles between the data in ( DinA ) and the data out ( DoutA ). The data ready signal ( RdyA ) is EnlnA delayed by three clock cycles.

At the leading edge of the clockA pulse after the last data symbol has been placed into the encoder, EnlnA and EnOutA are brought low. This will fill the parity generator with zeros. EnlnA and EnOutA are held low for ( r ) clock cycles which inputs zeros into the encoder while outputting the parity code symbols which are appended to the data symbols to form the output data stream. After at least r clock cycles EnlnA and EnOutA are brought high to start the next block.

The output data bus ( DoutA ) may be put into a high impedance state by bringing the TriEnA high. This will not effect the operation of the encoder except to disable the output bus.

When the input enable ( EnlnA ) is low, zeros will be clocked into the encoder input. This can be used to prevent spurious data from being encoded.

The number of data symbols (  $k$  ) of succeeding blocks can be changed as desired at any time. This will change the code rate for the blocks, but to change the correction power (  $r$  ) the section must be re-initialized. This can also be done at any time, but any blocks in process at that time will be lost.

### Encoder Duplex Operation

Half Duplex operation can be achieved on a single bi-directional channel at a maximum transmission rate equal to one half of the symbol clock. Allowing for transmission and circuit switching delays, data can be switched from the unit encoder to the decoder on any symbol boundary. External data switching and control circuits will be required to control data flow and device enables.

Full duplex at full clock rate can be implemented but requires two data carriers or echo cancellation.

### Encoder Pass Through Mode

Any number of symbols can be passed through the encoder without any encoding if the Enable In (EnInA) is held high and enable out (EnOutA) is held low while the symbols are clocked into the section. This will allow the maximum data transfer rate, but will not provide any error correction ( $t=0$ ). To end pass through mode operation EnInA must be brought high, which will start the encoding process. This must be at the beginning of a block for correct operations. Pass through mode may be invoked at any time but any blocks in process when this mode is started will not be encoded properly and will not be able to be decoded.

### Decoder Functional Description

COic5130A includes a high data rate programmable Forward Error Correction devices that can decode Reed-Solomon code blocks of up to 255 eight bit data symbols. It provides corrections of up to 10 symbol errors per block at data rates up to 320 Mbs. Blocks with more errors than are correctable are so flagged with data outputted as received ( no corrections ). Note: blocks must contain at least 8 parity symbols, except when operating in bypass mode.

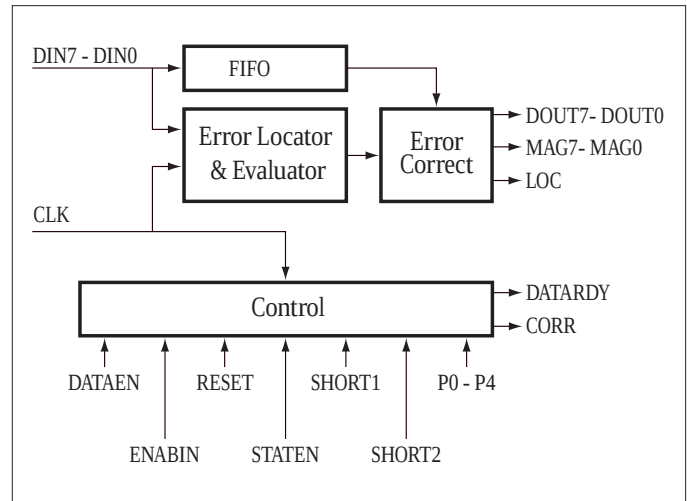
The decoder input code block will contain the transmitted data and parity symbols, including corruption by channel noise ( errors ). A symbol error is corrected the same regardless of the number of incorrect bits in the symbol and decoding time is the same regardless of the number of errors in a block. Decoder output data will be corrected data plus corrected parity or block error data. Error location and correction data is also provided. No clock other than the data clock is required. Input and output are one byte per clock cycle.

COic5130A uses the primitive polynomial  $P_x = x^8 + x^4 + x^3 + x^2 + x + 1$  which complies with SMPTE D-1 / D-2 Digital Video Standards, DVB, DBS, DAVIC, DSL, ANSI ID-1 / ID-2, and MIL STD 2179A. The COic5130A is functionally compatible with the COic5127 encoder and

COic5128 decoder as well as the T=5 AMPEX 1295126-01. It includes features not found in that device, and using  $r = 20$  corrects up to 10 errors per block.

$$\text{Devices use the generator polynomial : } G(x) = \prod_{i=0}^{r-1} (x - \mu^i)$$

### Decoder Functional Block Diagram



### Decoder Features

- Supports 8 bit symbol Reed Solomon codes (  $N, N-r$  ) with  $0 < r < 20$  and  $N < 255$ ,  $N$ = symbols per block including parity,  $r$  = number of parity symbols (Note:  $r$  is often called  $2t$ )
- Corrects up to 10 errors per block
- COic5128A has 3 selectable latencies:
  - Default ( Ampex / AHA ) =  $2N + 5r + 33$  clock cycles with a minimum block length of  $5r + 15$
  - Latency 1 =  $2N + 2r + 13$  clock cycles with a minimum block length of  $2r + 13$
  - Latency 2 =  $3N/2 + 3r/2 + 15$  clock cycles with a minimum block length of  $3r/2 + 15$
- Contains complete decoder device. No external memory or control required after initialization
- Data rates up to 40 MBS ( 320 Mbs ) with 0 to 40 Mhz symbol clock
- End of Block flag eases applications
- Input and output data are at the identical rate and operates on data clock only
- Provides Pass Through Mode ( no correction ) switching on-the-fly
- Latency is constant regardless of error patterns
- Allows code rate change ( less data, same parity ) on-the-fly

- Provides complete error location and correction information
- Flags uncorrectable blocks
- 4.5 to 5.5 volt operation
- -40 to + 85 degrees C operation range (extended range available)
- ISO 9000 certified manufacturing

### Decoder Functional Description

The device contains a decoder that will provide (N,N-r) Reed-Solomon forward error correction decoding of blocks of eight bit symbols. The number of parity symbols (r) may be from 8 to 20, 0 in Pass Through Mode, and the number of symbols in a block (N) up to 255. Two parity bytes will be used for each symbol error correction. This device will provide correction of up to 10 symbol errors (E) as long as  $2E \leq r$ . It will provide the number of corrections made in each block. Symbol errors are processed the same regardless of the number of incorrect bits in the symbol. Processing latency is the same regardless of the number of errors, including zero, in a block. The device can decode at data rates from 0 to 40 million symbols per second (320 Mbs) and two or more devices can be used together (see Application Brief for Reed-Solomon FEC) to process data at higher rates.

### Encoder Initialization

Before operations the device must be initialized to define N, r, P (the number of parity symbols that can be used (decoded) before a block is determined uncorrectable) and to set the block error information report (status) output. A two step process is used.

**Step One:** Set the level of OptLn to the desired level and maintain throughout all operations. While the binary value of P is held on the P control bus, Reset and DataEn are held low for at least four symbol clock cycles and then Reset is brought high and held high for at least two more symbol clock cycles. At the same time the StatEn line is held high if the decoder block error information bytes (status) output are desired and low if not. Note that the decoder will output corrected parity bytes in the space formerly used by parity which are not used by block error information (status) bytes. Symbols of any value can be used for this step.

**Step Two:** With Reset high a normal block processing procedure is used to set up values of N, r, and k (N-r). The Enabln is brought high with the first data symbol and held high throughout the decoding session. Also at the beginning of the block DataEn is brought high at the leading edge of the first symbol clock pulse and held high while the data symbols are being clocked into the device, that is N-r symbol clock pulses. DataEn is brought low with the first parity symbol and held low for r symbol clock cycles while the parity symbols are clocked in. DataEn, going high again marks the end of parity and the start of the next block. Reset will remain high throughout step 2 and normal use until a new reset cycle is desired. This step will set up the device timing for all following blocks until the device is reinitialized or an alternate length block with fewer data symbols (see Alternate Block Length) is used. A

regular data block may be used for this step but to prevent possible loss of data a block using dummy symbols of any value is recommended.

### Selecting the value of P

The value of P determines the number of parity bytes that can be used (decoded) before a block is flagged as uncorrectable. The decoder will always use all of the parity bytes available to correct a block regardless of the value of P, which is usually set equal to r (the number of parity bytes) but P can be less or more than r.

1. If P equals r the device will properly correct all blocks where  $2E \leq r$  and mark all other blocks as uncorrectable. This option is almost always used.
2. If P is less than r the device will use all of the parity bytes to correct the block but will mark corrected blocks as uncorrected if  $P < 2E < r$ . In this case the error status bytes must be checked to determine if correction was actually achieved. This feature can be used to detect more errors than can be corrected, but must be used with care.
3. If P is more than r normal correction will take place but the device will not provide uncorrectable block flags and may pass on to the output unflagged uncorrected data blocks. THIS SETTING HAS NO VALUE AND SHOULD NOT BE USED.
4. If P is more than 20 the decoder will pass all information directly to the data output without any corrections. THIS SETTING HAS NO VALUE AND SHOULD NOT BE USED.

The value of P may be changed at any time, but any blocks in process at the time of the change may not be properly flagged if uncorrectable.

### Minimum Block Lengths

Minimum block lengths and latency are a function of the number of parity bytes used in a code. OptLn must be set at the start of initialization and held at the correct level throughout operations. The device must repeat Initialization if OptLn is to be changed

The COic5130A allows three different equations to determine the minimum block lengths. When pin 16 is low and pin 9 LOW or NC the default equation is Minimum Block Length =  $5r + 15$  bytes. When pin 9 is held at High and pin 16 is low level Latency1 is invoked and the minimum block length equation is changed to  $(2r + 13)$  bytes. If pin 16 is high Latency 2 is invoked and the minimum block length is  $3r/2 + 15$  regardless of the level of pin 9.

### Decoder Latency

The time that is required for the data to flow through the device is called latency and is measured in symbol clock cycles. The devices can be operated with any of three latencies, under the control of OpLan1, pin 9 and OpLan2, pin 16. Latencies are a function of the block length and correction level, but unaffected by error patterns. The default latency (pin 9 and 16 both low) is equal to  $2N + 5r + 33$  symbol clock cycles,

which is compatible with the Ampex 1295126-01 device. When pin 9 is held to High level and pin 16 is low Latency 1 is invoked and the equation is changed to  $2N + 2r + 13$  symbol clock cycles. Latency 2 is invoked if pin 16 is high regardless of the level of pin 9 and the equation is  $3n/2 + 3r/2 + 15$ . Effects of optional shorter latency and minimum code length ( OptLn ) : The combination of the shorter code and latency can result in considerable increase in effective data transfer. In most new designs the Latency1 or Latency 2 option will provide the best operations.

Example: If a desired code is ( 64,48 )  $r=16$ , the default minimum block length (  $5r + 33$  ) is 95 bytes which requires 31 " filler " bytes to be inserted in each block., a loss of over 33 % of the channel effectiveness.

The latency (  $2N+5r+33$  ) is 313 clock cycles. With OptLn2 invoked the minimum block length is 39 bytes , which does not require any filler bytes so there is no loss of channel effectiveness. The latency is 135 clock cycles.

### Decoding

After the COic5130A is initialized it can begin decoding incoming blocks. It is a good idea, but not absolutely necessary, to pass at least as many dummy symbols as the latency through the device before actual data is used in order to clear out any spurious information in the unit. Although it is not recommended, block of data can be used to initialize the device can be made up of valid data, if step one has been completed.

To decode, the Enabln is brought high and held high throughout the decoding secession. At the beginning of a code block DataEn is brought high at the leading edge of the first symbol clock pulse and held high while the data symbols are being clocked into the device, that is N-r symbol clock pluses. DataEn is brought low with the first parity symbol and held low for r symbol clock cycles while the parity symbols are clocked into the decoder. DataEn,s going high again marks the end of parity and the start of the next block.

The first data symbol is placed on the Dout bus, the DatRdy line will go high and the unit will begin to output data symbols when the number of symbol clocks required for processing latency are complete. At the end of N-r symbols the DatRdy line goes low and parity symbols are outputted

### Correct

Correct pin --- goes high as the block starts being outputted if the block contains corrected symbols or low if the block is outputted as it was received due to either 0 or more than r errors in the block.

### UnCorr

If the block cannot be corrected UnCorr, pin --- will go to the high level. This will occur as the block being processed starts to be outputted.

### StatEN

If StatEn has been set high the first two parity bytes will be replaced with error information. Byte 1 will show FXXXXXXX and Byte 2 will show FXXTTTTT where:

F = block Not Correctable if high, block was Corrected if low.

EEEE = Erasure count will be 0.

TTTTT = Total number of corrections made in the block.

If the block was not correctable ( F bit is high ) E and T values will be meaningless. If StatEn is low all of the corrected parity symbols will be clocked out of the decoder.

### Decoder Error Information Output

In order to help optimize the application ECC function, detailed error information for each block is also available while the decoder data output is in process. It is not necessary to use this information for proper operation the part.

If the symbol being outputted from the decoder has been corrected ErLoc (pin 24) will go high. The pattern used to correct that symbol will appear on CMag 0 -CMag7 pins at the same time. Note that the error is actually the logical inverse of the correction. (The user must provide external storage and processing of this information as the COic5130 does not store these error location or correction information outputs. If the decoder detects more than  $r/2$  errors ErLoc will remain low throughout the block as no changes will be made. The UnCorr line or Status bytes must be monitored to flag this condition.

### Decoder Pass Through Mode ( $r=0$ )

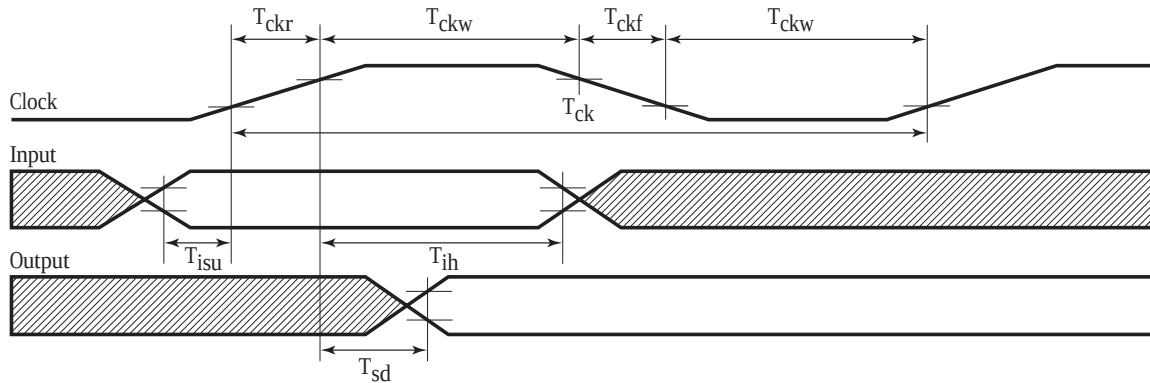
Any number of symbols can be passed through the decoder without any changes (corrections) if the Enable In ( Enabln ) is held low while symbols are clocked into the device. The input symbols, data and parity if any, will be passed unchanged to the output ( Dout ) after the number of symbol clocks needed for processing latency. In this mode there will normally not be any parity symbols. That will allow transfer of data symbols at the maximum rate, but will not provide any error correction ( $t=0$ ).

To end Pass Through Mode operation Enabln must be brought high, which will start the decoding process. This must be at the beginning of a block for correct operations. Pass Through Mode may be invoked at any time but any blocks in process when this mode is started will not be decoded properly.

### EnOBk

When the last byte of a block is outputted EnOBK pin 22 will go to the high level for one clock period.

### Encoder Output Timing

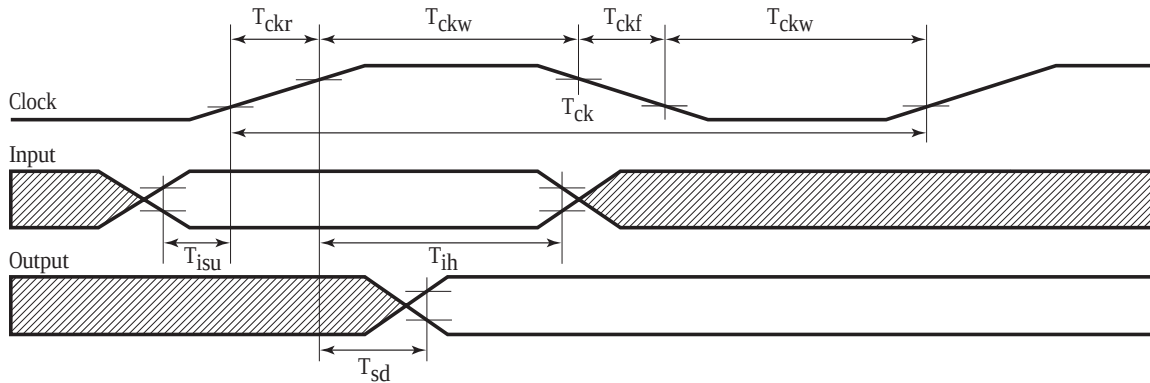


### Encoder Initialization

Before operation the encoder must be initialized to define the number of parity symbols ( $r$ ).

To initialize the binary value of  $r/2$ , (0 to 10) is placed in T0 – T3 (T0 is least significant) while RESET and ENIN are held low for four symbol clock periods. RESET is then brought high for two symbol clock periods. The inputs on T0 – T3 can then be released and the encoder can start normal operation. Any TX pin that is not used must be held low or connected to ground.

### Decoder Output Timing



### Decoder Initialization

Certain architectural and mathematical properties of this device are not hard wired and must be set up during the initialization control sequence. These properties include:

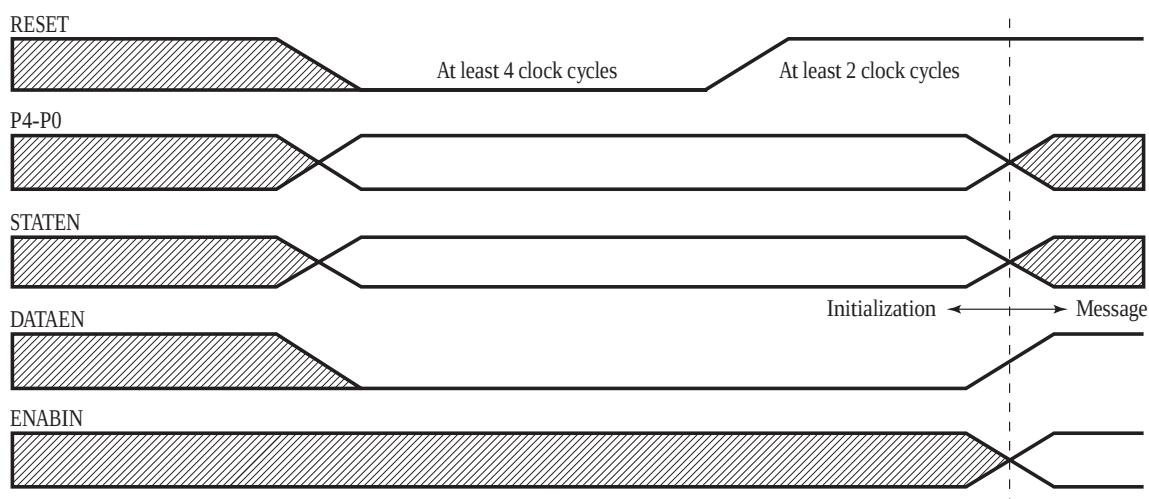
1. The overall message block length ( $N$ )
2. The number of data bytes ( $K$ )
3. The total number of check bytes ( $R$ )
4. The number of check bytes allocated for correction only ( $P$ )
5. Whether the first check byte output positions are used for status bytes or check bytes (STATEN)
6. Whether to use AMPEX compatible, non-compatible, or short timing (SHORT1, SHORT2)



These properties must be initialized before normal operation can begin. There are two distinct phases of the initialization process. In phase one, the values of P, STATEN and SHORT1 and SHORT2 are initialized. In phase two, the first message block through the device is used to set the values of N, K and R.

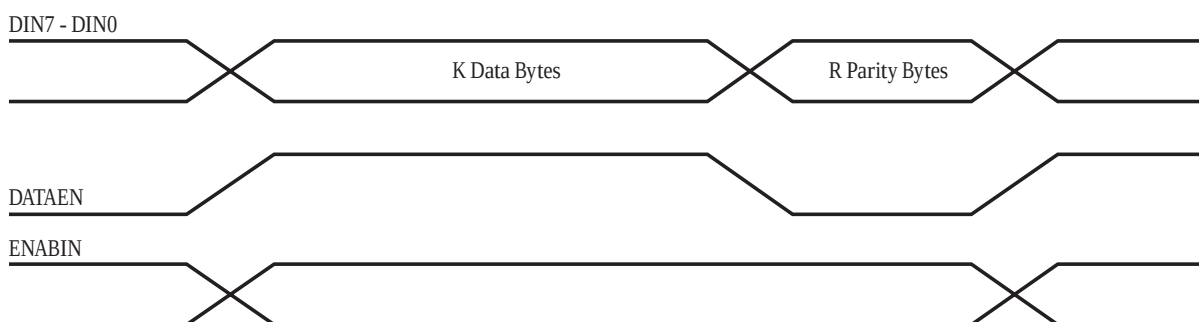
The phase one sequence consists of at least 4 clock cycles in which RESET is held LOW followed by at least 2 clock cycles during which RESET is held HIGH. RESET must then remain HIGH for all subsequent operations or else an unwanted initialization sequence will ensue. The desired values of STATEN and P4 - P0 must be maintained during the first phase of initialization. The desired value of SHORT1 and SHORT2 must be maintained during all the phases of operation of the device. DATAEN must be held LOW during the entire six clock sequence or unintended processing of spurious messages may occur.

#### Decoder Initialization Control Sequence Timing



The rising edge of DATAEN at the end of the phase one initialization sequence marks the beginning of the first message block, which is the beginning of phase two of the initialization process. DATAEN has the role of initializing the parameters of N, K and R. DATAEN has a different function on all subsequent blocks until an initialization sequence is begun once again. As the first message block passes through the device, DATAEN is held HIGH for K clock cycles and then LOW for R clock cycles. DATAEN going high again marks the first byte of the second block and implies the end of the phase two initialization sequence. DATAEN has thus defined R, K and N for all subsequent blocks until another initialization sequence is performed.

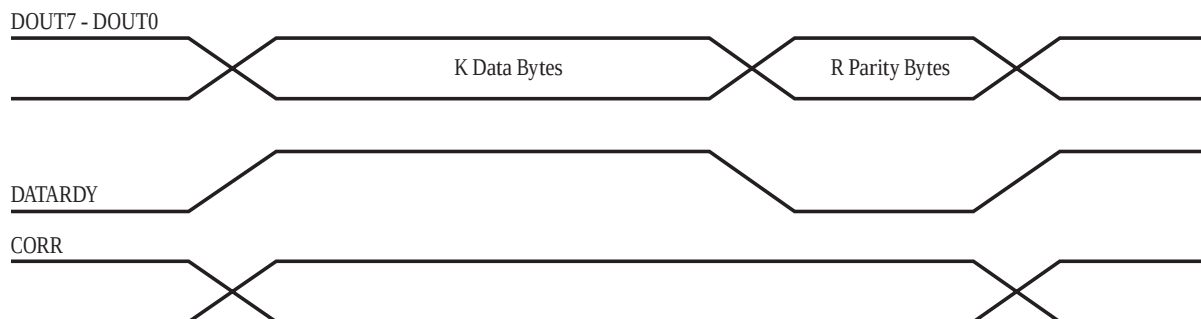
#### Decoder Message Input Timing



## Message Decoding

During message decoding the device clocks in the encoded message block from the DIN7 - DIN0 input bus on the rising edge of CLK. The device then computes polynomials for this data using a high performance Reed-Solomon coding algorithm, and then proceeds to use the calculated polynomials to correct any errors, if possible. These polynomials are a series of complex equations that will indicate not only the position of incorrect bytes but will also produce the necessary information to correct them. The timing of the decoding operation is defined

### Decoder Message Output Timing



The action taken by the decoder with respect to a given message block is determined in all cases by the quantity of errors received. The device reports its action via the CORR output pin. If  $P = R$ , a HIGH output on the CORR pin indicates that the message block being output is correct. A LOW output indicates that a correction was not performed because there were too many errors or no errors. In situations where  $P$  has been chosen to be not equal to  $R$ , the meaning of the UNCORR pin is that more than  $P/2$  errors have occurred.

### Decoder Optional Status Bytes

The optional status bytes, that may be output at the end of the message block, indicate the number of errors encountered and may be used to determine the exact meaning of the CORR output when  $P \neq R$ . The first status byte has all of its bits set LOW except bit 7, which is the CA (correction attempted) flag. The CA flag goes LOW when  $E \leq R/2$  (the message block was successfully decoded). Therefore, anytime CA is HIGH, the message block should be retransmitted since there were probably too many errors to reliably correct. Also, if  $P = R$  then CA will always be LOW when the CORR output pin is HIGH and HIGH when CORR is LOW.

In the second status byte, bits 4 through 0 are a binary count of the number of errors encountered. Bit 4 is most significant. The remaining bits are always LOW.



## Pinout

Table 1: Device Pinout

| Pin# | Signal Name     | Encoder / Decoder | Description                                                                                                                                                                                       | Signal Type |
|------|-----------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 1    | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 2    | DEC_MAG0        | Decoder           | Error Magnitude 0. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | TTL Output  |
| 3    | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 4    | DEC_MAG1        | Decoder           | Error Magnitude 1. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | TTL Output  |
| 5    | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 6    | DEC_MAG2        | Decoder           | Error Magnitude 2. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | TTL Output  |
| 7    | DEC_DOUT6       | Decoder           | Data output bit 6. Bit 7 is MSB.                                                                                                                                                                  | Output      |
| 8    | V <sub>dd</sub> | N/A               | +5 Volt Power                                                                                                                                                                                     | Power       |
| 9    | DEC_DOUT5       | Decoder           | Data output bit 5. Bit 7 is MSB.                                                                                                                                                                  | Output      |
| 10   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 11   | GND             | N/A               | Ground                                                                                                                                                                                            | Power       |
| 12   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 13   | DEC_DOUT4       | Decoder           | Data output bit 4. Bit 7 is MSB.                                                                                                                                                                  | Output      |
| 14   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 15   | DEC_DOUT3       | Decoder           | Data output bit 3. Bit 7 is MSB.                                                                                                                                                                  | Output      |
| 16   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 17   | V <sub>dd</sub> | N/A               | +5 Volt Power                                                                                                                                                                                     | Power       |
| 18   | DEC_DOUT2       | Decoder           | Data output bit 2. Bit 7 is MSB.                                                                                                                                                                  | Output      |
| 19   | DEC_DOUT1       | Decoder           | Data output bit 1. Bit 7 is MSB.                                                                                                                                                                  | Output      |
| 20   | GND             | N/A               | Ground                                                                                                                                                                                            | Power       |
| 21   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |

Table 1: Device Pinout, continued

| Pin# | Signal Name     | Encoder / Decoder | Description                                                                                                                                                                                       | Signal Type |
|------|-----------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 22   | DEC_DOUT0       | Decoder           | Data output bit 0. Bit 7 is MSB.                                                                                                                                                                  | Output      |
| 23   | GND             | N/A               | Ground                                                                                                                                                                                            | Power       |
| 24   | DEC_DATARDY     | Decoder           | Data Ready. Assertive HIGH. This output is held HIGH for data bytes and low check bytes.                                                                                                          | Output      |
| 25   | DEC_MAG3        | Decoder           | Error Magnitude 3. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | TTL Output  |
| 26   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 27   | DEC_MAG4        | Decoder           | Error Magnitude 4. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | TTL Output  |
| 28   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 29   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 30   | DEC_MAG5        | Decoder           | Error Magnitude 5. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | TTL Output  |
| 31   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 32   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 33   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 34   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 35   | V <sub>dd</sub> | N/A               | +5 Volt Power                                                                                                                                                                                     | Power       |
| 36   | ENC_TEST_SE     | Encoder           | Foundry Test Pin - Do not Use                                                                                                                                                                     |             |
| 37   | GND             | N/A               | Ground                                                                                                                                                                                            |             |
| 38   | GND             | N/A               | Ground                                                                                                                                                                                            |             |
| 39   | DEC_MAG6        | Decoder           | Error Magnitude 6. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | TTL Output  |
| 40   | DEC_STATEN      | Decoder           | Status Enable. Assertive HIGH. If this signal is HIGH during reset then the decoder will be programmed to output two status bytes with each message block.                                        | Input       |

Table 1: Device Pinout, continued

| Pin# | Signal Name     | Encoder / Decoder | Description                                                                                                                                                                                       | Signal Type |
|------|-----------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 41   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 42   | DEC_MAG7        | Decoder           | Error Magnitude 7. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | TTL Output  |
| 43   | V <sub>dd</sub> | N/A               | +5 Volt Power                                                                                                                                                                                     | Power       |
| 44   | DEC_DIN7        | Decoder           | Decoder symbol input bit 7. Bit 7 is MSB.                                                                                                                                                         | Input       |
| 45   | ENC_TEST_SI     | Encoder           | Foundry Test Pin - Do not Use                                                                                                                                                                     |             |
| 46   | DEC_DIN6        | Decoder           | Decoder symbol input bit 6. Bit 7 is MSB.                                                                                                                                                         | Input       |
| 47   | GND             | N/A               | Ground                                                                                                                                                                                            | Power       |
| 48   | ENC_DOUT6       | Encoder           | Encoder data output bit 6                                                                                                                                                                         | Tristate    |
| 49   | V <sub>dd</sub> | N/A               | +5 Volt Power                                                                                                                                                                                     | Power       |
| 50   | ENC_DIN6        | Encoder           | Encoder data input bit 6                                                                                                                                                                          | Input       |
| 51   | DEC_TEST_SI     | Decoder           | Foundry Test Pin - Do not Use                                                                                                                                                                     |             |
| 52   | V <sub>dd</sub> | N/A               | +5 Volt Power                                                                                                                                                                                     | Power       |
| 53   | DEC_DIN5        | Decoder           | Decoder symbol input bit 5. Bit 7 is MSB.                                                                                                                                                         | Input       |
| 54   | ENC_DIN7        | Decoder           | Encoder data input bit 7                                                                                                                                                                          | Input       |
| 55   | GND             | N/A               | Ground                                                                                                                                                                                            | Power       |
| 56   | ENC_DOUT7       | Encoder           | Encoder data output bit 7                                                                                                                                                                         | Tristate    |
| 57   | V <sub>dd</sub> | N/A               | +5 Volt Power                                                                                                                                                                                     | Power       |
| 58   | GND             | N/A               | Ground                                                                                                                                                                                            |             |
| 59   | DEC_DIN4        | Decoder           | Decoder symbol input bit 4. Bit 7 is MSB.                                                                                                                                                         | Input       |
| 60   | ENC_DOUT4       | Encoder           | Encoder data output bit 4                                                                                                                                                                         | Tristate    |
| 61   | DEC_DIN3        | Decoder           | Decoder symbol input bit 3. Bit 7 is MSB.                                                                                                                                                         | Input       |
| 62   | NC              | N/A               | No Connection                                                                                                                                                                                     |             |
| 63   | ENC_DIN4        | Encoder           | Encoder data input bit 4                                                                                                                                                                          | Input       |

Table 1: Device Pinout, continued

| Pin# | Signal Name     | Encoder / Decoder | Description                                                                                                                                                                                                                                           | Signal Type |
|------|-----------------|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 64   | NC              | N/A               | No Connection                                                                                                                                                                                                                                         |             |
| 65   | DEC_UNCORR      | Decoder           | Decoder uncorrectable block. Assertive HIGH. Indicates message block contains uncorrectable errors.                                                                                                                                                   | Output      |
| 66   | V <sub>dd</sub> | N/A               | +5 Volt Power                                                                                                                                                                                                                                         | Power       |
| 67   | ENC_DIN5        | Encoder           | Encoder data input bit 5                                                                                                                                                                                                                              | Input       |
| 68   | ENC_DOUT5       | Encoder           | Encoder data output bit 5                                                                                                                                                                                                                             | Tristate    |
| 69   | GND             | N/A               | Ground                                                                                                                                                                                                                                                | Power       |
| 70   | DEC_DIN2        | Decoder           | Decoder symbol input bit 2. Bit 7 is MSB.                                                                                                                                                                                                             | Input       |
| 71   | ENC_RDY         | Encoder           | Indicates data symbols are on the encoder ENC_DOUT bus                                                                                                                                                                                                | Output      |
| 72   | DEC_DIN1        | Decoder           | Decoder symbol input bit 1. Bit 7 is MSB.                                                                                                                                                                                                             | Input       |
| 73   | ENC_ENOUT       | Encoder           | Enables encoder DIN bus onto the DOUT bus                                                                                                                                                                                                             | Input       |
| 74   | V <sub>dd</sub> | N/A               | +5 Volt                                                                                                                                                                                                                                               | Power       |
| 75   | ENC_ENIN        | Encoder           | Enable encoder DIN bus into the parity generator                                                                                                                                                                                                      | Input       |
| 76   | DEC_DIN0        | Decoder           | Decoder symbol input bit 0. Bit 7 is MSB.                                                                                                                                                                                                             | Input       |
| 77   | ENC_RESET       | Encoder           | Initializes encoder into a know state (high)                                                                                                                                                                                                          | Input       |
| 78   | GND             | N/A               | Ground                                                                                                                                                                                                                                                | Power       |
| 79   | ENC_TRIEN       | Encoder           | Tri-states the encoder ENC_DOUT bus drivers when HIGH                                                                                                                                                                                                 | Input       |
| 80   | DEC_DATEN       | Decoder           | Decoder data enable. Assertive HIGH. This input is used to signal the difference between data bytes and check bytes.                                                                                                                                  | Input       |
| 81   | DEC_ENABIN      | Decoder           | "Decoder enable data correction. Assertive HIGH. When this input is asserted, the device performs corrections on the message block. When CEN is low, the device does not perform corrections but continues to report status is initialized to do so." | Input       |
| 82   | ENC_CLOCK       | Encoder           | Encoder master and symbol clock.                                                                                                                                                                                                                      | Input       |
| 83   | ENC_TA2         | Encoder           | Bit 2 of the encoder T select bus                                                                                                                                                                                                                     | Input       |
| 84   | V <sub>dd</sub> | N/A               | +5 Volt Power                                                                                                                                                                                                                                         | Power       |
| 85   | ENC_TA1         | Encoder           | Bit 1 of the encoder T select bus                                                                                                                                                                                                                     | Input       |

Table 1: Device Pinout, continued

| Pin# | Signal Name | Encoder / Decoder | Description                                                                                                                                                                                                                                                    | Signal Type |
|------|-------------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 86   | DEC_P3      | Decoder           | Decoder parity input bit 3. This determines the value of (P) which is the maximum of check bytes that the device will use in correction before flagging the block as uncorrectable. Normally set to the # of check bytes (R). P4 is the most significant bits. | Input       |
| 87   | ENC_TA0     | Encoder           | Bit 0 of the encoder T select bus                                                                                                                                                                                                                              | Input       |
| 88   | DEC_P2      | Decoder           | Decoder parity input bit 2. This determines the value of (P) which is the maximum of check bytes that the device will use in correction before flagging the block as uncorrectable. Normally set to the # of check bytes (R). P4 is the most significant bits. | Input       |
| 89   | Vdd         | N/A               | +5 Volt Power                                                                                                                                                                                                                                                  | Power       |
| 90   | DEC_P1      | Decoder           | Decoder parity input bit 1. This determines the value of (P) which is the maximum of check bytes that the device will use in correction before flagging the block as uncorrectable. Normally set to the # of check bytes (R). P4 is the most significant bits. | Input       |
| 91   | ENC_DIN3    | Encoder           | Encoder data input bit 3                                                                                                                                                                                                                                       | Input       |
| 92   | DEC_P4      | Decoder           | Decoder parity input bit 4. This determines the value of (P) which is the maximum of check bytes that the device will use in correction before flagging the block as uncorrectable. Normally set to the # of check bytes (R). P4 is the most significant bits. | Input       |
| 93   | ENC_DOUT3   | Encoder           | Encoder data output bit 3                                                                                                                                                                                                                                      | Tristate    |
| 94   | ENC_TA3     | Encoder           | Bit 3 of the encoder T select bus                                                                                                                                                                                                                              | Input       |
| 95   | DEC_SHORT2  | Decoder           | Decoder latency select 2. Selects latency according to Table 2: Latency and Minimum Block Size Selection.                                                                                                                                                      | Input       |
| 96   | NC          | N/A               | No Connection                                                                                                                                                                                                                                                  |             |
| 97   | ENC_DOUT2   | Encoder           | Encoder data output bit 2                                                                                                                                                                                                                                      | Tristate    |
| 98   | NC          | N/A               | No Connection                                                                                                                                                                                                                                                  |             |
| 99   | ENC_DIN2    | Encoder           | Encoder data input bit 2                                                                                                                                                                                                                                       | Input       |
| 100  | NC          | N/A               | No Connection                                                                                                                                                                                                                                                  |             |
| 101  | Vdd         | N/A               | +5 Volt Power                                                                                                                                                                                                                                                  | Power       |
| 102  | DEC_RESET   | Decoder           | Decoder system reset. Assertive LOW. Reset timing is critical to the initialization of the device                                                                                                                                                              | Input       |
| 103  | ENC_DIN1    | Encoder           | Encoder data input bit 1                                                                                                                                                                                                                                       | Input       |
| 104  | Vdd         | N/A               | +5 Volt Power                                                                                                                                                                                                                                                  | Power       |
| 105  | ENC_DOUT1   | Encoder           | Encoder data output bit 1                                                                                                                                                                                                                                      | Tristate    |

Table 1: Device Pinout, continued

| Pin# | Signal Name     | Encoder / Decoder | Description                                                                                                                             | Signal Type |
|------|-----------------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 106  | GND             | N/A               | Ground                                                                                                                                  | Power       |
| 107  | NC              | N/A               | No Connection                                                                                                                           |             |
| 108  | DEC_TEST_SO     | Decoder           | Foundry Test Pin - Do not Use                                                                                                           |             |
| 109  | GND             | N/A               | Ground                                                                                                                                  | Power       |
| 110  | DEC_SHORT1      | Decoder           | Decoder latency select 1. Selects latency according to Table 2: Latency and Minimum Block Size Selection.                               | Input       |
| 111  | ENC_DOUT0       | Encoder           | Encoder data output bit 0                                                                                                               | Tristate    |
| 112  | GND             | N/A               | Ground                                                                                                                                  | Power       |
| 113  | ENC_DIN0        | Encoder           | Encoder data input bit 0                                                                                                                | Input       |
| 114  | V <sub>dd</sub> | N/A               | +5 Volt Power                                                                                                                           | Power       |
| 115  | DEC_TEST_SE     | Decoder           | Foundry Test Pin - Do not Use                                                                                                           |             |
| 116  | ENC_TEST_SO     | Encoder           | Foundry Test Pin - Do not Use                                                                                                           |             |
| 117  | DEC_CLOCK       | Decoder           | Decoder master clock. All inputs and outputs are synchronized by the rising edge of DEC_CLOCK.                                          | Input       |
| 118  | GND             | N/A               | Ground                                                                                                                                  | Power       |
| 119  | DEC_CORR        | Decoder           | Decoder message block corrected. Assertive HIGH. Indicates that errors have been found and corrected in message block.                  | Output      |
| 120  | DEC_EOB         | Decoder           | Decoder End of Block. 1/0 = End/Not end of block.                                                                                       | Output      |
| 121  | NC              | N/A               | No Connection                                                                                                                           |             |
| 122  | DEC_DOUT7       | Decoder           | Data output bit 7. Bit 7 is MSB.                                                                                                        | Output      |
| 123  | DEC_LOC         | Decoder           | Decoder Error Location. Assertive HIGH. This output goes HIGH if the current symbol outout on Q7-Q0 has had a correction applied to it. | Output      |
| 124  | V <sub>dd</sub> | N/A               | +5 Volt Power                                                                                                                           | Power       |
| 125  | NC              | N/A               | No Connection                                                                                                                           |             |
| 126  | GND             | N/A               | Ground                                                                                                                                  | Power       |
| 127  | NC              | N/A               | No Connection                                                                                                                           |             |
| 128  | V <sub>dd</sub> | N/A               | +5 Volt Power                                                                                                                           | Power       |



## Pinout

## Decoder Input Pins

| Pin# | Signal   | Description                               | Signal Type |
|------|----------|-------------------------------------------|-------------|
| 76   | DEC_DIN0 | Decoder symbol input bit 0. Bit 7 is MSB. | Input       |
| 72   | DEC_DIN1 | Decoder symbol input bit 1. Bit 7 is MSB. | Input       |
| 70   | DEC_DIN2 | Decoder symbol input bit 2. Bit 7 is MSB. | Input       |
| 61   | DEC_DIN3 | Decoder symbol input bit 3. Bit 7 is MSB. | Input       |
| 59   | DEC_DIN4 | Decoder symbol input bit 4. Bit 7 is MSB. | Input       |
| 53   | DEC_DIN5 | Decoder symbol input bit 5. Bit 7 is MSB. | Input       |
| 46   | DEC_DIN6 | Decoder symbol input bit 6. Bit 7 is MSB. | Input       |
| 44   | DEC_DIN7 | Decoder symbol input bit 7. Bit 7 is MSB. | Input       |

## Decoder Output Pins

| Pin# | Signal    | Description                      | Signal Type |
|------|-----------|----------------------------------|-------------|
| 22   | DEC_DOUT0 | Data output bit 0. Bit 7 is MSB. | Output      |
| 19   | DEC_DOUT1 | Data output bit 1. Bit 7 is MSB. | Output      |
| 18   | DEC_DOUT2 | Data output bit 2. Bit 7 is MSB. | Output      |
| 15   | DEC_DOUT3 | Data output bit 3. Bit 7 is MSB. | Output      |
| 13   | DEC_DOUT4 | Data output bit 4. Bit 7 is MSB. | Output      |
| 9    | DEC_DOUT5 | Data output bit 5. Bit 7 is MSB. | Output      |
| 7    | DEC_DOUT6 | Data output bit 6. Bit 7 is MSB. | Output      |
| 122  | DEC_DOUT7 | Data output bit 7. Bit 7 is MSB. | Output      |

## Decoder Error Magnitude Pins

| Pin# | Signal   | Description                                                                                                                                                                                       | Signal Type |
|------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 2    | DEC_MAG0 | Error Magnitude 0. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | Output      |
| 4    | DEC_MAG1 | Error Magnitude 1. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | Output      |

## Decoder Error Magnitude Pins, continued

| Pin# | Signal   | Description                                                                                                                                                                                       | Signal Type |
|------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 6    | DEC_MAG2 | Error Magnitude 2. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | Output      |
| 25   | DEC_MAG3 | Error Magnitude 3. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | Output      |
| 27   | DEC_MAG4 | Error Magnitude 4. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | Output      |
| 30   | DEC_MAG5 | Error Magnitude 5. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | Output      |
| 39   | DEC_MAG6 | Error Magnitude 6. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | Output      |
| 42   | DEC_MAG7 | Error Magnitude 7. This output indicates which bit of the current symbol output on Q7-Q0 has been corrected when LOC is HIGH. This output is indeterminate and should be ignored when LOC is low. | Output      |

## Decoder Parity Input Pins

| Pin# | Signal | Description                                                                                                                                                                                                                                                    | Signal Type |
|------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 90   | DEC_P1 | Decoder parity input bit 1. This determines the value of (P) which is the maximum of check bytes that the device will use in correction before flagging the block as uncorrectable. Normally set to the # of check bytes (R). P4 is the most significant bits. | Input       |
| 88   | DEC_P2 | Decoder parity input bit 2. This determines the value of (P) which is the maximum of check bytes that the device will use in correction before flagging the block as uncorrectable. Normally set to the # of check bytes (R). P4 is the most significant bits. | Input       |
| 86   | DEC_P3 | Decoder parity input bit 3. This determines the value of (P) which is the maximum of check bytes that the device will use in correction before flagging the block as uncorrectable. Normally set to the # of check bytes (R). P4 is the most significant bits. | Input       |
| 92   | DEC_P4 | Decoder parity input bit 4. This determines the value of (P) which is the maximum of check bytes that the device will use in correction before flagging the block as uncorrectable. Normally set to the # of check bytes (R). P4 is the most significant bits. | Input       |

## Decoder Latency Select Pins

| Pin# | Signal     | Description                                                                                               | Signal Type |
|------|------------|-----------------------------------------------------------------------------------------------------------|-------------|
| 110  | DEC_SHORT1 | Decoder latency select 1. Selects latency according to Table 2: Latency and Minimum Block Size Selection. | Input       |
| 95   | DEC_SHORT2 | Decoder latency select 2. Selects latency according to Table 2: Latency and Minimum Block Size Selection. | Input       |

## Decoder Control and Status Pins

| Pin# | Signal      | Description                                                                                                                                                                                                                                         | Signal Type |
|------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 117  | DEC_CLOCK   | Decoder master clock. All inputs and outputs are synchronized by the rising edge of DEC_CLOCK.                                                                                                                                                      | Input       |
| 119  | DEC_CORR    | Decoder message block corrected. Assertive HIGH. Indicates that errors have been found and corrected in message block.                                                                                                                              | Output      |
| 24   | DEC_DATARDY | Data Ready. Assertive HIGH. This output is held HIGH for data bytes and low check bytes.                                                                                                                                                            | Output      |
| 80   | DEC_DATEN   | Decoder data enable. Assertive HIGH. This input is used to signal the difference between data bytes and check bytes.                                                                                                                                | Input       |
| 81   | DEC_ENABIN  | Decoder enable data correction. Assertive HIGH. When this input is asserted, the device performs corrections on the message block. When CEN is low, the device does not perform corrections but continues to report status is initialized to do so. | Input       |
| 120  | DEC_EOB     | Decoder End of Block. 1/0 = End/Not end of block.                                                                                                                                                                                                   | Output      |
| 123  | DEC_LOC     | Decoder Error Location. Assertive HIGH. This output goes HIGH if the current symbol output on Q7-Q0 has had a correction applied to it.                                                                                                             | Output      |
| 102  | DEC_RESET   | Decoder system reset. Assertive LOW. Reset timing is critical to the initialization of the device.                                                                                                                                                  | Input       |
| 40   | DEC_STATEN  | Status Enable. Assertive HIGH. If this signal is HIGH during reset then the decoder will be programmed to output two status bytes with each message block.                                                                                          | Input       |
| 65   | DEC_UNCORR  | Decoder uncorrectable block. Assertive HIGH. Indicates message block contains uncorrectable errors.                                                                                                                                                 | Output      |

## Encoder Data Input Pins

| Pin# | Signal   | Description               | Signal Type |
|------|----------|---------------------------|-------------|
| 113  | ENC_DIN0 | Encoder data input bit 0. | Input       |
| 103  | ENC_DIN1 | Encoder data input bit 1. | Input       |
| 99   | ENC_DIN2 | Encoder data input bit 2. | Input       |
| 91   | ENC_DIN3 | Encoder data input bit 3. | Input       |
| 63   | ENC_DIN4 | Encoder data input bit 4. | Input       |
| 67   | ENC_DIN5 | Encoder data input bit 5. | Input       |
| 50   | ENC_DIN6 | Encoder data input bit 6. | Input       |
| 54   | ENC_DIN7 | Encoder data input bit 7. | Input       |

## Encoder Data Output Pins

| Pin# | Signal    | Description               | Signal Type |
|------|-----------|---------------------------|-------------|
| 111  | ENC_DOUT0 | Encoder data output bit 0 | Tristate    |
| 105  | ENC_DOUT1 | Encoder data output bit 1 | Tristate    |
| 97   | ENC_DOUT2 | Encoder data output bit 2 | Tristate    |
| 93   | ENC_DOUT3 | Encoder data output bit 3 | Tristate    |
| 60   | ENC_DOUT4 | Encoder data output bit 4 | Tristate    |
| 68   | ENC_DOUT5 | Encoder data output bit 5 | Tristate    |
| 48   | ENC_DOUT6 | Encoder data output bit 6 | Tristate    |
| 56   | ENC_DOUT7 | Encoder data output bit 7 | Tristate    |

## Encoder T Select Pins

| Pin# | Signal  | Description                       | Signal Type |
|------|---------|-----------------------------------|-------------|
| 87   | ENC_TA0 | Bit 0 of the encoder T select bus | Input       |
| 85   | ENC_TA1 | Bit 1 of the encoder T select bus | Input       |
| 83   | ENC_TA2 | Bit 2 of the encoder T select bus | Input       |
| 94   | ENC_TA3 | Bit 3 of the encoder T select bus | Input       |

## Encoder Control and Status Pins

| Pin# | Signal    | Description                                            | Signal Type |
|------|-----------|--------------------------------------------------------|-------------|
| 79   | ENC_TRIEN | Tri-states the encoder ENC_DOUT bus drivers when HIGH  | Input       |
| 75   | ENC_ENIN  | Enable encoder DIN bus into the parity generator       | Input       |
| 73   | ENC_ENOUT | Enables encoder DIN bus onto the DOUT bus              | Input       |
| 71   | ENC_RDY   | Indicates data symbols are on the encoder ENC_DOUT bus | Output      |
| 77   | ENC_RESET | Initializes encoder into a know state (high)           | Input       |
| 82   | ENC_CLOCK | Encoder master and symbol clock.                       | Input       |

## Encoder and Decoder Foundry Test Pins

| Pin# | Signal      | Description                   | Signal Type |
|------|-------------|-------------------------------|-------------|
| 115  | DEC_TEST_SE | Foundry Test Pin - Do not Use | Input       |
| 51   | DEC_TEST_SI | Foundry Test Pin - Do not Use | Input       |
| 108  | DEC_TEST_SO | Foundry Test Pin - Do not Use | Output      |
| 36   | ENC_TEST_SE | Foundry Test Pin - Do not Use | Input       |
| 45   | ENC_TEST_SI | Foundry Test Pin - Do not Use | Input       |
| 116  | ENC_TEST_SO | Foundry Test Pin - Do not Use | Output      |

## Ground Pins

| Pin# | Signal | Description |
|------|--------|-------------|
| 11   | GND    | Ground      |
| 20   | GND    | Ground      |
| 23   | GND    | Ground      |
| 37   | GND    | Ground      |
| 38   | GND    | Ground      |
| 47   | GND    | Ground      |
| 55   | GND    | Ground      |
| 58   | GND    | Ground      |
| 69   | GND    | Ground      |
| 78   | GND    | Ground      |
| 106  | GND    | Ground      |
| 109  | GND    | Ground      |
| 112  | GND    | Ground      |
| 118  | GND    | Ground      |
| 126  | GND    | Ground      |

## No Connect Pins

| Pin# | Signal | Description   |
|------|--------|---------------|
| 1    | NC     | No Connection |
| 3    | NC     | No Connection |
| 5    | NC     | No Connection |
| 10   | NC     | No Connection |
| 12   | NC     | No Connection |
| 14   | NC     | No Connection |
| 16   | NC     | No Connection |
| 21   | NC     | No Connection |
| 26   | NC     | No Connection |
| 28   | NC     | No Connection |
| 29   | NC     | No Connection |
| 31   | NC     | No Connection |
| 32   | NC     | No Connection |
| 33   | NC     | No Connection |
| 34   | NC     | No Connection |

## No Connect Pins, continued

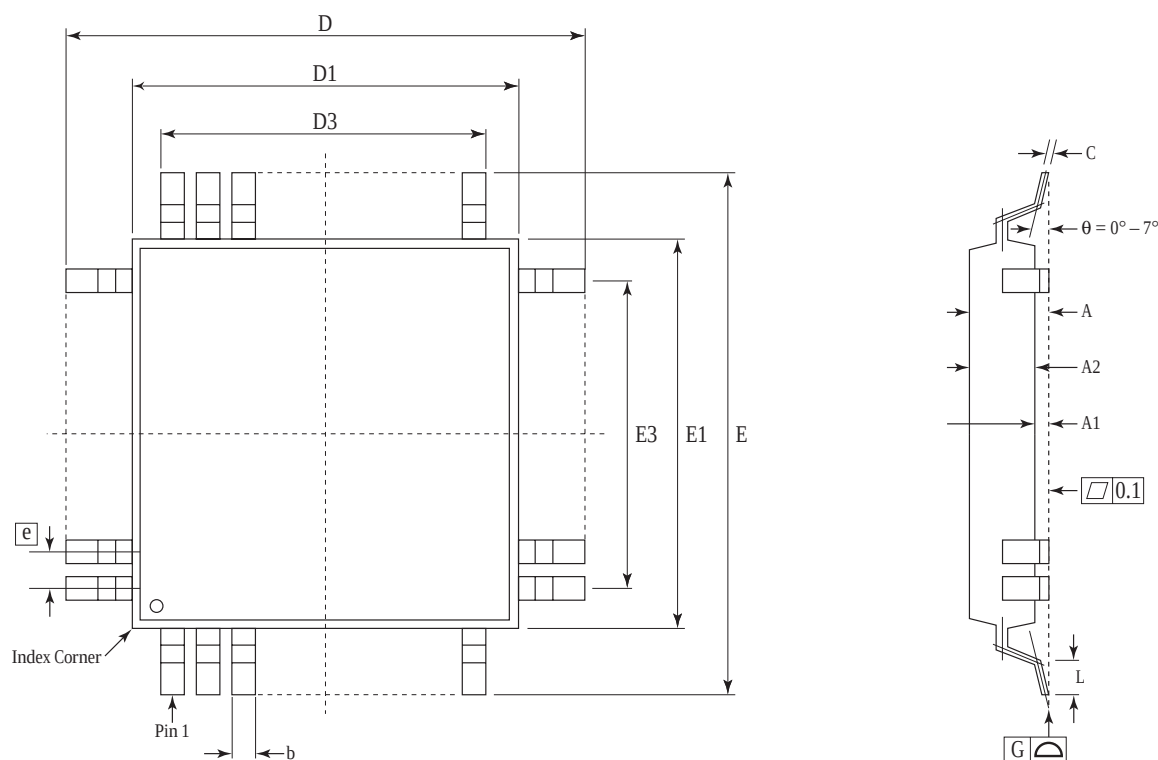
| Pin# | Signal | Description   |
|------|--------|---------------|
| 41   | NC     | No Connection |
| 62   | NC     | No Connection |
| 64   | NC     | No Connection |
| 96   | NC     | No Connection |
| 98   | NC     | No Connection |
| 100  | NC     | No Connection |
| 107  | NC     | No Connection |
| 121  | NC     | No Connection |
| 125  | NC     | No Connection |
| 127  | NC     | No Connection |

## Votlage Supply Pins

| Pin# | Signal          | Description |
|------|-----------------|-------------|
| 8    | V <sub>dd</sub> | +5 V Power  |
| 17   | V <sub>dd</sub> | +5 V Power  |
| 35   | V <sub>dd</sub> | +5 V Power  |
| 43   | V <sub>dd</sub> | +5 V Power  |
| 49   | V <sub>dd</sub> | +5 V Power  |
| 52   | V <sub>dd</sub> | +5 V Power  |
| 57   | V <sub>dd</sub> | +5 V Power  |
| 66   | V <sub>dd</sub> | +5 V Power  |
| 74   | V <sub>dd</sub> | +5 V Power  |
| 84   | V <sub>dd</sub> | +5 V Power  |
| 89   | V <sub>dd</sub> | +5 V Power  |
| 101  | V <sub>dd</sub> | +5 V Power  |
| 104  | V <sub>dd</sub> | +5 V Power  |
| 114  | V <sub>dd</sub> | +5 V Power  |
| 124  | V <sub>dd</sub> | +5 V Power  |
| 128  | V <sub>dd</sub> | +5 V Power  |

## Packaging

Table 6: PLCC Dimensions



## Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm.
6. Coplanarity, measured at seating plane G, to be 0.10 mm max.

Part Numbers: Complete ordering code COic5130A

Parts are packaged in anti static tubes of 18 units each.

To order call 650-321-3390, fax 650-322-8569,  
or email [sales@co-optic.com](mailto:sales@co-optic.com)

| Symbol       | Control Dimensions<br>in millimeters |         |       | Alternate Dimensions<br>in inches |         |       |
|--------------|--------------------------------------|---------|-------|-----------------------------------|---------|-------|
|              | Min                                  | Nominal | Max   | Min                               | Nominal | Max   |
| A            | 3.45                                 |         | 4.10  | 0.136                             |         | 0.161 |
| A1           | 0.25                                 |         | 0.50  | 0.010                             |         | 0.020 |
| A2           | 3.20                                 |         | 3.60  | 0.126                             |         | 0.142 |
| D            | 30.95                                |         | 31.45 | 1.219                             |         | 1.238 |
| D1           | 27.80                                |         | 28.20 | 1.094                             |         | 1.110 |
| D3           | 24.80 Ref.                           |         |       | 0.976 Ref.                        |         |       |
| E            | 30.95                                |         | 31.45 | 1.219                             |         | 1.238 |
| E1           | 27.80                                |         | 28.20 | 1.094                             |         | 1.110 |
| E3           | 24.80 Ref.                           |         |       | 0.976 Ref.                        |         |       |
| L            | 0.73                                 |         | 1.03  | 0.029                             |         | 0.041 |
| e            | 0.80 BSC.                            |         |       | 0.031 BSC.                        |         |       |
| b            | 0.30                                 |         | 0.45  | 0.012                             |         | 0.018 |
| c            | 0.11                                 |         | 0.23  | 0.004                             |         | 0.009 |
| Pin Features |                                      |         |       |                                   |         |       |
| N            | 128                                  |         |       |                                   |         |       |
| ND           | 32                                   |         |       |                                   |         |       |
| NE           | 32                                   |         |       |                                   |         |       |
| Note         | Square                               |         |       |                                   |         |       |