DATA SHEET

TDA8766
10-bit high-speed 2.7 to 5.25 V analog-to-digital converter

Product specification
Supersedes data of 1995 Mar 22
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

10-bit high-speed 2.7 to 5.25 V analog-to-digital converter

TDA8766

FEATURES

- 10-bit resolution
- 2.7 to 5.25 V operation
- Sampling rate up to 20 MHz
- DC sampling allowed
- High signal-to-noise ratio over a large analog input frequency range (9.3 effective bits at 1.0 MHz full-scale input at f_{clk} = 20 MHz)
- In range (IR) CMOS output
- CMOS/TTL compatible digital inputs and outputs
- External reference voltage regulator
- Power dissipation only 53 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- Standby mode
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Camera
- Camcorder
- Radio communication.

GENERAL DESCRIPTION

The TDA8766 is a 10-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. It converts with 2.7 to 5.25 V operation the analog input signal into 10-bit binary-coded digital words at a maximum sampling rate of 20 MHz. All digital inputs and outputs are CMOS compatible. A standby mode allows reduction of the device power consumption down to 4 mW.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		2.7	3.3	5.25	V
V_{DDD1}	digital supply voltage 1		2.7	3.3	5.25	V
V_{DDD2}	digital supply voltage 2		2.7	3.3	5.25	V
V_{DDO}	output stages supply voltage		2.5	3.3	5.25	V
I_{DDA}	analog supply current		–	7.5	10	mA
I_{DDD}	digital supply current		–	7.5	10	mA
I_{DDO}	output stages supply current	f_{clk} = 20 MHz; C_L = 20 pF; ramp input	–	1	2	mA
INL	integral non-linearity	f_{clk} = 20 MHz; ramp input	–	±1	±2	LSB
DNL	differential non-linearity	f_{clk} = 20 MHz; ramp input	–	±0.25	±0.7	LSB
$f_{clk(max)}$	maximum clock frequency		20	–	–	MHz
P_{tot}	total power dissipation	$V_{DDA} = V_{DDD} = V_{DDO}$ = 3.3 V	–	53	73	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8766G	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1

BLOCK DIAGRAM

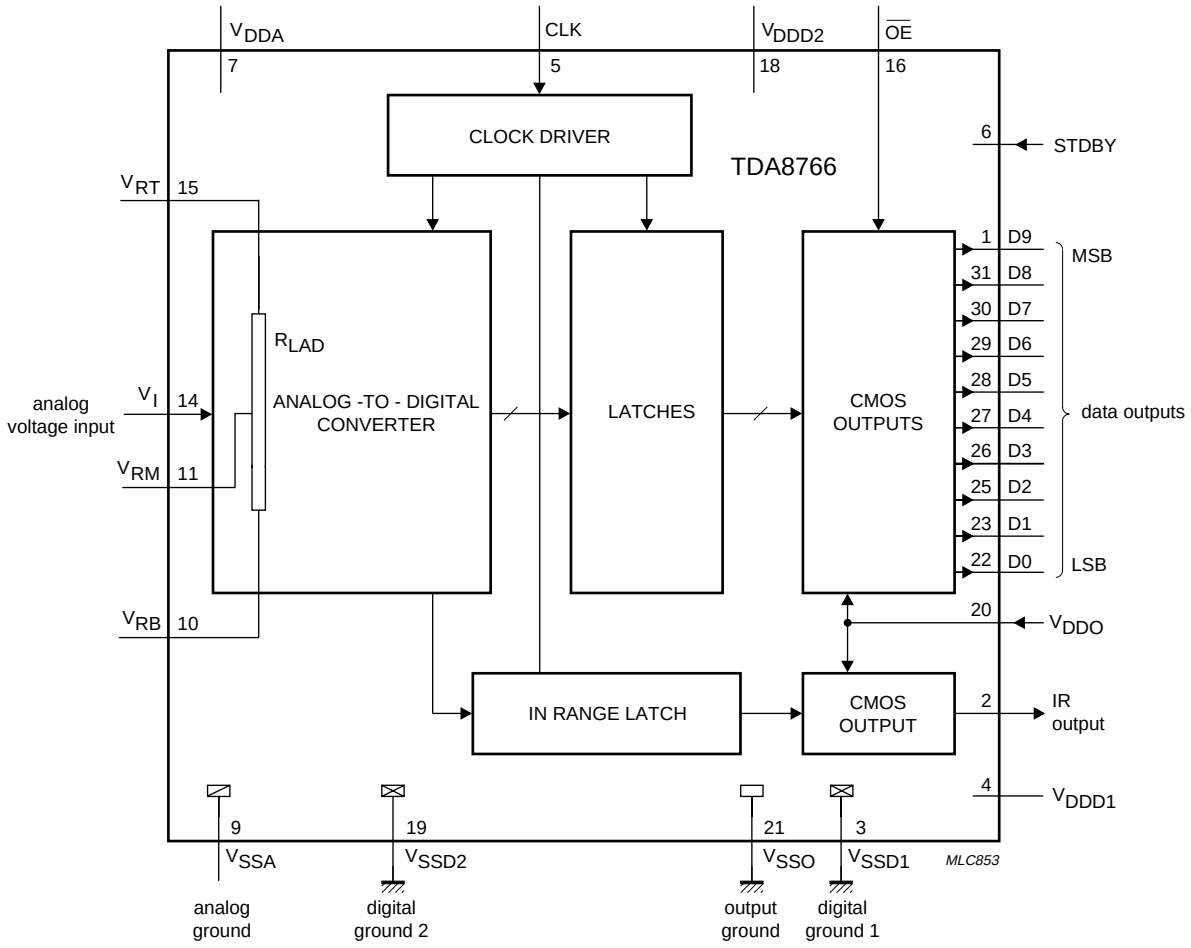


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D9	1	data output; bit 9 (MSB)
IR	2	in range data output
V_{SSD1}	3	digital ground 1
V_{DDD1}	4	digital supply voltage 1 (2.7 to 5.25 V)
CLK	5	clock input
STDBY	6	standby mode input
V_{DDA}	7	analog supply voltage (2.7 to 5.25 V)
n.c.	8	not connected
V_{SSA}	9	analog ground
V_{RB}	10	reference voltage BOTTOM input
V_{RM}	11	reference voltage MIDDLE
n.c.	12	not connected
n.c.	13	not connected
V_I	14	analog input voltage
V_{RT}	15	reference voltage TOP input
$\overline{OE}$	16	output enable input
n.c.	17	not connected

SYMBOL	PIN	DESCRIPTION
V_{DDD2}	18	digital supply voltage 2 (2.7 to 5.25 V)
V_{SSD2}	19	digital ground 2
V_{DDO}	20	positive supply voltage for output stage (2.5 to 5.25 V)
V_{SSO}	21	digital output ground
D0	22	data output; bit 0 (LSB)
D1	23	data output; bit 1
n.c.	24	not connected
D2	25	data output; bit 2
D3	26	data output; bit 3
D4	27	data output; bit 4
D5	28	data output; bit 5
D6	29	data output; bit 6
D7	30	data output; bit 7
D8	31	data output; bit 8
n.c.	32	not connected

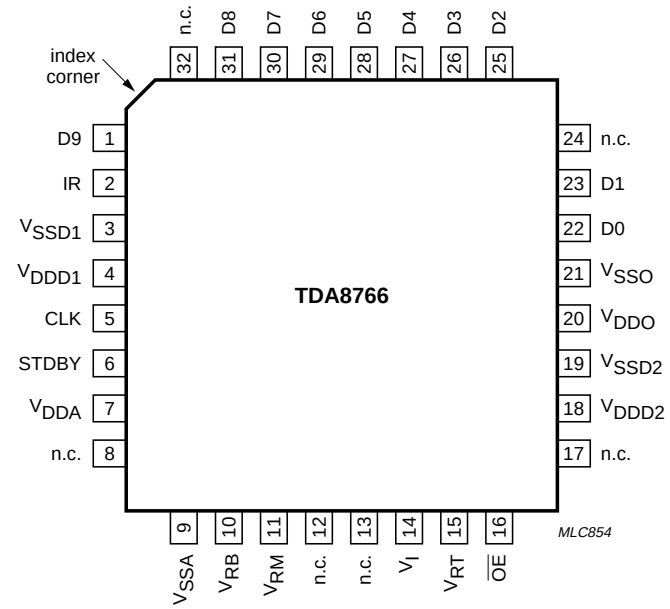


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	note 1	–0.3	+7.0	V
V_{DDD1}, V_{DDD2}	digital supply voltages	note 1	–0.3	+7.0	V
V_{DDO}	output stages supply voltage	note 1	–0.3	+7.0	V
ΔV_{DD}	supply voltage difference				
	$V_{DDA} - V_{DDD}$		–1.0	+4.0	V
	$V_{DDD} - V_{DDO}$		–1.0	+4.0	V
	$V_{DDA} - V_{DDO}$		–1.0	+4.0	V
V_I	input voltage	referenced to V_{SSA}	–0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to V_{SSD}	–	V_{DDD}	V
I_O	output current		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–20	+75	°C
T_j	junction temperature		–	+150	°C

Note

1. The supply voltages V_{DDA}, V_{DDD} and V_{DDO} may have any value between –0.3 V and +7.0 V provided that the supply voltage differences ΔV_{DD} are respected.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	90	K/W

CHARACTERISTICS

V_{DDA} = V_7 to V_9 = 3.3 V; V_{DDD} = V_4 to V_3 = V_{18} to V_{19} = 3.3 V; V_{DDO} = V_{20} to V_{21} = 3.3 V; V_{SSA}, V_{SSD} and V_{SSO} short-circuited together; $V_{i(p-p)}$ = 1.83 V; C_L = 20 pF; T_{amb} = 0 to +70 °C; typical values measured at T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		2.7	3.3	5.25	V
V_{DDD1}	digital supply voltage 1		2.7	3.3	5.25	V
V_{DDD2}	digital supply voltage 2		2.7	3.3	5.25	V
V_{DDO}	output stages supply voltage		2.5	3.3	5.25	V
ΔV_{DD}	voltage difference					
	$V_{DDA} - V_{DDD}$		–0.2	–	+0.2	V
	$V_{DDA} - V_{DDO}$		–0.2	–	+3.0	V
	$V_{DDD} - V_{DDO}$		–0.2	–	+3.0	V
I_{DDA}	analog supply current		–	7.5	10	mA
I_{DDD}	digital supply current		–	7.5	10	mA
I_{DDO}	output stages supply current	f_{clk} = 20 MHz; ramp input; C_L = 20 pF	–	1	2	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO V_{SSD}); see note 1						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	V_{DDD}	V
		$V_{DDD} \leq 3.6$ V	$0.6V_{DDD}$	–	V_{DDD}	V
I_{IL}	LOW level input current	$V_{clk} = 0.3V_{DDD}$	–1	0	+1	µA
I_{IH}	HIGH level input current	$V_{clk} = 0.7V_{DDD}$	–	–	5	µA
Z_I	input impedance	f_{clk} = 20 MHz	–	4	–	kΩ
C_I	input capacitance	f_{clk} = 20 MHz	–	3	–	pF
INPUTS $\overline{OE}$ AND STDBY (REFERENCED TO V_{SSD}); see Table 3						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DDD}$	–	V_{DDD}	V
		$V_{DDD} \leq 3.6$ V	$0.6V_{DDD}$	–	V_{DDD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.3V_{DDD}$	–1	–	–	µA
I_{IH}	HIGH level input current	$V_{IH} = 0.7V_{DDD}$	–	–	+1	µA
V_I (ANALOG INPUT VOLTAGE REFERENCED TO V_{SSA})						
I_{IL}	LOW level input current	$V_I = V_{RB}$	–	0	–	µA
I_{IH}	HIGH level input current	$V_I = V_{RT}$	–	35	–	µA
Z_I	input impedance	f_i = 1 MHz	–	5	–	kΩ
C_I	input capacitance	f_i = 1 MHz	–	8	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltages for the resistor ladder; see Table 1						
V_{RB}	reference voltage BOTTOM		1.1	1.2	–	V
V_{RT}	reference voltage TOP	$V_{TOP} \leq V_{DDA}$	2.7	3.3	V_{DDA}	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		1.5	2.1	2.7	V
I_{ref}	reference current		–	7.2	–	mA
R_{LAD}	resistor ladder		–	290	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	1860	–	ppm
			–	539	–	mΩ/K
V_{osB}	offset voltage BOTTOM	note 2	–	135	–	mV
V_{osT}	offset voltage TOP	note 2	–	135	–	mV
$V_{i(p-p)}$	analog input voltage (peak-to-peak value)	note 3	1.4	1.83	2.4	V
Outputs						
DIGITAL OUTPUTS D9 TO D0 AND IR (REFERENCED TO V_{SSD})						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.5	V
V_{OH}	HIGH level output voltage	I_O = –1 mA	V_{DDO} – 0.5	–	V_{DDO}	V
I_{OZ}	output current in 3-state mode	0.5 V < V_O < V_{DDO}	–20	–	+20	μA
Switching characteristics						
CLOCK INPUT CLK; see Fig.4; note 1						
$f_{clk(max)}$	maximum clock frequency		20	–	–	MHz
t_{CPH}	clock pulse width HIGH		15	–	–	ns
t_{CPL}	clock pulse width LOW		15	–	–	ns
Analog signal processing						
LINEARITY						
INL	integral non-linearity	f_{clk} = 20 MHz; ramp input; (see Fig.6)	–	±1	±2	LSB
DNL	differential non-linearity	f_{clk} = 20 MHz; ramp input; (see Fig.7)	–	±0.25	±0.7	LSB
INPUT SET RESPONSE (f_{clk} = 20 MHz; see Fig.8; note 4)						
t_{STLH}	analog input settling time LOW-to-HIGH	full-scale square wave	–	4	6	ns
t_{STHL}	analog input settling time HIGH-to-LOW	full-scale square wave	–	4	6	ns
HARMONICS; (f_{clk} = 20 MHz; see Fig.9; note 5)						
THD	total harmonic distortion	f_i = 1 MHz	–	–63	–	dB
SIGNAL-TO-NOISE RATIO; see Fig.9; note 5						
S/N	signal-to-noise ratio (full scale)	without harmonics; f_{clk} = 20 MHz; f_i = 1 MHz	–	60	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EFFECTIVE BITS; see Fig.9; note 5						
EB	effective bits	f_{clk} = 20 MHz				
		f_i = 300 kHz	–	9.5	–	bits
		f_i = 1 MHz	–	9.3	–	bits
		f_i = 3.58 MHz	–	8.0	–	bits
Timing (f_{clk} = 20 MHz; C_L = 20 pF); see Fig.4; note 6						
t_{ds}	sampling delay time		–	–	5	ns
t_h	output hold time		5	–	–	ns
t_d	output delay time	V_{DDO} = 4.75 V	8	12	15	ns
		V_{DDO} = 3.15 V	8	17	20	ns
		V_{DDO} = 2.7 V	8	21	24	ns
3-state output delay times; see Fig.5						
t_{dZH}	enable HIGH		–	14	18	ns
t_{dZL}	enable LOW		–	16	20	ns
t_{dHZ}	disable HIGH		–	16	20	ns
t_{dLZ}	disable LOW		–	14	18	ns
Standby mode output delay times						
t_{dSTBLH}	standby (LOW-to-HIGH transition)		–	–	200	ns
t_{dSTBHL}	start-up (HIGH-to-LOW transition)		–	–	500	ns

Notes

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 1 ns.
2. Analog input voltages producing code 0 up to and including 1023:
   a) V_{osB} (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C.
   b) V_{osT} (voltage offset TOP) is the difference between V_{RT} (reference voltage TOP) and the analog input which produces data outputs equal to 1023 at T_{amb} = 25 °C.
3. In order to ensure the optimum linearity performance of such converter architecture the lower and upper extremities of the converter reference resistor ladder (corresponding to output codes 0 and 1023 respectively) are connected to pins V_{RB} and V_{RT} via offset resistors R_{OB} and R_{OT} as shown in Fig.3.
   a) The current flowing into the resistor ladder is $I_L = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$ and the full-scale input range at the converter, to cover code 0 to code 1023, is $V_I = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} - V_{RB}) = 0.871 \times (V_{RT} - V_{RB})$
   b) Since R_L, R_{OB} and R_{OT} have similar behaviour with respect to process and temperature variation, the ratio $\frac{R_L}{R_{OB} + R_L + R_{OT}}$ will be kept reasonably constant from part to part. Consequently variation of the output codes at a given input voltage depends mainly on the difference $V_{RT} - V_{RB}$ and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is then optimized.

4. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
5. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: S/N = EB $\times$ 6.02 + 1.76 dB.
6. Output data acquisition: the output data is available after the maximum delay time of t_d.

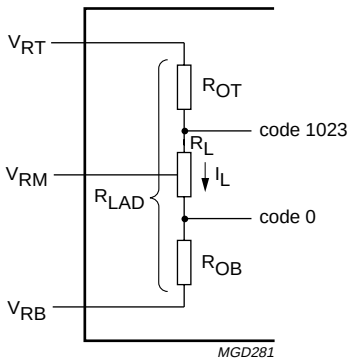


Fig.3 Explanation of note 3.

Table 1 Output coding and input voltage (typical values; referenced to V_{SSA})

STEP	$V_{I(p-p)}$ (V)	IR	BINARY OUTPUT BITS									
			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<1.335	0	0	0	0	0	0	0	0	0	0	0
0	1.335	1	0	0	0	0	0	0	0	0	0	0
1	.	1	0	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
1022	.	1	1	1	1	1	1	1	1	1	1	0
1023	3.165	1	1	1	1	1	1	1	1	1	1	1
Overflow	>3.165	0	1	1	1	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{OE}$	D9 TO D0	IR
1	high impedance	high impedance
0	active; binary	active

Table 3 Standby selection

STDBY	D9 TO D0	$I_{DDA} + I_{DDD}$ (typ.)
1	last logic state	1.2 mA
0	active	15 mA

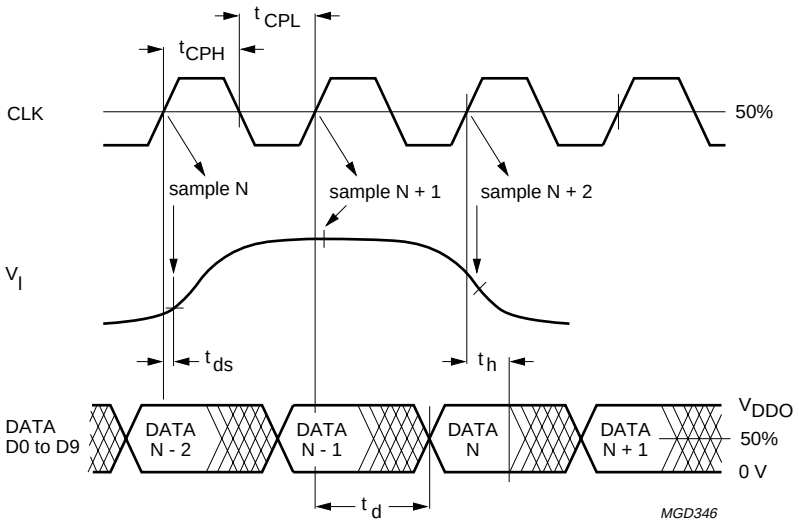
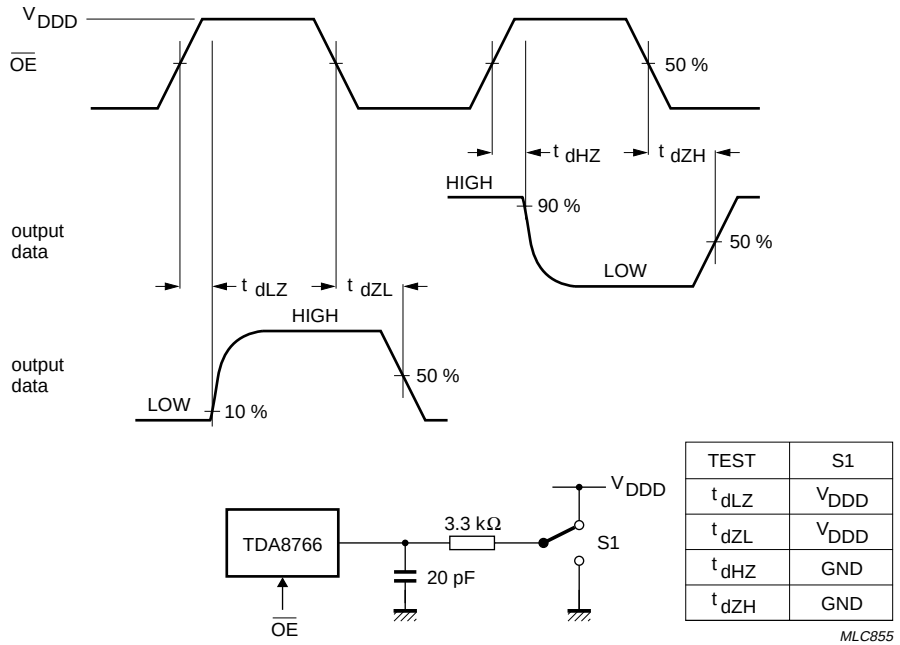


Fig.4 Timing diagram.



TEST	S1
t_{dLZ}	V_{DDD}
t_{dZL}	V_{DDD}
t_{dHZ}	GND
t_{dZH}	GND

$f_{\overline{OE}}$ = 100 kHz.

Fig.5 Timing diagram and test conditions of 3-state output delay time.

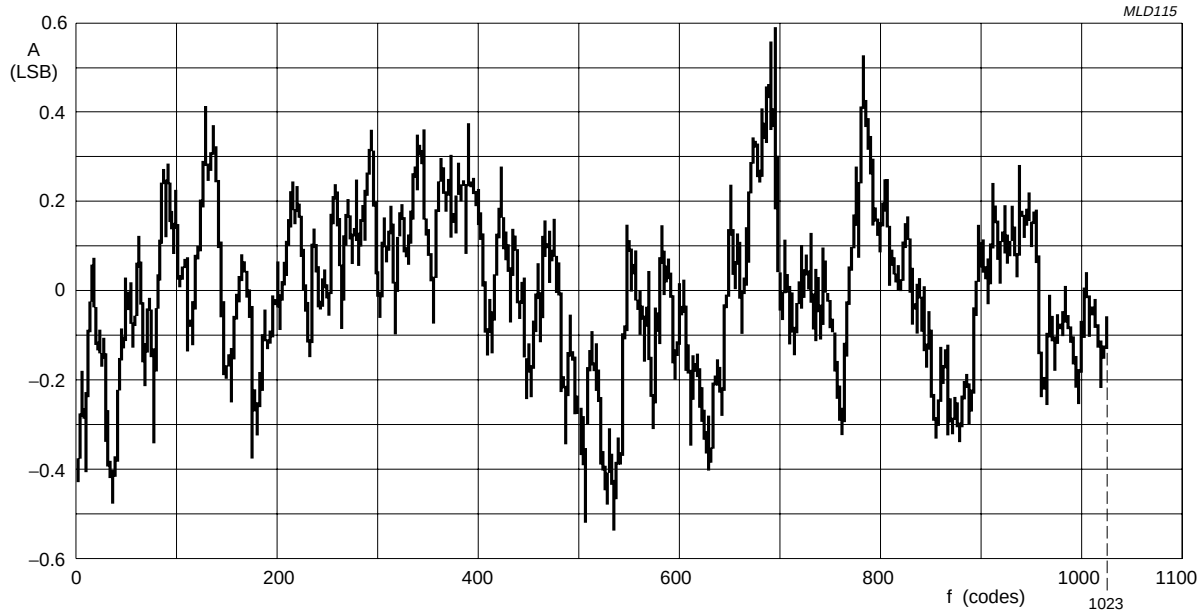


Fig.6 Typical integral non-linearity (INL) performance.

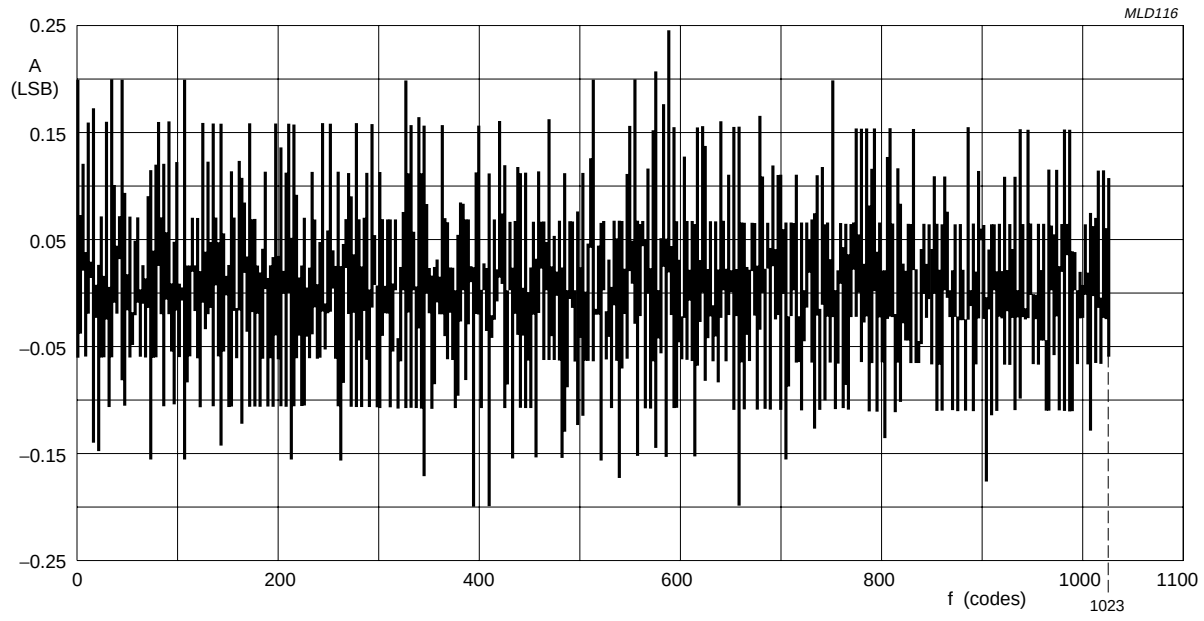


Fig.7 Typical differential non-linearity (DNL) performance.

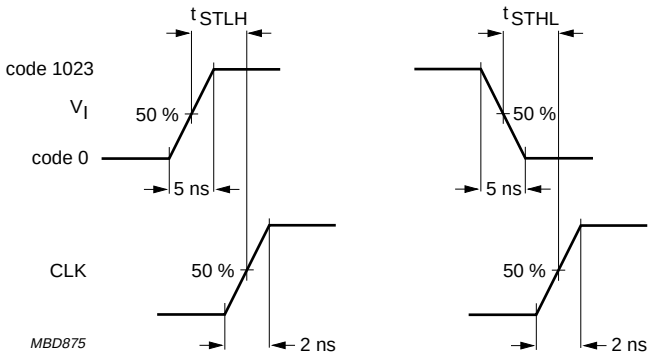
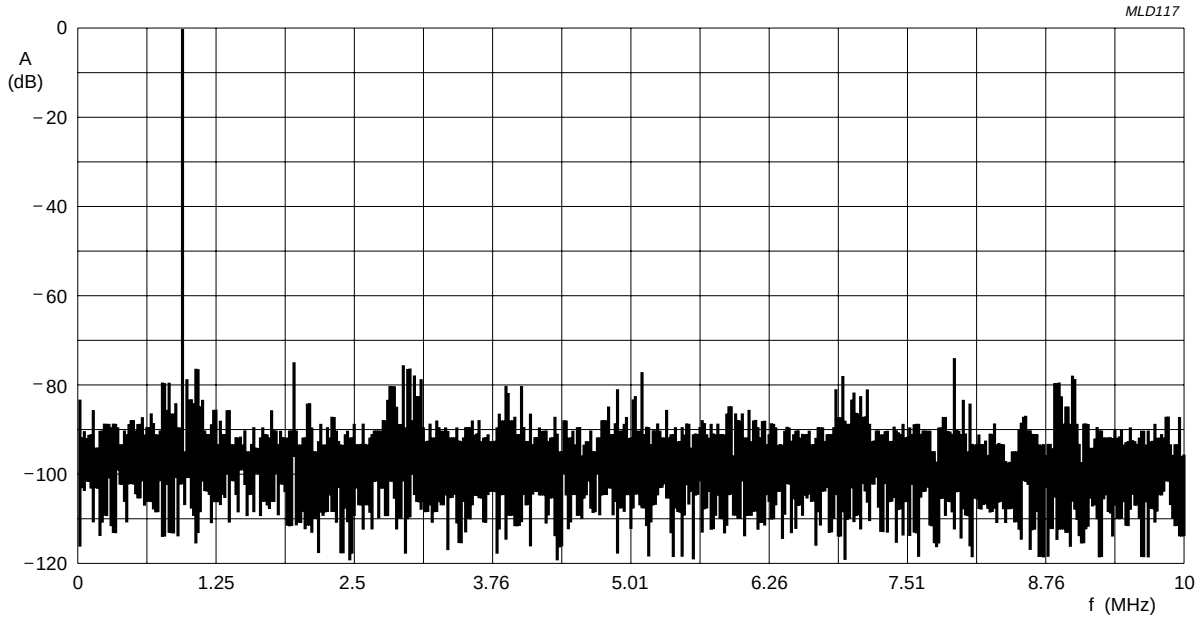


Fig.8 Analog input settling-time diagram.



Effective bits: 9.59; THD = −76.60 dB.
Harmonic levels (dB): 2nd = −81.85; 3rd = −87.56; 4th = −88.81; 5th = −88.96; 6th = −79.58.

Fig.9 Typical Fast Fourier Transform (f_{clk} = 20 MHz; f_i = 1 MHz).

INTERNAL PIN CONFIGURATIONS

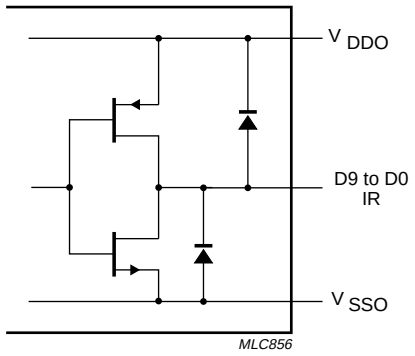


Fig.10 CMOS data and In Range (IR) outputs.

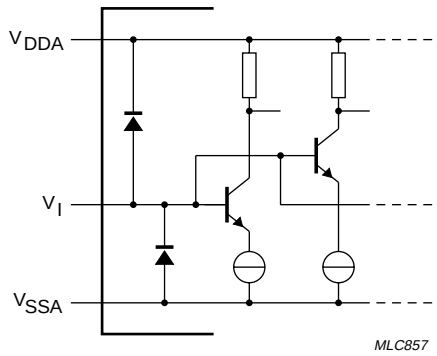


Fig.11 Analog inputs.

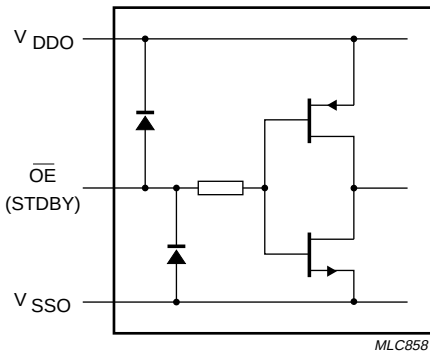


Fig.12 $\overline{OE}$ (STDBY) input.

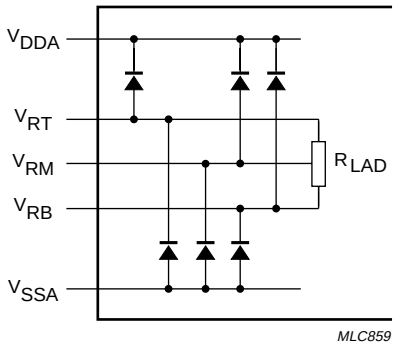


Fig.13 V_{RB}, V_{RM} and V_{RT}.

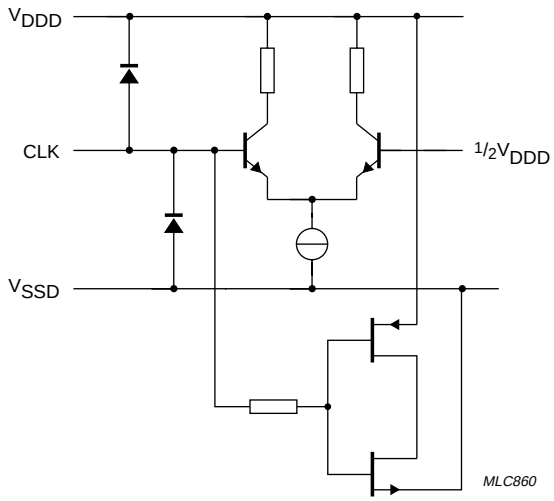
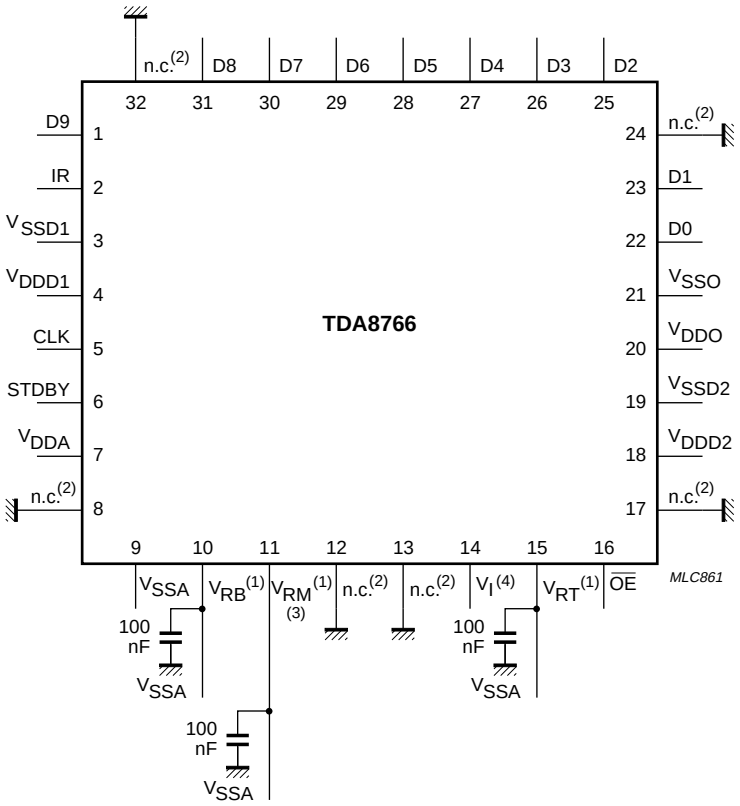


Fig.14 CLK input.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number *"AN96012"*).



The analog and digital supplies should be separated and decoupled.

The external voltage reference generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value. Eventually, the reference ladder voltages can be derived from a well regulated V_{DDA} supply through a resistor bridge and a decoupled capacitor.

(1) V_{RB}, V_{RM} and V_{RT} are decoupled to V_{SSA}.

(2) Pins 8, 12, 13, 17, 24 and 32 should be connected to the closest ground pin in order to prevent noise influence.

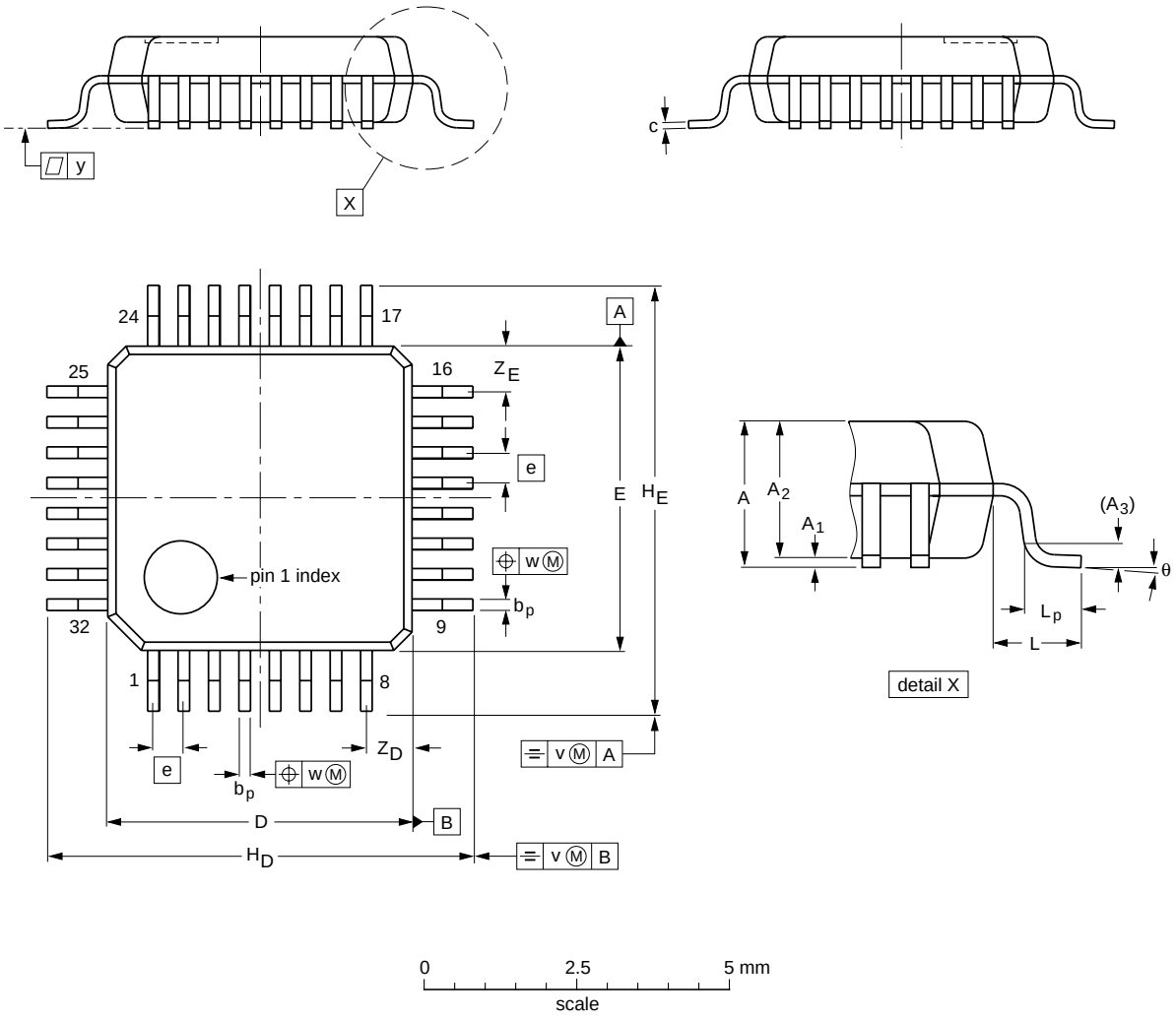
(3) When V_{RM} is not used, pin 11 can be left open, avoiding the decoupling capacitor. In any case, pin 11 must not be grounded.

(4) When analog input signal is AC coupled, an input bias or a clamping level must be applied to V_I input (pin 14).

Fig.15 Application diagram.

PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm **SOT401-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1						~~95-12-19~~ 97-08-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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