TS507

High precision rail-to-rail operational amplifier

Features

- Ultra low offset voltage: 25 µV typ, 100 µV max
- Rail-to-rail input/output voltage swing
- Operating from 2.7 V to 5.5 V
- High speed: 1.9 MHz
- 45° phase margin with 100 pF
- Low consumption: 0.8 mA at 2.7 V
- Very large signal voltage gain: 131 dB
- High power supply rejection ratio: 105 dB
- Very high ESD protection 5kV (HBM)
- Latch-up immunity
- Available in SOT23-5 micropackage

Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Medical instrumentation

Description

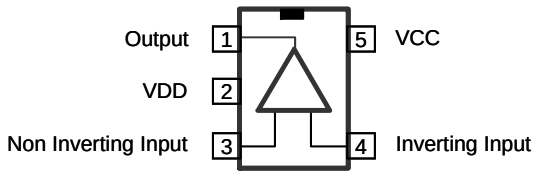
The TS507 is a high performance rail-to-rail input and output amplifier with very low offset voltage. This amplifier uses a new trimming technique that yields ultra low offset voltages without any need for external zeroing.

The circuit offers very stable electrical characteristics over the entire supply voltage range, and is particularly intended for automotive and industrial applications.

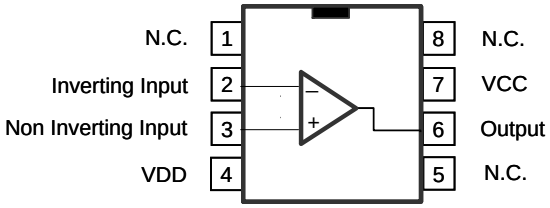
The TS507 is housed in the space-saving 5-pin SOT23 package, making it well suited for battery-powered systems. This micropackage simplifies the PC board design because of its ability to be placed in tight spaces (external dimensions are 2.8 mm x 2.9 mm).

Pin connections (top view)

SOT23-5



SO-8



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1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_{id}	Differential input voltage (2)	±2.5	V
V_{in}	Input voltage (3)	V_{DD}-0.3 to V_{CC}+0.3	V
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient(4) (5) SOT23-5 SO-8	 250 125	°C/W
R_{thjc}	Thermal resistance junction to case SOT23-5 SO-8	 81 40	°C/W
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model(6)	5	kV
	MM: machine model(7)	300	V
	CDM: charged device model(8)	2	kV
	Latch-up immunity	class A	

1. Value with respect to V_{DD} pin.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. V_{CC}-V_{in} must not exceed 6V and V_{in} must not exceed 6V.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. $R_{thja/c}$ are typical values.
6. Human body model: A 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
7. Machine model: A 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
8. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	2.7 to 5.5	V
V_{icm}	Common mode input voltage range	V_{DD} to V_{CC}	V
V_{id}	Differential input voltage(2)	±2.5	V
T_{oper}	Operating free air temperature range TS507C TS507I	 0 to +85 -40 to +125	°C

1. Value with respect to V_{DD} pin.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.

2 Electrical characteristics

Table 3. Electrical characteristics at V_{CC} = +5V, V_{DD} = 0V, V_{icm} = V_{CC}/2, T_{amb} = 25°C, R_L connected to V_{CC}/2 (unless otherwise specified)(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage(2)	V_{icm} = 0 to 3.8V, T=25°C TS507C full temp range TS507I full temp range		25	100 250 400	µV
		V_{icm} = 0V to 5V, T=25°C TS507C full temp range TS507I full temp range			450 550 750	µV
$\Delta V_{io}/\Delta t$	V_{io} drift vs. temperature	$T_{min} < T_{op} < T_{max}$		1		µV/°C
I_{ib}	Input bias current	T = 25°C TS507C full temp range TS507I full temp range		8	70 75 110	nA
I_{io}	Input offset current	T = 25°C TS507C full temp range TS507I full temp range		2	25 35 50	nA
CMRR	Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} from 0V to 3.8V, T=25°C TS507C full temp range TS507I full temp range	94 94 91	115		dB
		V_{icm} from 0V to 5V		96		
PSRR	Power supply rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$)	V_{CC} from 2.7V to 5.5V, V_{icm}=v_{cc}/2, T=25°C TS507C full temp range TS507I full temp range	91 90 89	105		dB
A_{vd}	Large signal voltage gain	R_L = 10kΩ, V_{out}= 0.5V to 4.5V Full temp range	99 98	131		dB
V_{CC}-V_{OH}	High level output voltage drop	R_L = 600Ω, T=25°C TS507C full temp range TS507I full temp range		67	95 110 120	mV
		R_L = 10kΩ, T=25°C Full Temp range		4	15 15	
V_{OL}	Low level output voltage	R_L = 600Ω, T=25°C TS507C full temp range TS507I full temp range		64	90 110 125	mV
		R_L = 10kΩ, T=25°C Full temp range		4	15 15	

Table 3. Electrical characteristics at V_{CC} = +5V, V_{DD} = 0V, V_{icm} = V_{CC}/2, T_{amb} = 25°C, R_L connected to V_{CC}/2 (unless otherwise specified)(1) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{out}	I_{sink}	V_{out} = V_{CC}, V_{id}=-1V, T=25°C TS507C full temp range TS507I full temp range	74 60 53	104		mA
	I_{source}	V_{out} = V_{DD}, V_{id}=1V, T=25°C TS507C full temp range TS507I full temp range	90 77 70	128		
I_{CC}	Supply current (per operator)(2)	No load, V_{out}=V_{CC}/2, V_{icm}=0 to 5V, T=25°C Full temp range		0.85	1.15 1.25	mA
Dynamic performance						
GBP	Gain bandwidth product	R_L = 2kΩ, C_L = 100pF, f = 100kHz		1.9		MHz
ϕ_m	Phase margin	R_L = 2kΩ, C_L=100pF		45		Degrees
G_m	Gain margin	R_L = 2kΩ, C_L=100pF		10		dB
SR	Slew rate	R_L = 2kΩ, C_L=100pF, V_{out} = 1.25V to 3.75V, 10% to 90%		0.6		V/µs
e_N	Equivalent input noise voltage	f = 1kHz		12		nV/√Hz
i_N	Equivalent input noise current	f = 10kHz		1.2		pA/√Hz
THD+e_N	THD + noise	f=1kHz, G=1, R_L=2kΩ, V_{icm}=2V, V_{out}=3.5V_{pp}		0.0003		%

1. All parameter limits at temperatures different from 25° C are guaranteed by correlation.
2. Measurements done at 4 V_{icm} values: V_{icm}=0 V, V_{icm}=3.8 V, V_{icm}=4.2 V, V_{icm}=5 V.

Table 4. Electrical characteristics at V_{CC} = +3.3V, V_{DD} = 0V, V_{icm} = V_{CC}/2, T_{amb} = 25°C, R_L connected to V_{CC}/2 (unless otherwise specified)(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage(2)	V_{icm} = 0 to 2.1V, T=25°C TS507C full temp range TS507I full temp range		25	100 250 400	µV
		V_{icm} = 0V to 3.3V, T=25°C TS507C full temp range TS507I full temp range			450 550 750	µV
ΔV_{io}	V_{io} drift vs. temperature	$T_{min} < T_{op} < T_{max}$		1		µV/°C
I_{ib}	Input bias current	T = 25°C TS507C full temp range TS507I full temp range		6	70 75 145	nA
I_{io}	Input offset current	T = 25°C TS507C full temp range TS507I full temp range		2	25 40 45	nA
CMRR	Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} from 0V to 2.1V		115		dB
A_{vd}	Large signal voltage gain	R_L = 10kΩ, V_{out}= 0.5V to 2.8V		127		dB
V_{CC}-V_{OH}	High level output voltage drop	R_L = 600Ω, T=25°C TS507C full temp range TS507I full temp range		59	85 100 110	mV
		R_L = 10kΩ, T=25°C Full temp range		4	15 15	
V_{OL}	Low level output voltage	R_L = 600Ω, T=25°C TS507C full temp range TS507I full temp range		57	80 100 115	mV
		R_L = 10kΩ, T=25°C Full temp range		4	15 15	
I_{out}	I_{sink}	V_{out} = V_{CC}, V_{id}=-1V, T=25°C TS507C full temp range TS507I full temp range	33 26 22	48		mA
	I_{source}	V_{out} = V_{DD}, V_{id}=1V, T=25°C TS507C full temp range TS507I full temp range	37 32 29	56		
I_{CC}	Supply current (per operator)(2)	No load, V_{out}=V_{CC}/2, V_{icm}=0 to 3.3V, T=25°C Full temp range		0.81	1.1 1.2	mA

Table 4. Electrical characteristics at V_{CC} = +3.3V, V_{DD} = 0V, V_{icm} = V_{CC}/2, T_{amb} = 25°C, R_L connected to V_{CC}/2 (unless otherwise specified)(1) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dynamic performance						
GBP	Gain bandwidth product	R_L = 2kΩ, C_L = 100pF, f = 100kHz		1.9		MHz
ϕ_m	Phase margin	R_L = 2kΩ, C_L=100pF		45		Degrees
G_m	Gain margin	R_L = 2kΩ, C_L=100pF		10		dB
SR	Slew rate	R_L = 2kΩ, C_L=100pF, V_{out}= 0.5V to 2.8V, 10% to 90%		0.6		V/µs
e_N	Equivalent input noise voltage	f = 1kHz		12		nV/√Hz
THD+e_N	THD + noise	f=1KHz, G=1, R_L=2kΩ, V_{icm}=1.15V, V_{out}=1.8V_{pp}		0.0004		%

1. All parameter limits at temperatures different from 25° C are guaranteed by correlation.
2. Measurements done at 4 V_{icm} values: V_{icm}=0 V, V_{icm}=2.1 V, V_{icm}=2.5 V, V_{icm}=3.3 V.

Table 5. Electrical characteristics at V_{CC} = +2.7V V_{DD} = 0V, V_{icm} = V_{CC}/2, T_{amb} = 25°C, R_L connected to V_{CC}/2 (unless otherwise specified)(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage(2)	V_{icm} = 0 to 1.9V, T=25°C TS507C full temp range TS507I full temp range		25	100 250 400	µV
		V_{icm} = 0V to 2.7V, T=25°C TS507C full temp range TS507I full temp range			450 550 750	µV
ΔV_{io}	V_{io} drift vs. temperature	$T_{min} < T_{op} < T_{max}$		1		µV/°C
I_{ib}	Input bias current	T = 25°C TS507C full temp range TS507I full temp range		8	70 75 160	nA
I_{io}	Input offset current	T = 25°C TS507C full temp range TS507I full temp range		2	25 45 45	nA
CMRR	Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} from 0V to 1.5V		115		dB
A_{vd}	Large signal voltage gain	R_L = 10kΩ, V_{out}= 0.5V to 2.2V		126		dB
V_{CC}-V_{OH}	High level output voltage drop	R_L = 600Ω, T=25°C TS507C full temp range TS507I full temp range		57	85 100 105	mV
		R_L = 10kΩ, T=25°C Full temp range		4	15 15	
V_{OL}	Low level output voltage	R_L = 600Ω, T=25°C TS507C full temp range TS507I full temp range		57	80 100 115	mV
		R_L = 10kΩ, T=25°C Full temp range		4	15 15	
I_{out}	I_{sink}	V_{out} = V_{CC}, V_{id}=-1V, T=25°C TS507C full temp range TS507I full temp range	20 15 13	30		mA
	I_{source}	V_{out} = V_{DD}, V_{id}=1V, T=25°C TS507C full temp range TS507I full temp range	22 19 17	35		
I_{CC}	Supply current (per operator)(2)	No load, V_{out}=V_{CC}/2, V_{icm}=0 to 2.7V, T=25°C Full temp range		0.79	1.1 1.2	mA

Table 5. Electrical characteristics at V_{CC} = +2.7V V_{DD} = 0V, V_{icm} = V_{CC}/2, T_{amb} = 25°C, R_L connected to V_{CC}/2 (unless otherwise specified)(1) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dynamic performance						
GBP	Gain bandwidth product	R_L = 2kΩ, C_L = 100pF, f = 100kHz		1.9		MHz
ϕ_m	Phase margin	R_L = 2kΩ, C_L=100pF		45		Degrees
G_m	Gain margin	R_L = 2kΩ, C_L=100pF		11		dB
SR	Slew rate	R_L = 2kΩ, C_L=100pF, V_{out}= 0.5V to 2.2V, 10% to 90%		0.6		V/µs
e_N	Equivalent input noise voltage	f = 1kHz		12		nV/√Hz
THD+e_N	THD + noise	f=1KHz, G=1, R_L=2kΩ, V_{icm}=0.85V, V_{out}=1.2V_{pp}		0.0005		%

1. All parameter limits at temperatures different from 25° C are guaranteed by correlation.
2. Measurements done at 4 V_{icm} values: V_{icm}=0 V, V_{icm}=1.5 V, V_{icm}=1.9 V, V_{icm}=2.7 V.

Figure 1. Input offset voltage distribution for $V_{icm} \leq V_{CC}$-1.2V at T=25°C

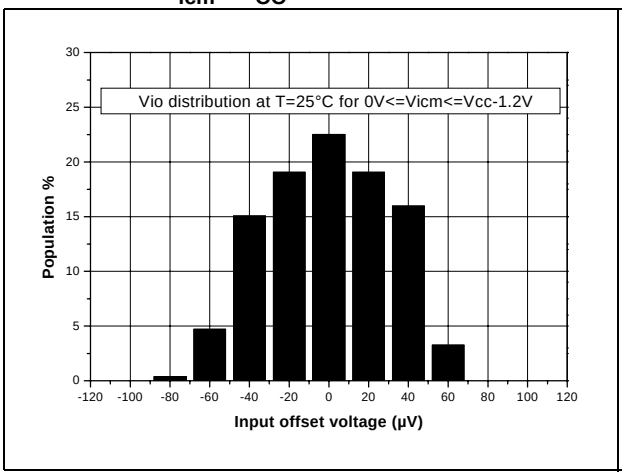


Figure 2. Input offset voltage distribution vs. temperature for $V_{icm} \leq V_{CC}$-1.2V

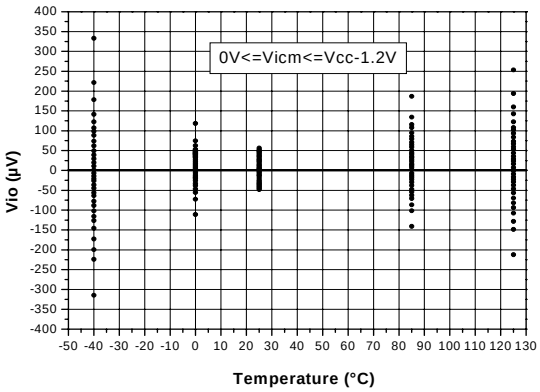


Figure 3. Input offset voltage distribution vs. temperature for $V_{icm} \geq V_{CC}$-0.8V

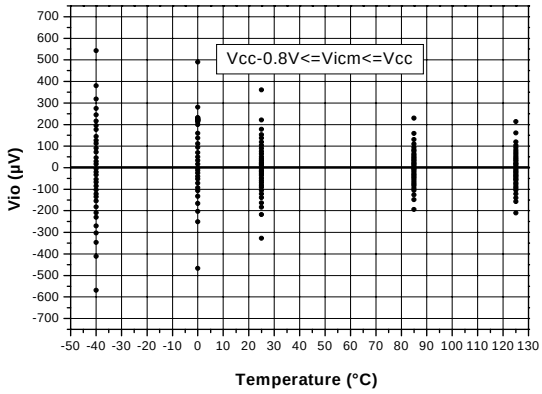


Figure 4. Input offset voltage distribution for $V_{icm} \leq V_{CC}$-1.2V at T=25°C after HTB

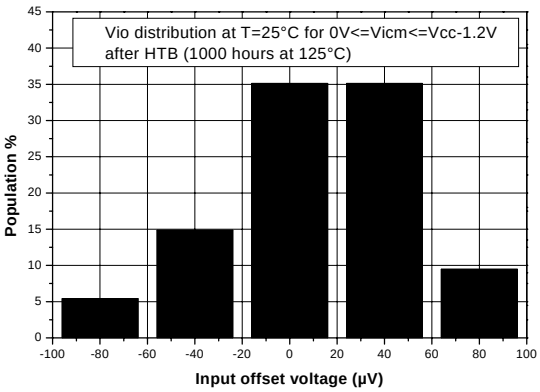


Figure 5. Input offset voltage distribution for $V_{icm} \leq V_{CC}$-1.2V at T=25°C after THB

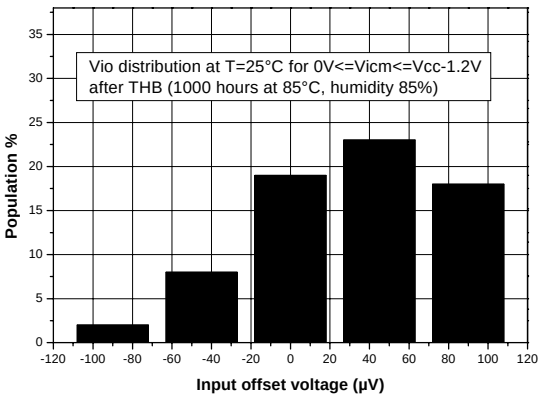


Figure 6. Input offset voltage vs. input common mode voltage at T=25°C

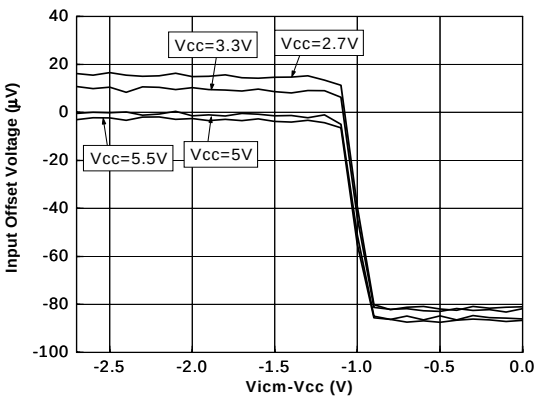


Figure 7. Supply current vs. input common mode voltage in closed loop configuration at V_{CC}=5V

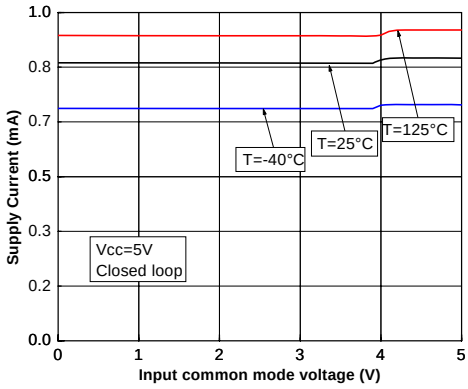


Figure 8. Supply current vs. supply voltage at $V_{icm}=V_{CC}/2$

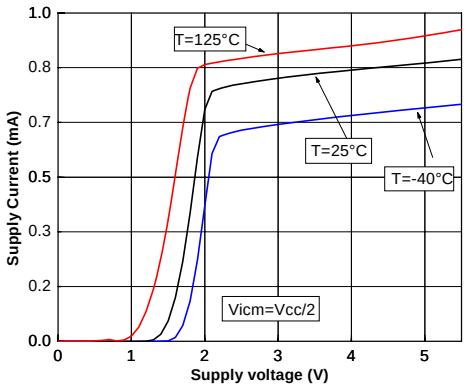


Figure 9. Supply current vs. input common mode voltage in follower configuration at V_{CC}=2.7V

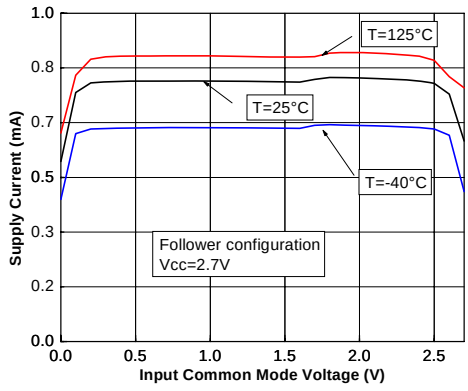


Figure 10. Supply current vs. input common mode voltage in follower configuration at V_{CC}=5V

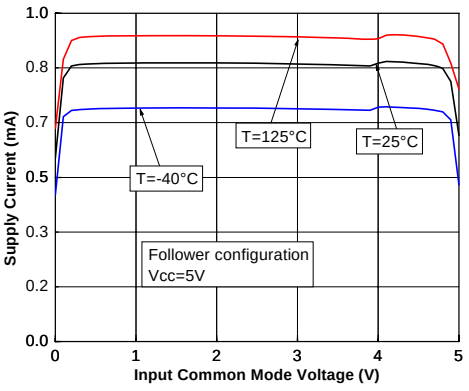


Figure 11. Output current vs. supply voltage at $V_{icm}=V_{CC}/2$

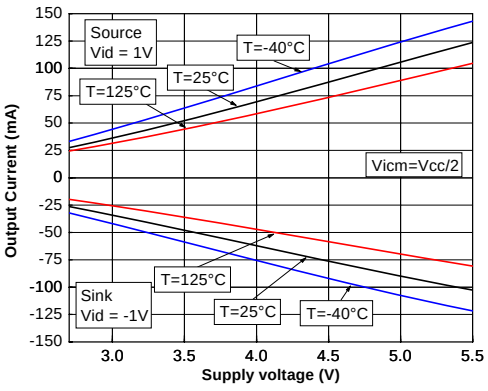


Figure 12. Output current vs. output voltage at V_{CC}=2.7V

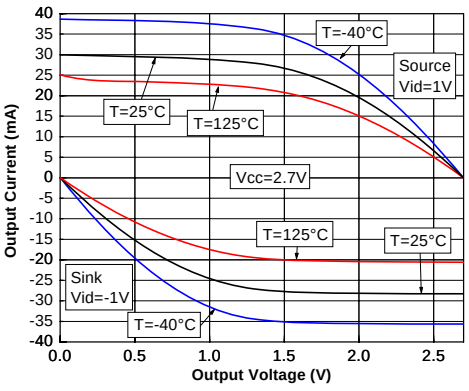


Figure 13. Output current vs. output voltage at V_{CC}=5V

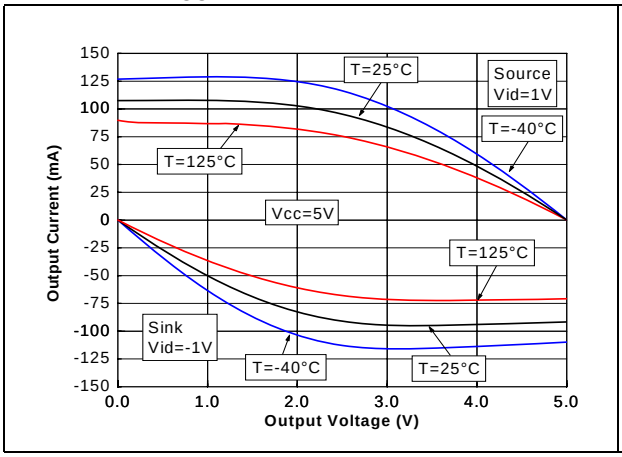


Figure 14. Positive and negative slew rate vs. supply voltage

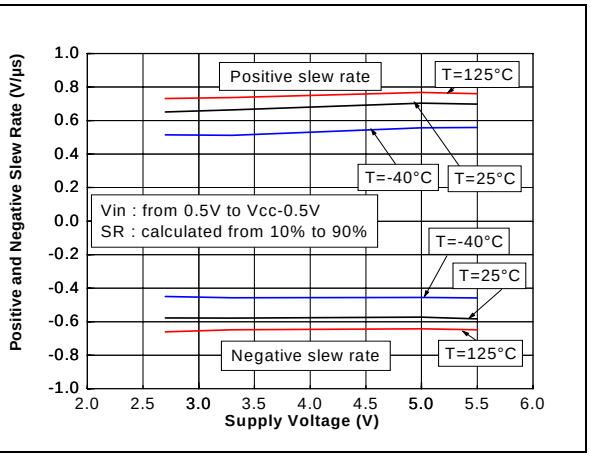


Figure 15. Voltage gain and phase vs. frequency at V_{CC}=5V and V_{icm}=2.5V at T=25°C

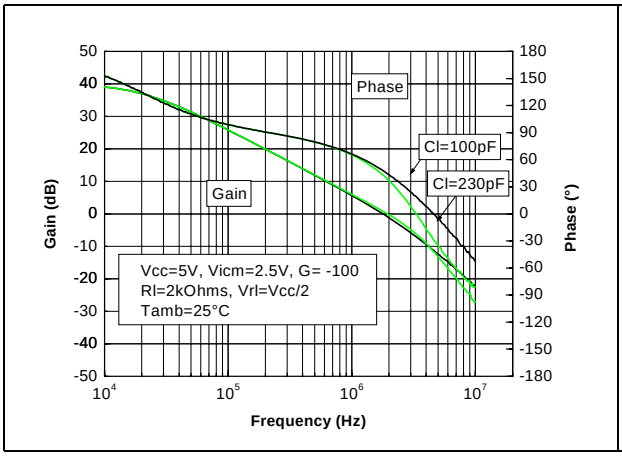


Figure 16. Voltage gain and phase vs. frequency at V_{CC}=5V and V_{icm}=2.5V at T=-40°C

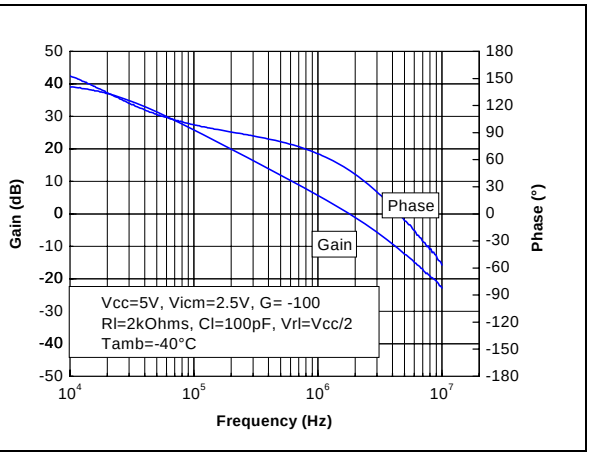


Figure 17. Voltage gain and phase vs. frequency at V_{CC}=5V and V_{icm}=2.5V at T=125°C

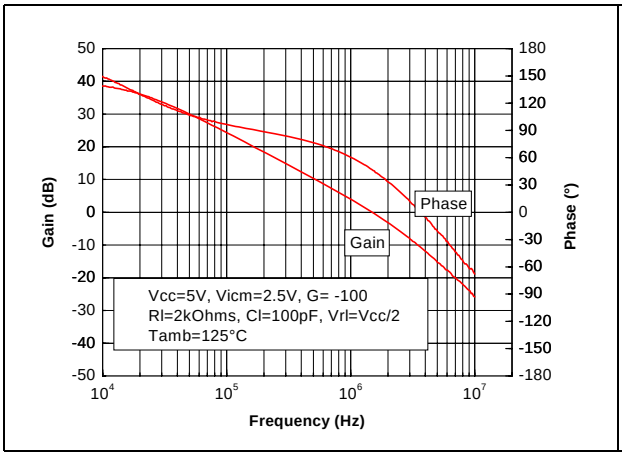


Figure 18. Closed loop gain in voltage follower configuration for different capacitive load at T=25°C

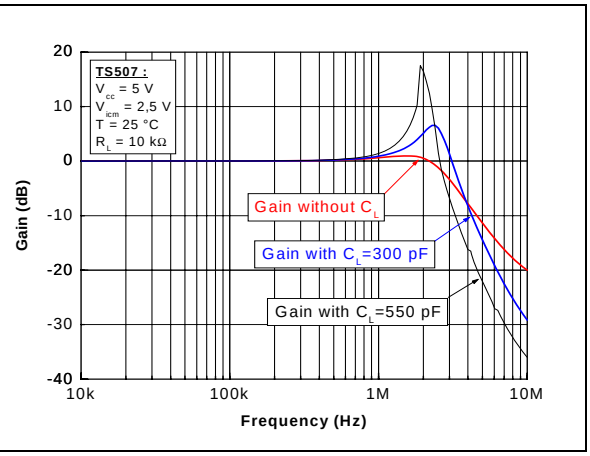


Figure 19. Gain margin according the output load, at V_{CC}=5V and T=25°C

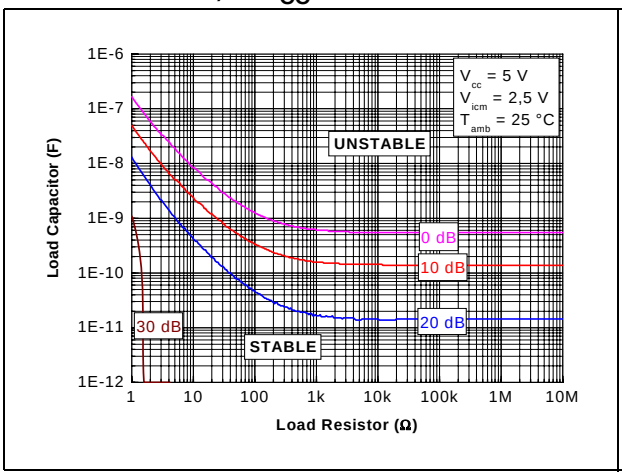


Figure 20. Phase margin according the output load, at V_{CC}=5V and T=25°C

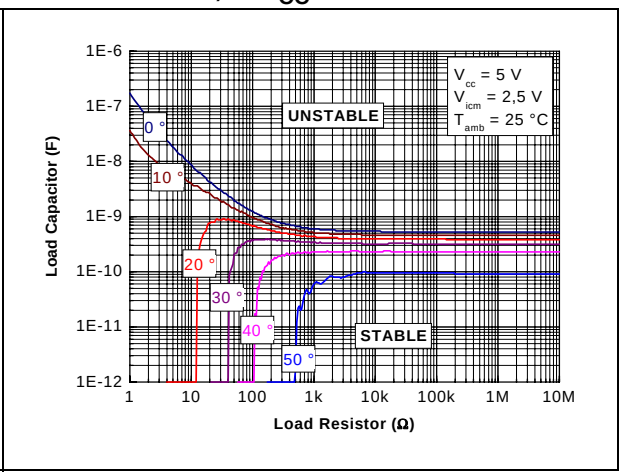


Figure 21. Gain margin vs. output current, at V_{CC}=5V and T=25°C

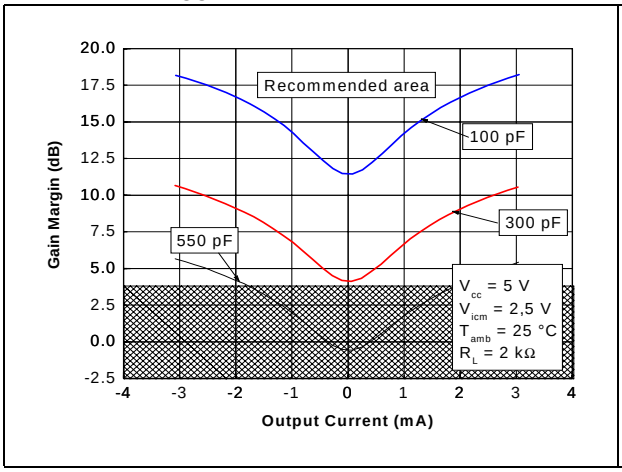


Figure 22. Phase margin vs. output current, at V_{CC}=5V and T=25°C

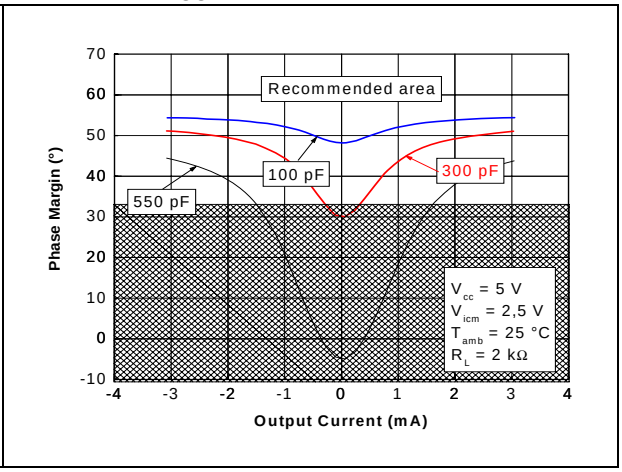


Figure 23. Phase and gain margins vs capacitive load at = 25°C

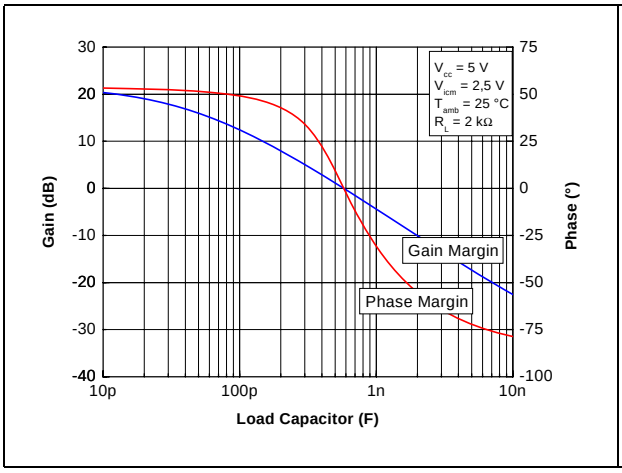


Figure 24. Distortion + noise vs. output voltage

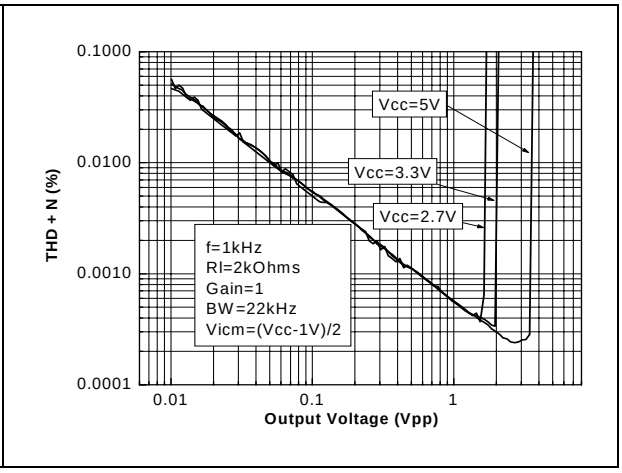


Figure 25. Distortion + noise vs. frequency

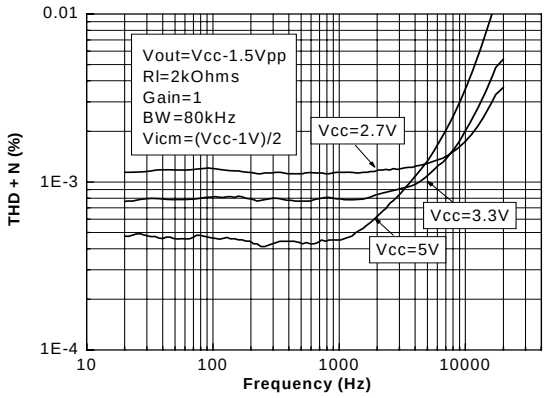
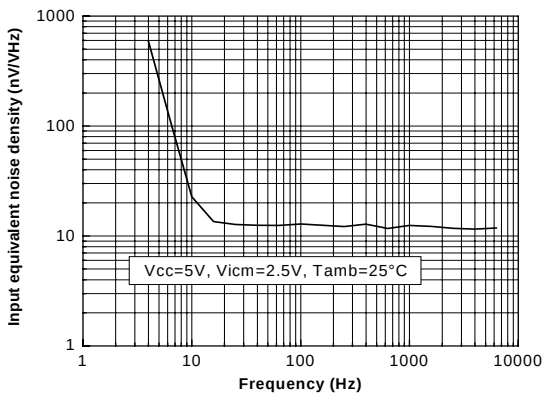


Figure 26. Noise vs. frequency



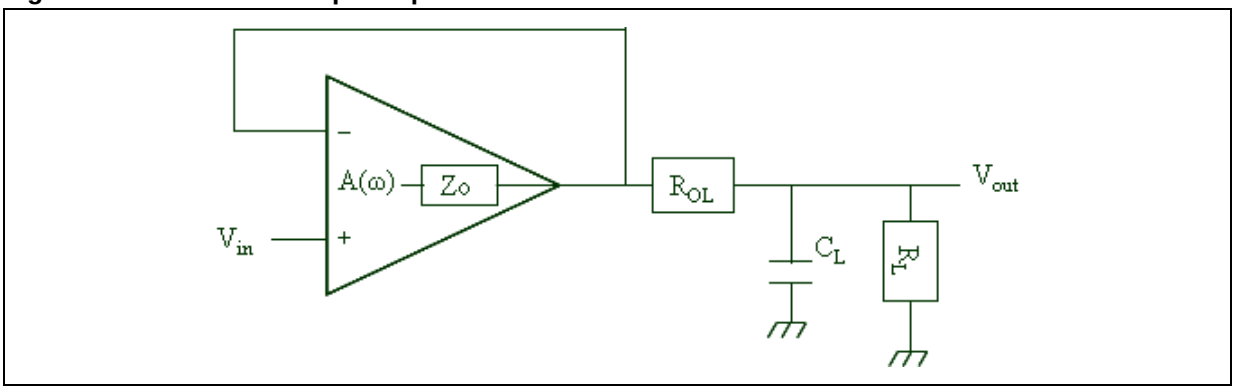
3 Application note

An application note, based on the TS507, describes three compensation techniques for solving stability issues when driving large capacitive loads. Two of them are briefly explained here. For more details, refer to the application note on *www.st.com*. To find it, do a keyword search for **AN2653**.

3.1 Out-of-the-loop compensation technique

The first technique, named the **out-of-the-loop** compensation, uses an isolation resistor, R_{OL}, added in series between the output of the amplifier and its load (see *Figure 27*). The resistor isolates the op-amp feedback network from the capacitive load. This compensation method is effective, but the drawback is a limitation on the accuracy of V_{out} depending on the resistive load value.

Figure 27. Out-of-the-loop compensation schematics



To help implement the compensation, the abacus given in *Figure 28* to *Figure 29* provide the R_{OL} value to choose for a given C_L and phase/gain margins. These abacus are plotted in the case of a voltage follower configuration with a load resistor of 10 kΩ at 25°C.

Figure 28. Gain margin abacus : serial resistor to be added in a voltage follower configuration at 25°C

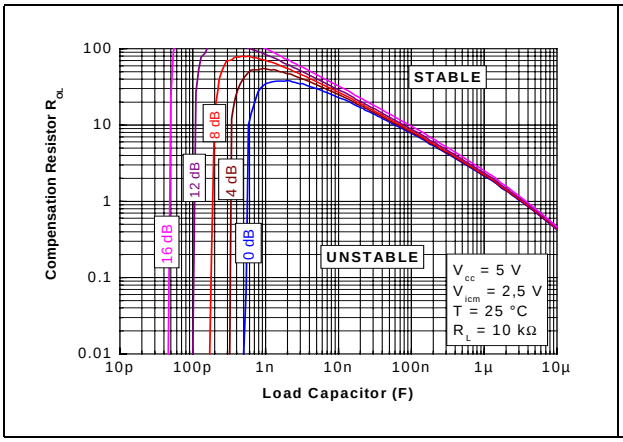
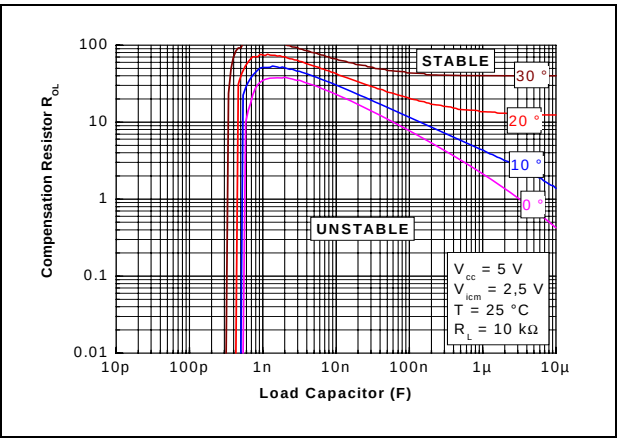


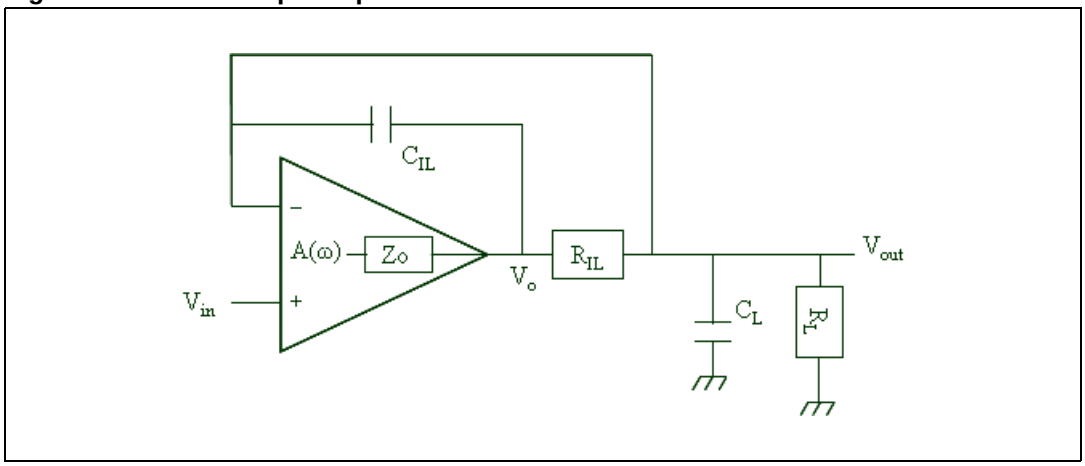
Figure 29. Phase margin abacus : serial resistor to be added in a voltage follower configuration at 25°C



3.2 In-the-loop-compensation technique

The second technique is called the **in-the-loop-compensation** technique, because the additional components (a resistor and a capacitor) used to improve the stability are inserted in the feedback loop (see *Figure 30*).

Figure 30. In-the-loop compensation schematics



This compensation method allows, by a good choice of compensation components, to compensate the original pole (caused by the capacitive load), and thus to improve stability.

The main drawback of this circuit is the reduction of the output swing, because the isolation resistor is in the signal path.

Table 6 helps you to choose the best compensation components for different ranges of load capacitors (and with R_L = 10 kΩ) in voltage follower configuration.

Table 6. Best compensation components for different load capacitor ranges in voltage follower configuration for TS507 (with R_L = 10 kΩ)

Load capacitor range	R_{IL} (kΩ)	C_{IL} (pF)	Minimum gain margin (dB)(1)	Minimum phase margin (degree)(1)
10 pF to 100 pF	1	250	17	55
100 pF to 1 nF	1	250	16	42
1 nF to 10 nF	1	630	11	27

1. Parameter guaranteed by design at 25°C.

4 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

4.1 SOT23-5 package information

Figure 31. SOT23-5 package mechanical drawing

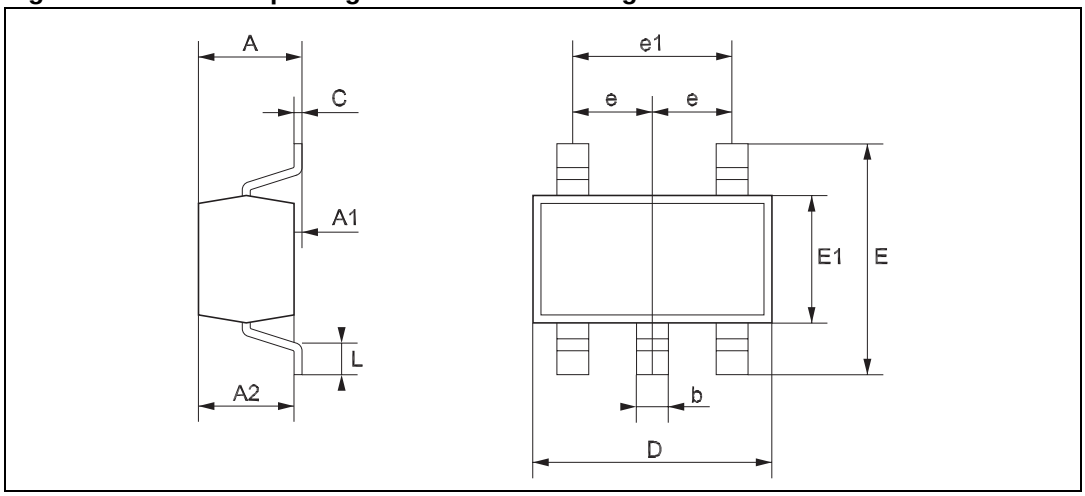


Table 7. SOT23-5 package mechanical data

Ref.	Dimensions					
	Millimeters			Mils		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.00		5.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e		0.95			37.4	
e1		1.9			74.8	
L	0.35		0.55	13.7		21.6

4.2 SO-8 package

Figure 32. SO-8 package mechanical drawing

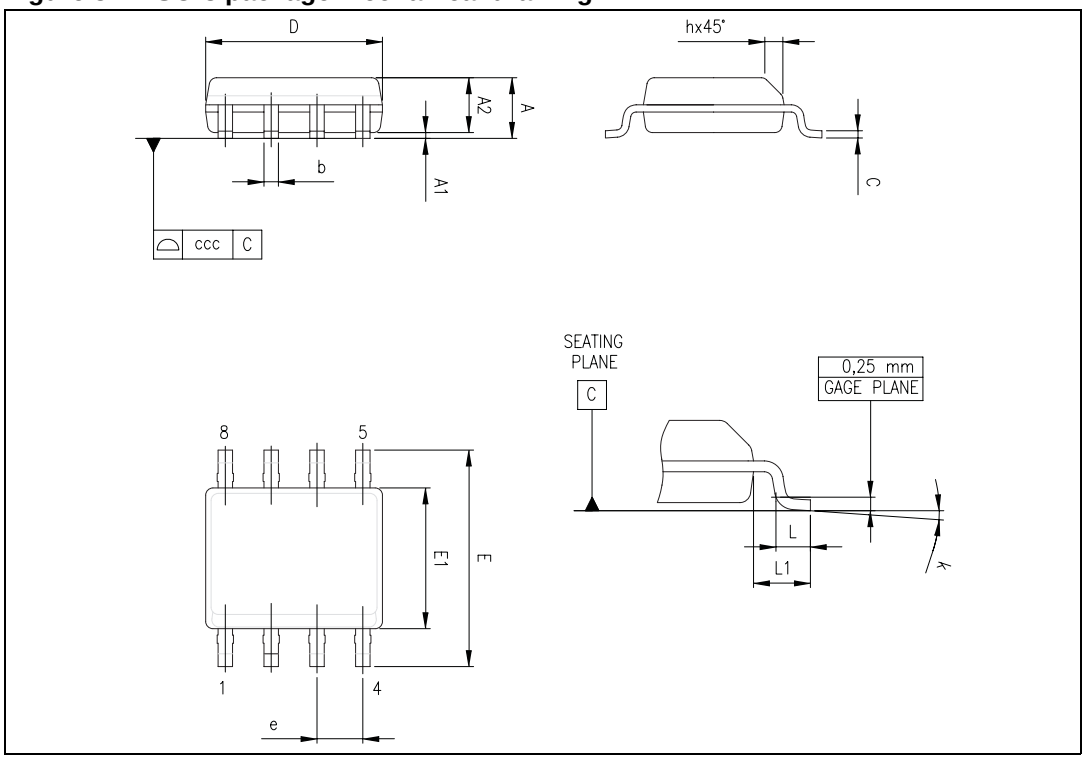


Table 8. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004

5 Ordering information

Table 9. Order codes

Order code	Temperature range	Package	Packing	Marking
TS507ID TS507IDT	-40°C to 125°C	SO-8	Tube or Tape & reel	TS507I
TS507IYD(1) TS507IYDT(1)		SO-8 (Automotive grade)		TS507Y
TS507ILT	-40°C to 125°C	SOT23-5(2)	Tape & reel	K131
TS507IYLT(1)		SOT23-5(2) (Automotive grade)	Tape & reel	K137
TS507CD TS507CDT	0°C to 85°C	SO-8	Tube or Tape & reel	TS507C
TS507CLT		SOT23-5(2)	Tape & reel	K136

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.
2. All information related to the SOT23-5 package is subject to change without notice.

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Oct-2004	1	Preliminary data release for product in development.
02-May-2006	2	Update preliminary data release for product in development.
15-Dec-2006	3	First public release.
03-May-2007	4	Automotive grade products added.
08-Apr-2008	5	Electrical characteristics curves for Bode and AC stability added and updated. Application note section added.

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