TDA3330

TV COLOR PROCESSOR

This device will accept a PAL or NTSC composite video signal and output the three color signals, needing only a simple driver amplifier to interface to the picture tube.

Its simplified approach makes it particularly suitable for low cost CTV systems.

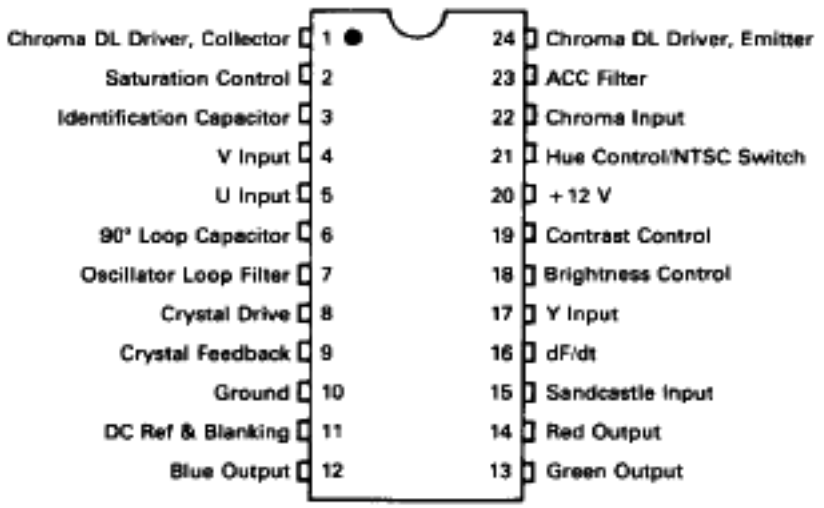
- No Oscillator Adjustment Required
- Four dc High Impedance User Controls
- Uses Inexpensive 4.43/3.58 MHz Crystals
- Interfaces With TDA3030B SECAM Adaptor
- Uses Horizontal Flyback or Super Sandcastle Pulse
- Single 12 V Supply
- Low Dissipation

TV COLOR PROCESSOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 724

FIGURE 1 — PIN ASSIGNMENT



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MAXIMUM RATINGS (T_A = +25°C unless otherwise stated)

Rating	Pin	Value	Unit
Supply Voltage	20	14	Vdc
Operating Temperature Range		0 to +70	°C
Storage Temperature Range		−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	20	10.8	12	13.2	V
Supply Current		—	—	50	mA
Composite Video Input	17	—	1.0	—	Vp-p
Video Input Resistance					
Burst Gate On		—	5.0	—	kΩ
Burst Gate Off		—	1.5	—	MΩ
Chroma Input (Burst)	22	10	100	200	mVp-p
Input Resistance	22	—	5.0	—	kΩ
ACC Effectiveness	1	−1.5	0	+1.5	dB
Luminance Gain between Pin 17 and Outputs (Contrast max)		—	8.0	—	
Luminance Bandwidth (−3.0 dB)	12, 13, 14	—	5.0	—	MHz
Output Resistance		—	170	—	Ω
Residual Carrier (4.43 MHz)		—	—	200	mVp-p
PAL Offset (H/2)		—	—	50	mVp-p
U Input Sensitivity for 5.0 V Blue Output	5	—	340	—	mVp-p
Matrix Error	12, 13, 14	—	—	10	%
Oscillator Capture Range		300	500	—	Hz
U Reference Phase Error		—	—	5.0	Degrees
V Reference Phase Error		—	—	5.0	Degrees
Color Kill Attenuation	12, 13, 14	50	—	—	dB
Contrast Tracking Luma/Chroma	12, 13, 14	—	0	2.0	dB
Sandcastle Slice Level	15				
Burst Gate		—	7.2	8.0	V
Line Blanking		0.5	1.5	2.5	V
R Input $V_{15} > 7.0$ V		—	5.0	—	kΩ
$V_{15} < 7.0$ V		—	10	—	kΩ

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INPUT/OUTPUT FUNCTIONS

FIGURE 2 — BRIGHTNESS CONTROL

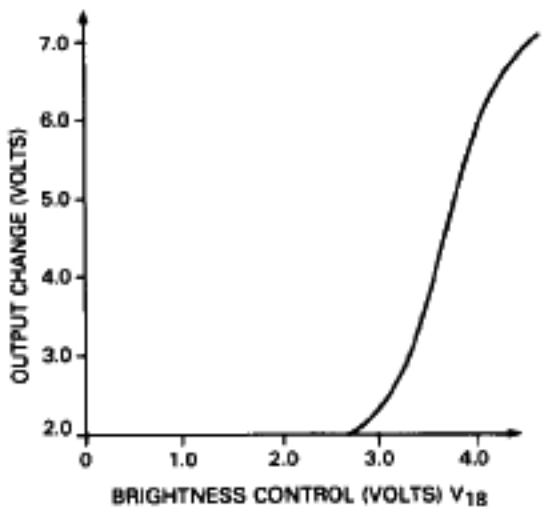
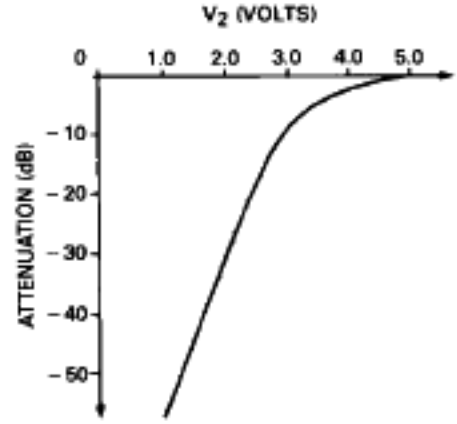


FIGURE 3 — SATURATION CONTROL VOLTAGE



Pin 2 is automatically pulled to ground with a mis-identified PAL signal.

Note: Nominal 100% saturation point is given by choice of $R_{pin\ 23}$ which sets ACC operating point.

FIGURE 4 — CONTRAST CONTROL

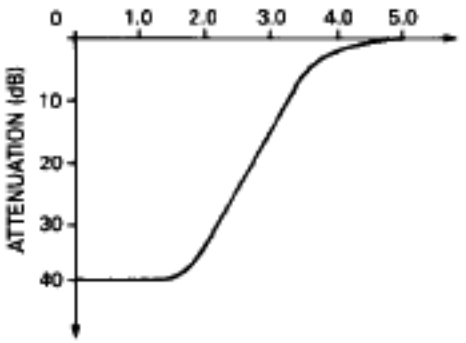
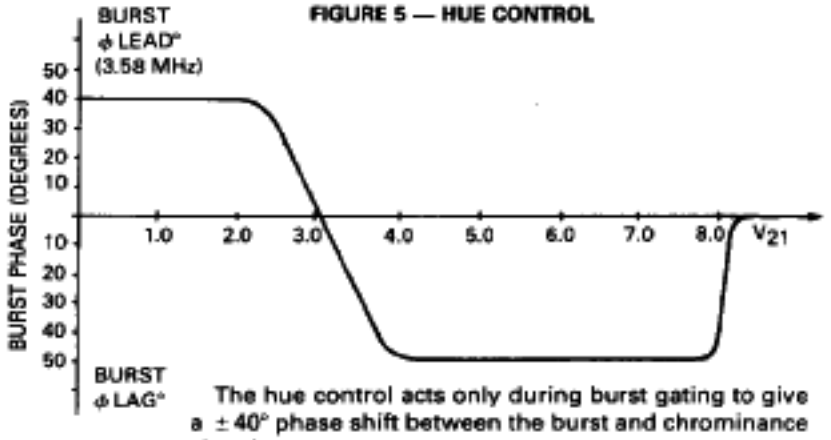


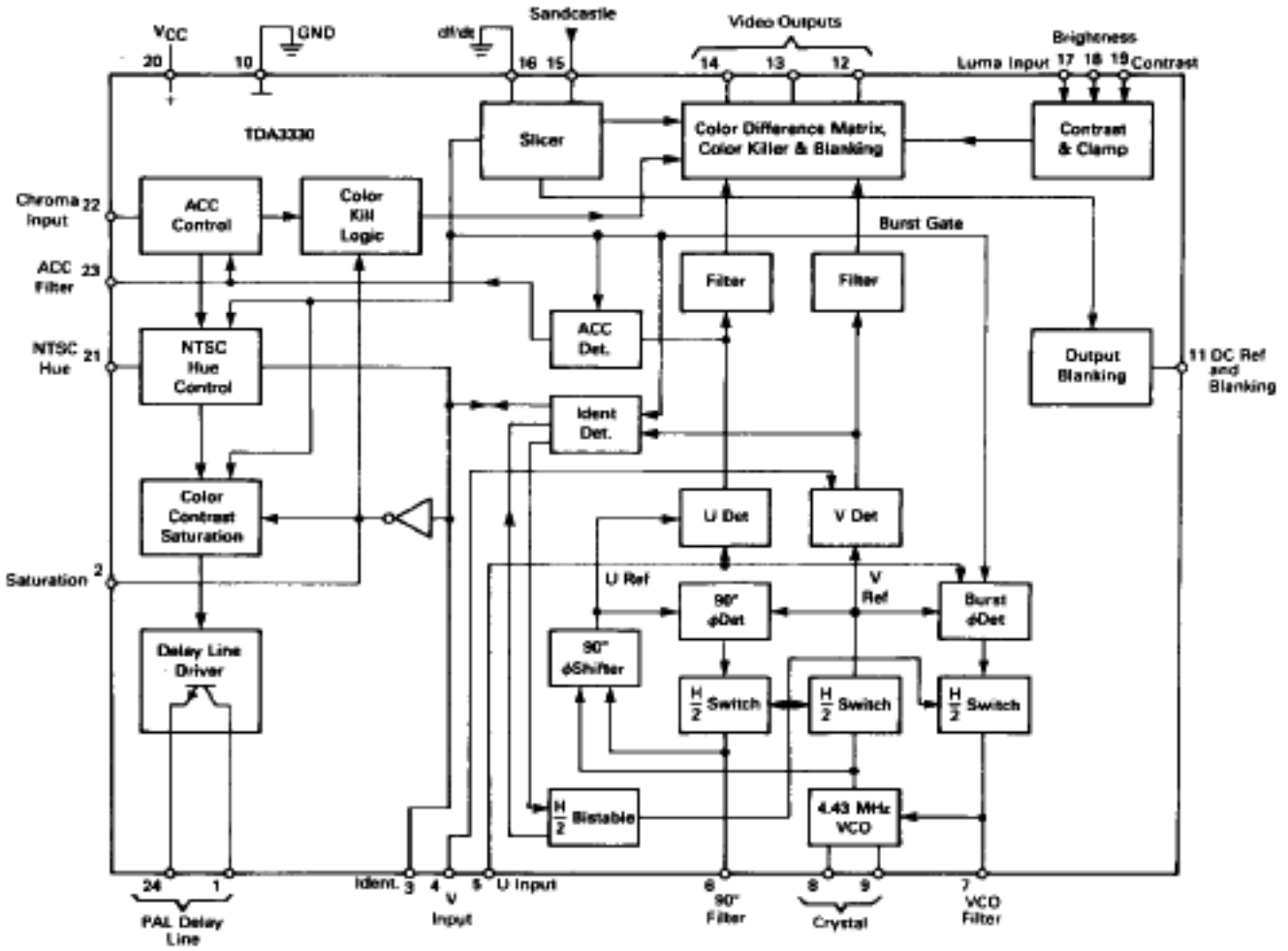
FIGURE 5 — HUE CONTROL



The hue control acts only during burst gating to give a ±40° phase shift between the burst and chrominance signal.

Pin 21 is also used to select NTSC when $V_{21} < 8.0$ V and thus the control will operate only in this mode. NTSC selection means the PAL phase switching is turned off. Delay-line and filter switching must be implemented externally.

FIGURE 6 — BLOCK DIAGRAM



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CIRCUIT OPERATION

CHROMINANCE DECODER SECTION

The chrominance decoder section of the TDA3330 consists of the following blocks:

Phase-locked reference oscillator — Figures 7, 8 and 9
Phase-locked 90 degree servo loop — Figures 9 and 10
U and V axis decoders
ACC detector and identification detector — Figure 11
Identification circuits and PAL bistable — Figure 12
Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

- — a minimum number of factory adjustments
- — a minimum number of external components
- — compatibility with the SECAM adapter TDA3030B
- — low dissipation
- — use of a standard 4.433618 MHz crystal rather than a 2.0 fc crystal with divider, (or standard 3.579545 MHz for NTSC).

REFERENCE REGENERATION

The crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. Much care was taken to ensure that the oscillator loop gain and the crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade crystals (crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

By referring to Figures 7 and 8 it can be seen that the necessary ±45° phase shift is obtained by variable addition of two currents I_1 and I_2 which are then fed into the load resistance of the crystal tuned circuit R_1. Feedback is taken from the crystal load capacitance which gives a voltage VF lagging the crystal current by 90°.

The RC network in Q1 collector causes I_1 to lag the collector current of Q1 by 45°.

For SECAM operation the currents I_1 and I_2 are added together in a fixed ratio giving a frequency close to nominal.

When decoding PAL there are two departures from normal chroma reference regeneration practice:

a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal noise ratio is gained but more important is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification.

FIGURE 7 — VOLTAGE CONTROLLED OSCILLATOR (VCO)

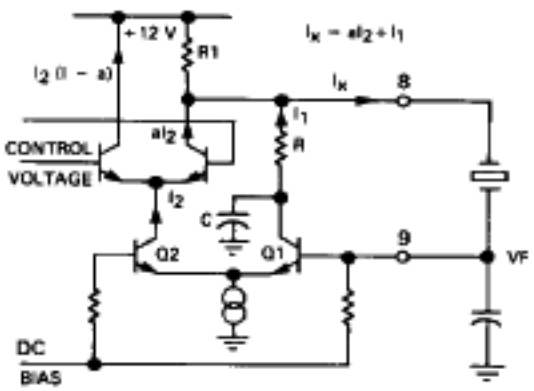
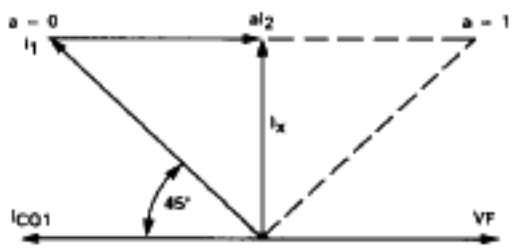


FIGURE 8 — VECTOR DIAGRAM FOR VCO



b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not DC. A commutator at the phase detector output also driven from the PAL bistable converts this AC signal to a DC prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC this cannot be considered to be serious disadvantage.

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90° REFERENCE GENERATION

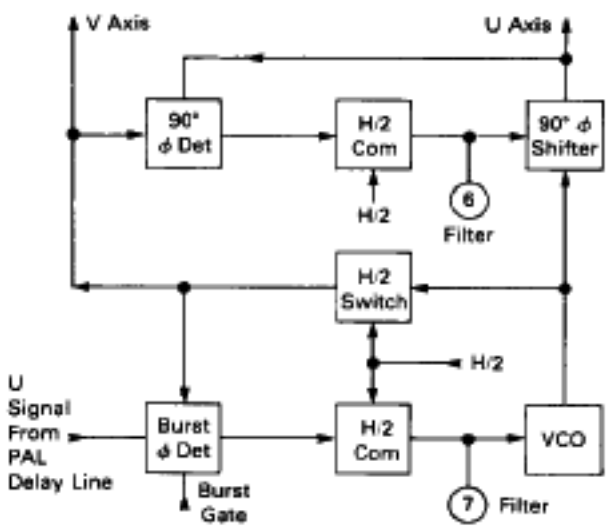
To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the variable all-pass network. (See Figure 10.)

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation with TDA3030B the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B adapter.

FIGURE 9 — BLOCK DIAGRAM OF REFERENCE SECTION



ACC AND IDENTIFICATION DETECTORS

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

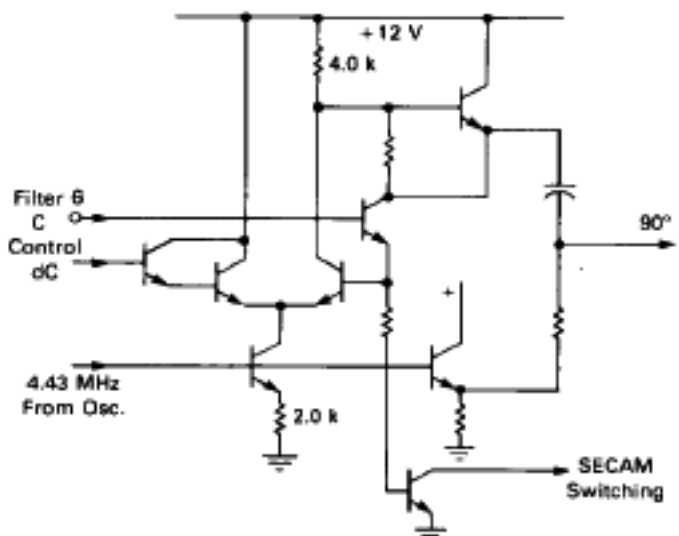
IDENTIFICATION

See Figure 12 for definitions.

Monochrome	$I_1 > I_2$
PAL ident. OK	$I_1 < I_2$
PAL ident. X	$I_1 > I_2$
NTSC	$I_3 > I_2$

Only for correctly identified PAL signal is the capacitor voltage held low since I_2 is then greater than I_1.

FIGURE 10 — VARIABLE ALL-PASS NETWORK



For monochrome and incorrectly identified PAL signals $I_1 > I_2$ hence voltage V_C rises with each burst gate pulse.

When $V_{ref}1$ is exceeded by 0.7 V latch 1 is made conducting which increases rate of voltage rise on C. Maximum current is limited by R_1.

When $V_{ref}2$ is exceeded by 0.7 V then latch 2 is made conducting until C is completely discharged and the current drops to a value insufficient to hold on latch 2.

As latch 2 turns on latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

The inhibit line on latch 2 restricts latch 2 conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing latch 2 in the correct phase for SECAM. For NTSC latch 2 is fired by current (I_3) injected into Pin 3 by the NTSC switch. This is supplied internally when V_{21} falls below 8.0 V.

If the voltage on C is greater than 1.4 V then the saturation is held down. Only for SECAM/NTSC with latch 2 on or correctly identified PAL can the saturation control be anywhere but minimum.

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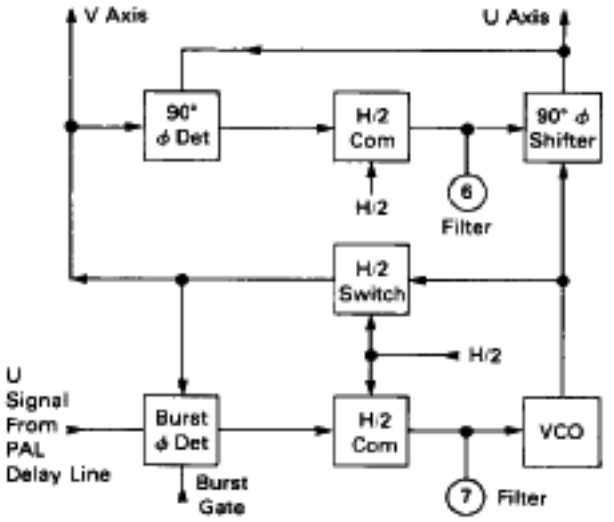

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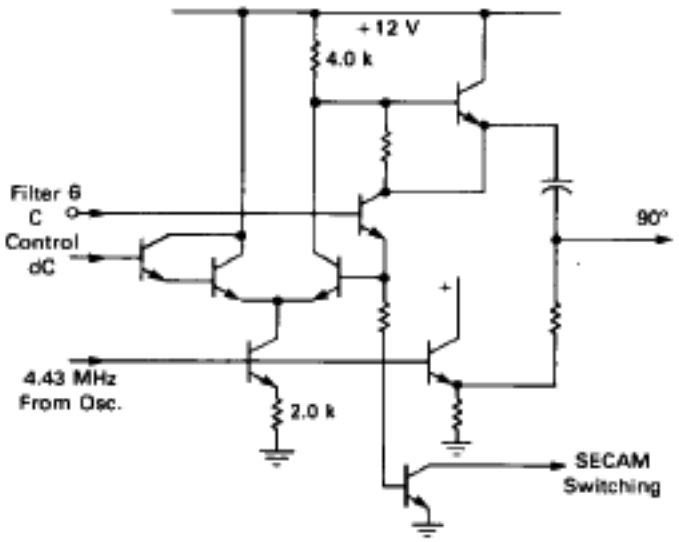

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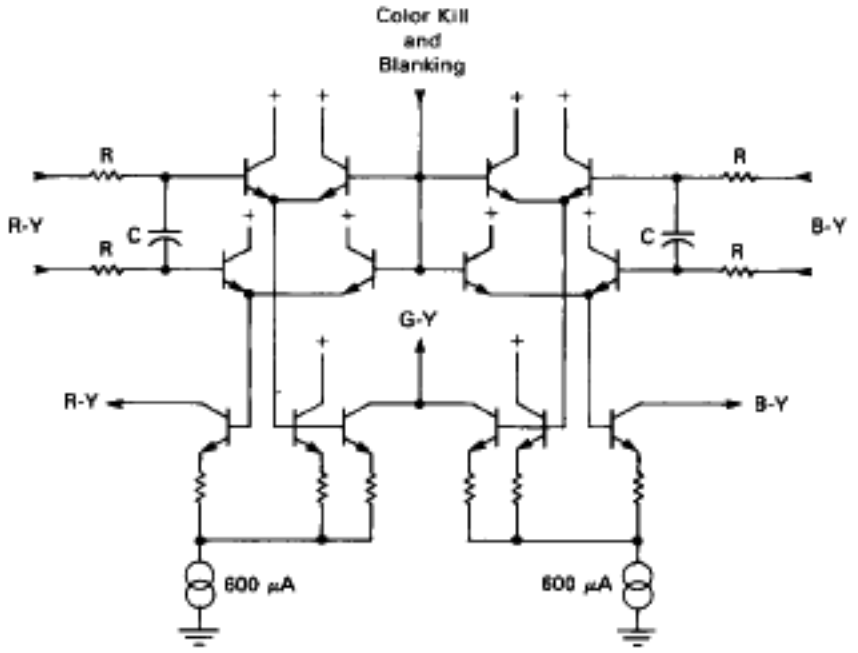
FIGURE 13 — COLOR DIFFERENCE STAGES



SANDCASTLE SECTION

The input signal is sliced at 2 levels, 1.5 V and 7.2 V. Above 1.5 V is used for blanking, above 7.2 V for burst gating provided level on Pin 16 is below 0.7 V. If a normal Sandcastle is used, it is recommended to ground the Pin 16. This input is used to inhibit the burst gate. This is used if a true Sandcastle is not available; in this case horizontal flyback may be used instead and differentiated flyback applied to the $\frac{df}{dt}$ pin (input resistance 1.0 kΩ).

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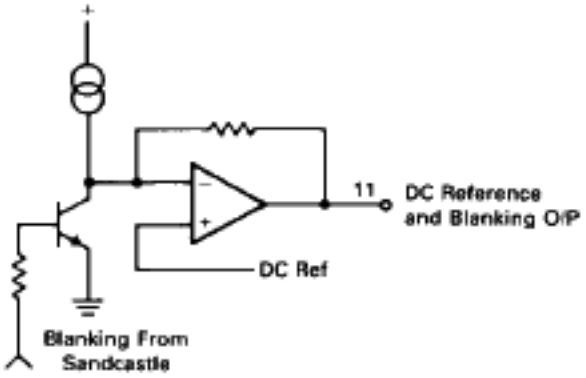
FIGURE 14 — DC REFERENCE AND BLANKING SECTION



The DC Reference and Blanking section is used to bias the Video output stages. The temperature coefficient is arranged to be a V_{BE} drift less than the Red, Green and Blue outputs.

FIGURE 15 — TYPICAL PAL APPLICATION

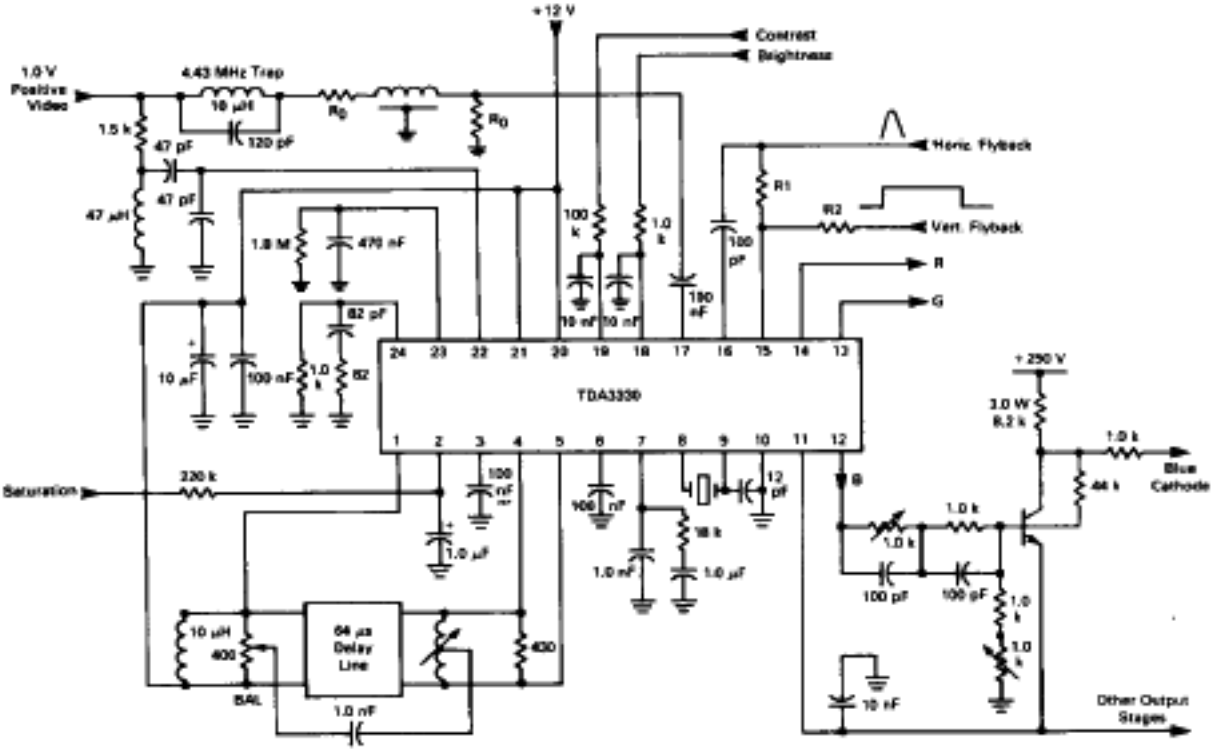
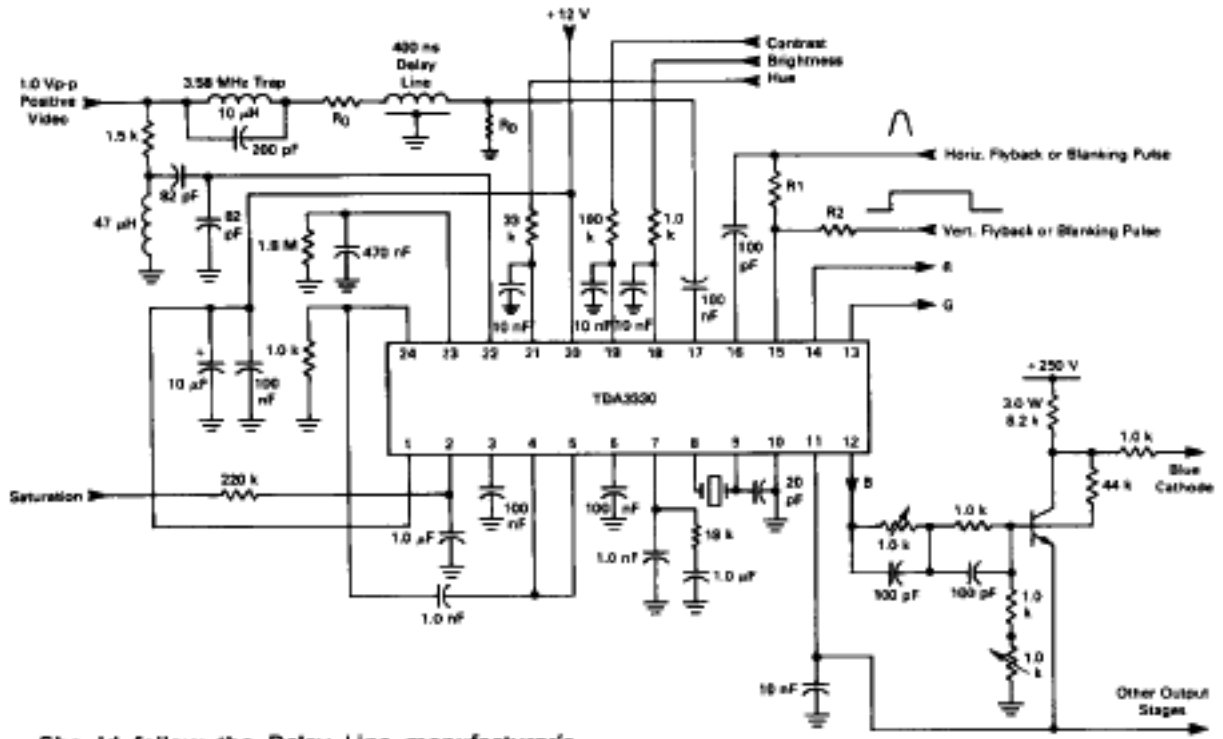


FIGURE 16 — TYPICAL NTSC APPLICATION



R_0 — Should follow the Delay Line manufacturer's recommendations.

R_1 — Should be selected to give approximately 10–12 V pulse at Pin 15 (approximately 5.0 k internal resistance).

R_2 — Should be selected to give approximately 4.0 to 5.0 V pulse at Pin 15 (approximately 10 k internal resistance).