TPIC5223L 2-CHANNEL INDEPENDENT GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

SLIS043A - NOVEMBER 1994 - REVISED SEPTEMBER 1995

- Low r_{DS(on)} . . . 0.38 Ω Typ
 Voltage Output . . . 60 V
- Input Protection Circuitry . . . 18 V
- Pulsed Current . . . 3 A Per Channel
- Extended ESD Capability . . . 4000 V
- Direct Logic-Level Interface

GND [1 8] DRAIN1 SOURCE1 [2 7] GATE1 GATE2 [3 6] SOURCE2 DRAIN2 [4 5] NC

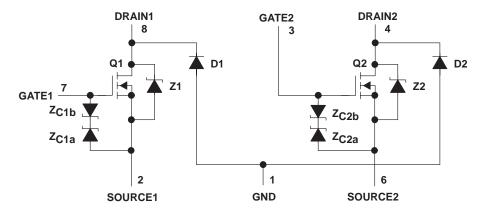
NC - No internal connection

description

The TPIC5223L is a monolithic gate-protected logic-level power DMOS array that consists of two electrically isolated independent N-channel enhancement-mode DMOS transistors. Each transistor features integrated high-current zener diodes (Z_{CXa} and Z_{CXb}) to prevent gate damage in the event that an overstress condition occurs. These zener diodes also provide up to 4000 V of ESD protection when tested using the human-body model of a 100-pF capacitor in series with a 1.5-k Ω resistor.

The TPIC5223L is offered in a standard eight-pin small-outline surface-mount (D) package and is characterized for operation over the case temperature of -40° C to 125° C.

schematic



NOTE A: For correct operation, no terminal may be taken below GND.

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SLIS043A – NOVEMBER 1994 – REVISED SEPTEMBER 1995

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V _{DS}	60 V
Source-to-GND voltage	100 V
Drain-to-GND voltage	100 V
Gate-to-source voltage range, V _{GS}	–9 V to 18 V
Continuous drain current, each output, T _C = 25°C	1 A
Continuous source-to-drain diode current, T _C = 25°C	
Pulsed drain current, each output, I _{max} , T _C = 25°C (see Note 1 and Figure 15)	3 A
Continuous gate-to-source zener diode current, T _C = 25°C	±50 mA
Pulsed gate-to-source zener-diode current, T _C = 25°C	±500 mA
Single-pulse avalanche energy, E_{AS} , $T_{C} = 25^{\circ}C$ (see Figures 4 and 16)	108 mJ
Continuous total power dissipation, T _C = 25°C (see Figure 15)	0.95 W
Operating virtual junction temperature range, T _J	40°C to 150°C
Operating case temperature range, T _C	40°C to 125°C
Storage temperature range, T _{stq}	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%



TPIC5223L 2-CHANNEL INDEPENDENT GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY SLIS043A – NOVEMBER 1994 – REVISED SEPTEMBER 1995

electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER	TEST COND	MIN	TYP	MAX	UNIT	
V(BR)DSX	Drain-to-source breakdown voltage	$I_D = 250 \mu A$,	$V_{GS} = 0$	60			V
VGS(th)	Gate-to-source threshold voltage	I _D = 1 mA, See Figure 5	V _{DS} = V _{GS} ,	1.5	2.05	2.2	٧
V _(BR) GS	Gate-to-source breakdown voltage	I _{GS} = 250 μA		18			V
V _(BR) SG	Source-to-gate breakdown voltage	I _{SG} = 250 μA		9			V
V _(BR)	Reverse drain-to-GND breakdown voltage (across D1, D2)	Drain-to-GND curren	t = 250 μA	100			V
V _{DS(on)}	Drain-to-source on-state voltage	I _D = 1 A, See Notes 2 and 3	V _{GS} = 5 V,		0.375	0.425	V
VF(SD)	Forward on-state voltage, source-to-drain	I _S = 1 A, V _{GS} = 0 (Z1, Z2), See Notes 2 and 3 and Figure 12			0.85	1.2	V
VF	Forward on-state voltage, GND-to-drain	I _D = 1 A (D1, D2), See Notes 2 and 3			3		V
	Zero-gate-voltage drain current	V _{DS} = 48 V, V _{GS} = 0	T _C = 25°C		0.05	1	μΑ
IDSS			T _C = 125°C			10	
IGSSF	Forward-gate current, drain short circuited to source	V _{GS} = 15 V,	$V_{DS} = 0$		20	200	nA
IGSSR	Reverse-gate current, drain short circuited to source	$V_{SG} = 5 V$,	$V_{DS} = 0$		10	100	nA
lu	Leakage current, drain-to-GND	V _{DGND} = 48 V	T _C = 25°C		0.05	1	μА
likg	Leakage current, drain-to-OND	VDGND = 40 V	T _C = 125°C		0.5	10	μΛ
[DC(***)	Static drain-to-source on-state resistance	V _{GS} = 5 V, I _D = 1 A,	T _C = 25°C		0.38	0.43	Ω
rDS(on)	otatic drain to source on state resistance	See Notes 2 and 3 and Figures 6 and 7	T _C = 125°C		0.61	0.65	32
9fs	Forward transconductance	V _{DS} = 15 V, See Notes 2 and 3 a	I _D = 500 mA, nd Figure 9	1.2	1.49		S
C _{iss}	Short-circuit input capacitance, common source				150	190	
Coss	Short-circuit output capacitance, common source	$V_{DS} = 25 \text{ V},$	$V_{GS} = 0$,		100	125	pF
C _{rss}	Short-circuit reverse transfer capacitance, common source	f = 1 MHz,	See Figure 11		40	50	рі

NOTES: 2. Technique should limit T_J – T_C to 10°C maximum.

source-to-drain and GND-to-drain diode characteristics, $T_C = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT	
	Povorce recovery time			Z1 and Z2		50		20	
t _{rr} Reverse-recovery time		I _S = 500 mA, V _{GS} = 0, See Figures 1 and 14	$di/dt = 100 A/\mu s$,	D1 and D2		210		ns	
Opp. Total diodo charge	Z1 and Z2				50		nC		
Q _{RR}	Total diode charge			D1 and D2		800		IIC	

^{3.} These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

TPIC5223L 2-CHANNEL INDEPENDENT GATE-PROTECTED LOGIC-LEVEL POWER DMOS ARRAY

SLIS043A - NOVEMBER 1994 - REVISED SEPTEMBER 1995

resistive-load switching characteristics, T_C = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _d (on)	Turn-on delay time			34	70	
td(off)	Turn-off delay time	$V_{DD} = 25 \text{ V}, R_L = 50 \Omega, t_{r1} = 10 \text{ ns},$		20	40	no
t _{r1}	Rise time	t _{f1} = 10 ns, See Figure 2		28	55	ns
t _{f2}	Fall time			15	30	
Qg	Total gate charge			3.1	3.8	
Q _{gs(th)}	Threshold gate-to-source charge	$V_{DS} = 48 \text{ V}$, $I_{D} = 500 \text{ mA}$, $V_{GS} = 5 \text{ V}$, See Figure 3		0.5	0.6	nC
Q _{gd}	Gate-to-drain charge	occ riguic o		1.9	2.3	
LD	Internal drain inductance			5		nH
LS	Internal source inductance			5		ш
Rg	Internal gate resistance			0.25		Ω

thermal resistance

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	See Notes 4 and 7	130		
$R_{\theta JB}$	Junction-to-board thermal resistance	See Notes 5 and 7	78.6		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance	See Notes 6 and 7	34		

NOTES: 4. Package mounted on an FR4 printed-circuit board with no heatsink.

- 5. Package mounted on a 24 in², 4-layer FR4 printed-circuit board.
- 6. Package mounted in intimate contact with infinite heatsink.
- 7. All outputs with equal power

PARAMETER MEASUREMENT INFORMATION

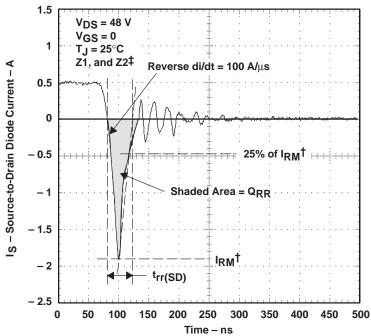


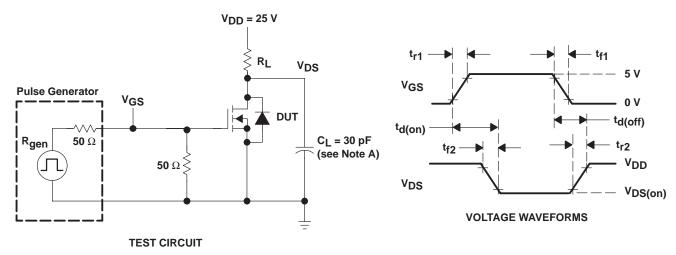
Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



[†] I_{RM} = maximum recovery current ‡ The above waveform is representative of D1 and D2 in shape only.

SLIS043A - NOVEMBER 1994 - REVISED SEPTEMBER 1995

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

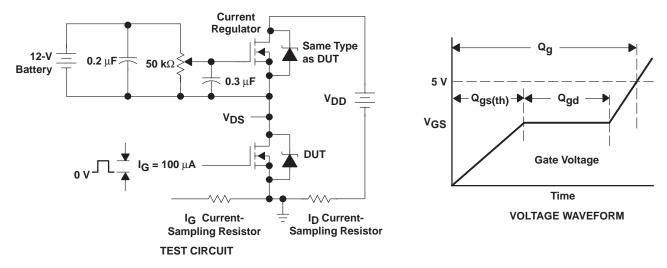
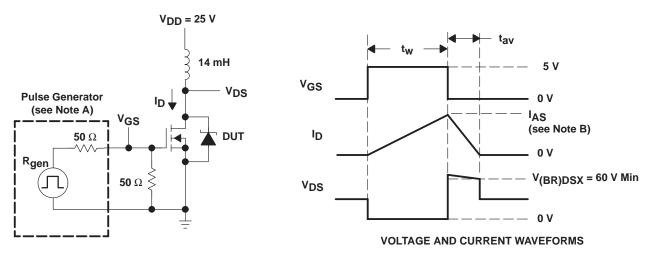


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

POWER DMOS ARRAY

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $z_O = 50 \Omega$.

B. Input pulse duration (t_W) is increased until peak current $I_{AS} = 3 A$.

Energy test level is defined as $E_{\mbox{AS}} = \frac{I_{\mbox{AS}} \times V_{\mbox{(BR)DSX}} \times t_{\mbox{av}}}{2} = 108 \ \mbox{mJ}, \ \mbox{where } t_{\mbox{av}} = \mbox{avalanche time}.$

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE JUNCTION TEMPERATURE 2.5 VGS(th) - Gate-to-Source Threshold Voltage - V $V_{DS} = V_{GS}$ 2 $I_D = 1 \text{ mA}$ $I_D = 100 \mu A$ 1.5 1 0.5 -40 -2040 60 80 100 120 140 160 0 20 T_.I - Junction Temperature - °C

Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs
JUNCTION TEMPERATURE

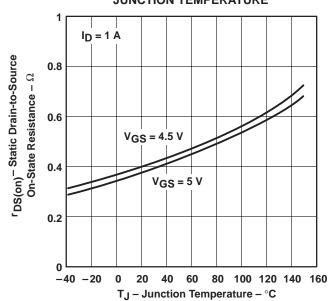
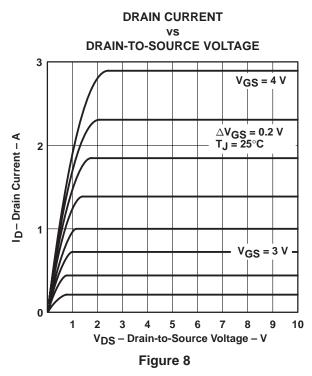


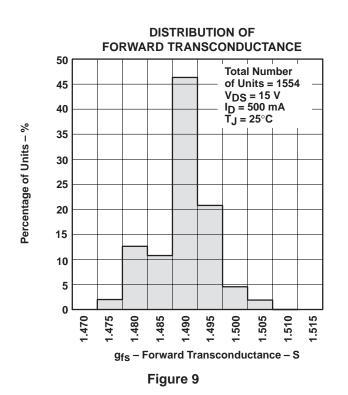
Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE **DRAIN CURRENT** 0.9 TJ = 25°C 0.8 r DS(on) - Static Drain-to-Source 0.7 0.6 On-State Resistance – Ω 0.5 V_{GS} = 4.5 V 0.4 $V_{GS} = 5 V$ 0.3 0.2 0.1 10 ID - Drain Current - A

Figure 7





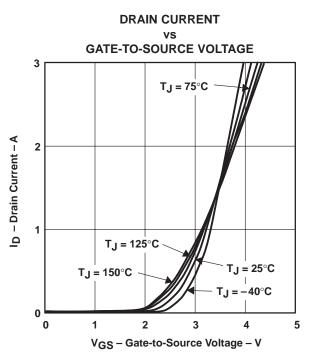
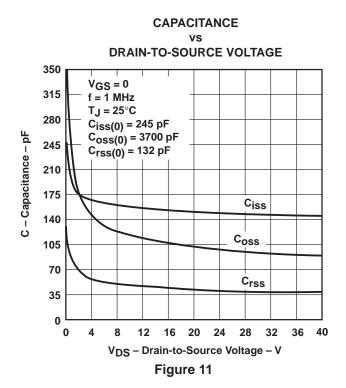
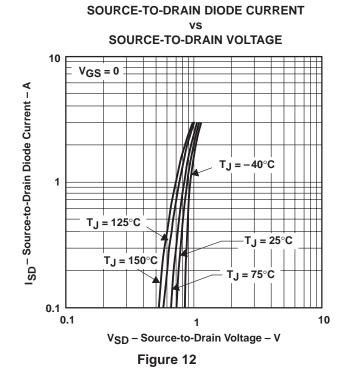


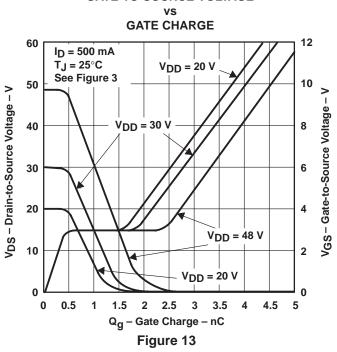
Figure 10

TYPICAL CHARACTERISTICS

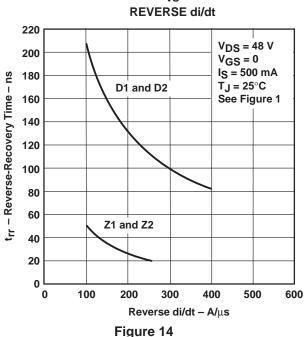




DRAIN-TO-SOURCE VOLTAGE AND GATE-TO-SOURCE VOLTAGE

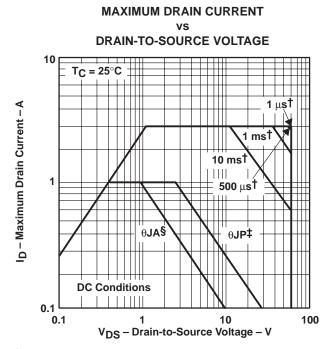


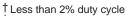
REVERSE-RECOVERY TIME vs





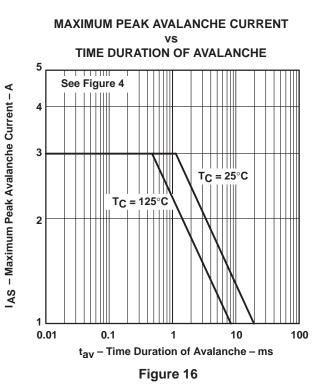
THERMAL INFORMATION





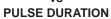
- ‡ Device mounted in intimate contact with infinite heatsink.
- § Device mounted on FR4 printed-circuit board with no heatsink.

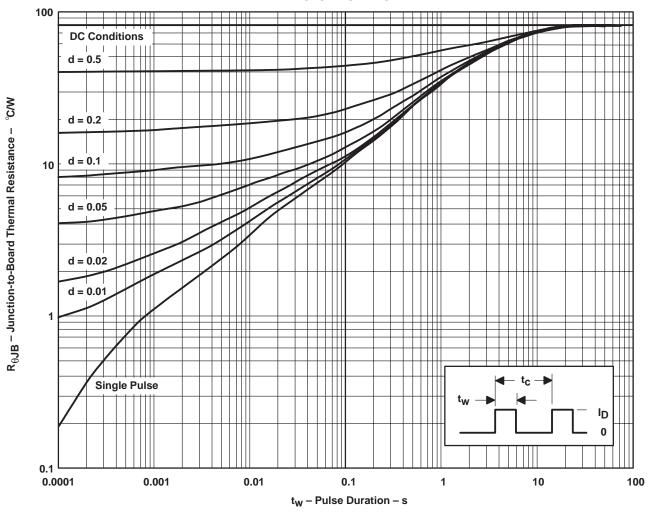
Figure 15



THERMAL INFORMATION

D PACKAGE† JUNCTION-TO-BOARD THERMAL RESISTANCE





† Device mounted on 24 in², 4-layer FR4 printed-circuit board with no heatsink.

 $\begin{array}{lll} \text{NOTE A:} & Z_{\theta B}(t) = r(t) \; R_{\theta JB} \\ & t_W = \text{pulse duration} \\ & t_C = \text{cycle time} \\ & d = \text{duty cycle} = \; t_W/t_C \end{array}$

Figure 17





PACKAGE OPTION ADDENDUM

8-Apr-2005

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPIC5223LD	OBSOLETE	SOIC	D	8	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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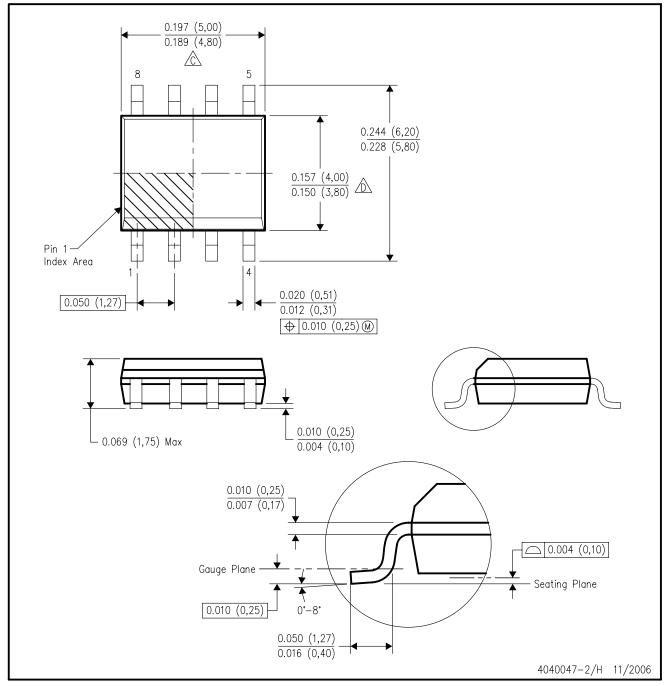
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.



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Mailing Address: Texas Instruments

Post Office Box 655303 Dallas, Texas 75265

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