

Low Threshold P-Channel Enhancement Mode Vertical DMOS FETs

Features

- ▶ Low threshold — -2.4V max.
- ▶ High input impedance
- ▶ Low input capacitance — 125pF max.
- ▶ Fast switching speeds
- ▶ Low on resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage
- ▶ Complementary N and P-channel devices

Applications

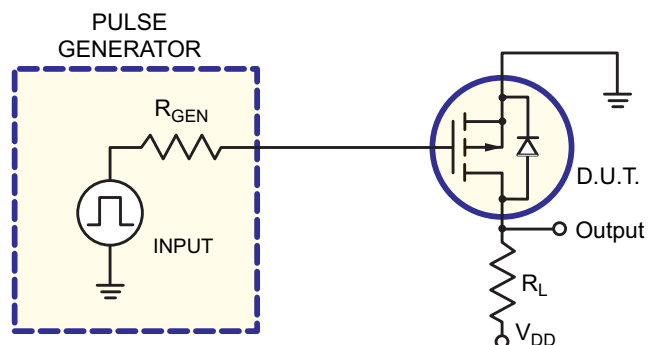
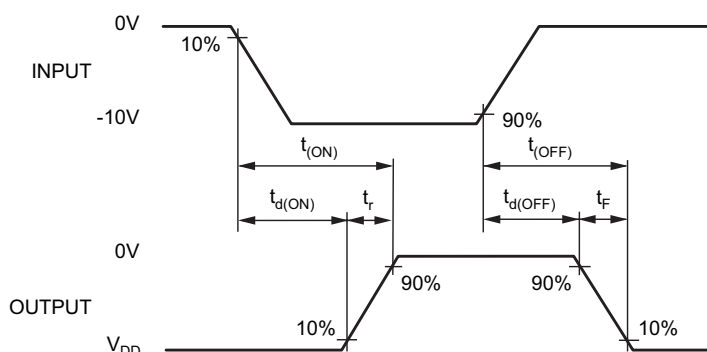
- ▶ Logic level interfaces — ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

General Description

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a widerange of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Switching Waveforms and Test Circuit



Thermal Characteristics

Package	I_D continuous† (mA)	I_D pulsed (A)	Power Dissipation @ $T_A = 25^\circ\text{C}$ (W)	θ_{jc} ($^\circ\text{C/W}$)	θ_{jc} ($^\circ\text{C/W}$)	I_{DR} † (mA)	I_{DRM} (A)
TO-243AA	-480	-2.5	1.6‡	15	78‡	-480	-2.5

† I_D (continuous) is limited by max rated T_J .

‡ Mounted on FR5 board, 25mm x 25mm x 1.57mm.

Ordering Information

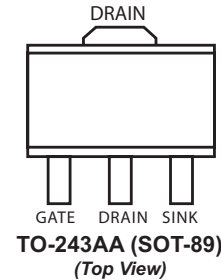
Device	Package Options		BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Ω)	$V_{GS(TH)}$ (max) (V)	$I_{D(ON)}$ (min) (A)
	TO-243AA (SOT-89)	Die*				
TP2510	TP2510N8-G	TP2510ND	-100	3.5	-2.4	-1.5

* MIL visual screening available.

-G indicates package is RoHS compliant ("Green")



Pin Configuration



Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking



W = Code for Week Sealed
= "Green" Packaging

TO-243AA (SOT-89) N8

Electrical Characteristics (@25°C unless otherwise specified)

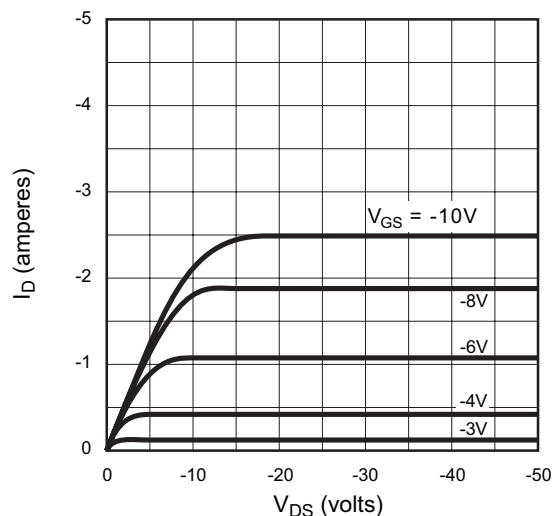
Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-100	-	-	V	$V_{GS} = 0V, I_D = -2.0mA$
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	$V_{GS} = V_{DS}, I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	5.0	mV/°C	$V_{GS} = V_{DS}, I_D = -1.0mA$
I_{GSS}	Gate body leakage	-	-	-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	-	-	-10	μA	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
			-	-1.0	mA	$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}, T_A = 125^\circ C$
$I_{D(ON)}$	ON-state drain current	-0.4	-0.6	-	A	$V_{GS} = -5.0V, V_{DS} = -25V$
		-1.5	-2.5	-		$V_{GS} = -10V, V_{DS} = -25V$
$R_{DS(ON)}$	Static drain-to-source ON-State Resistance	-	5.0	7.0	Ω	$V_{GS} = -5.0V, I_D = -250mA$
			2.0	3.5		$V_{GS} = -10V, I_D = -0.75A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.7	%/°C	$V_{GS} = -10V, I_D = -0.75A$
G_{FS}	Forward transconductance	300	360	-	mmho	$V_{DS} = -25V, I_D = -0.75A$
C_{ISS}	Input capacitance	-	80	125	pF	$V_{GS} = 0V, V_{DS} = -25V, f = 1.0 \text{ MHz}$
C_{OSS}	Common source output capacitance	-	40	70		
C_{RSS}	Reverse transfer capacitance	-	10	25		
$t_{d(ON)}$	Turn-ON delay time	-	-	10	ns	$V_{DD} = -25V, I_D = -1.0A, R_{GEN} = 25\Omega$
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-OFF delay time	-	-	20		
t_f	Fall time	-	-	15		
V_{SD}	Diode forward voltage drop	-	-	-1.8	V	$V_{GS} = 0V, I_{SD} = -1.0A$
t_{rr}	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = -1.0A$

Notes:

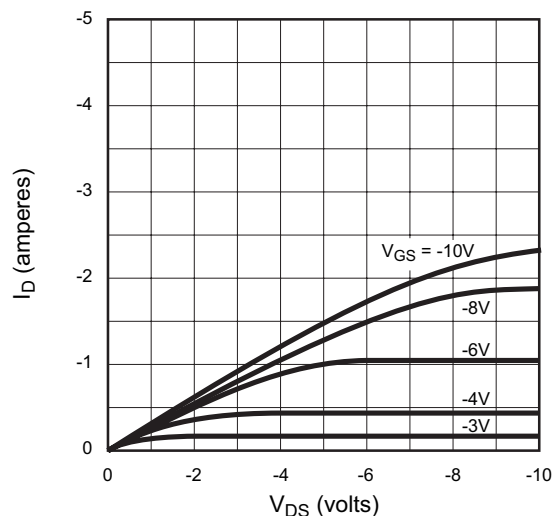
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Typical Performance Curves

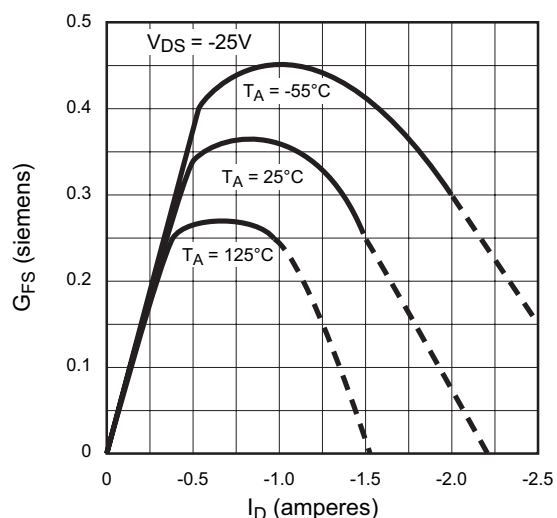
Output Characteristics



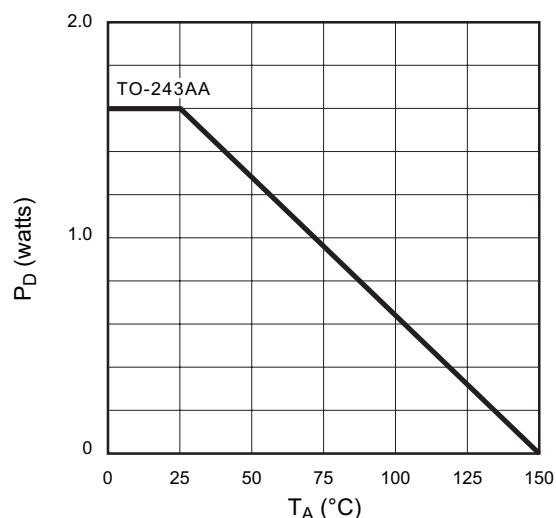
Saturation Characteristics



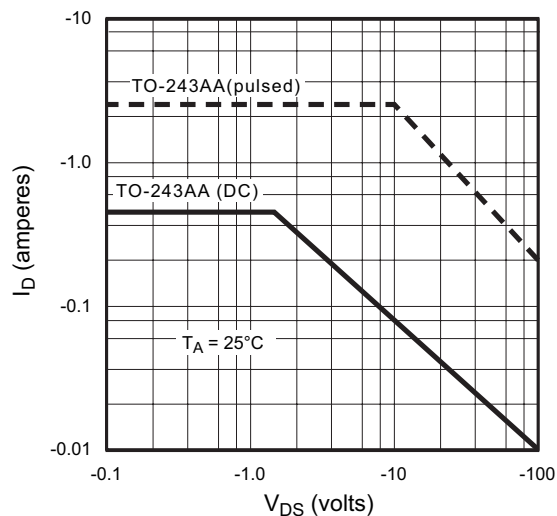
Transconductance vs. Drain Current



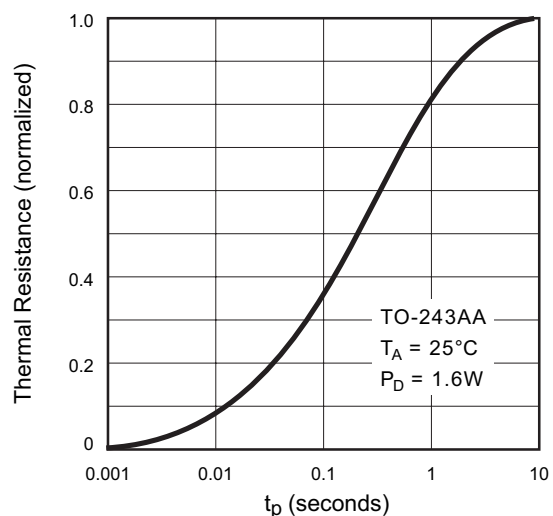
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

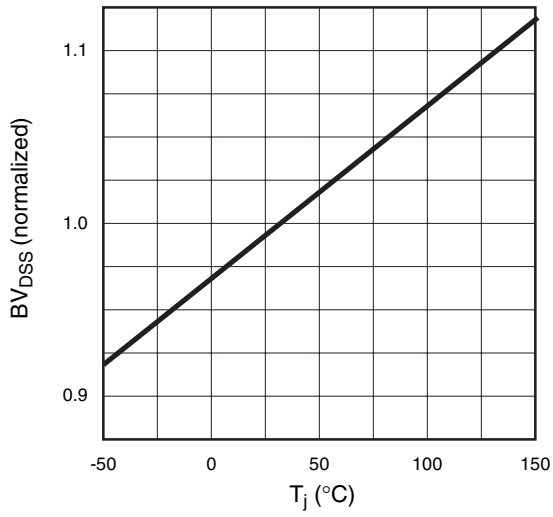


Thermal Response Characteristics

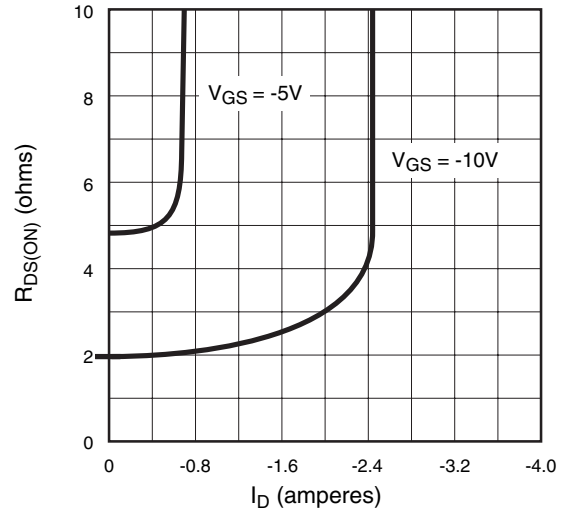


Typical Performance Curves

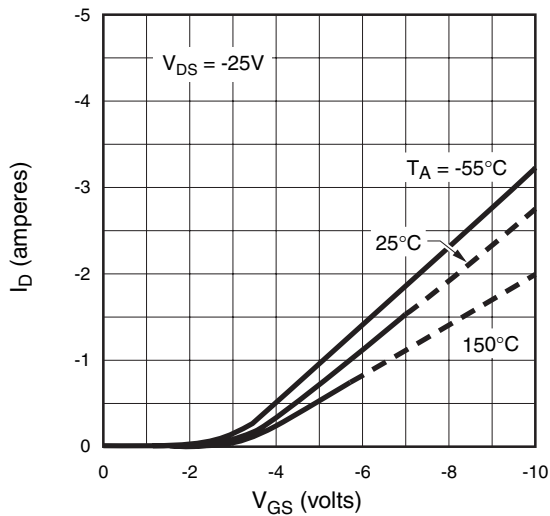
BV_{DS} Variation with Temperature



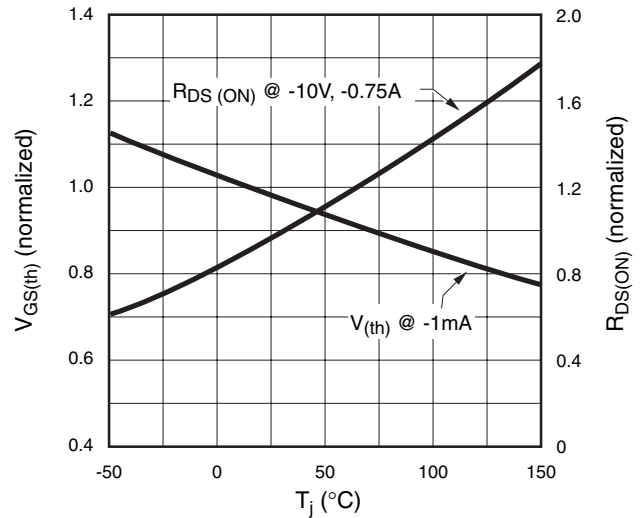
On-Resistance vs. Drain Current



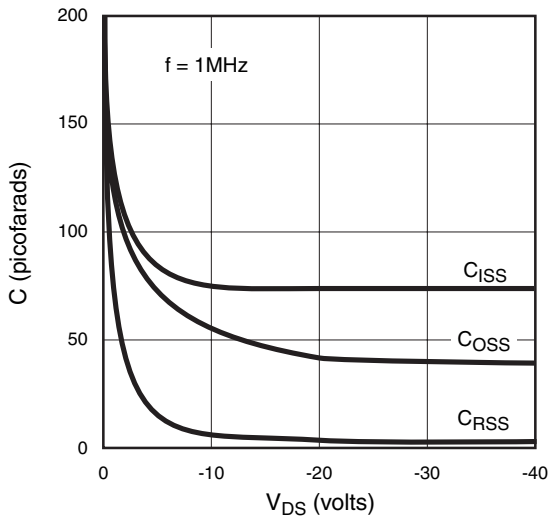
Transfer Characteristics



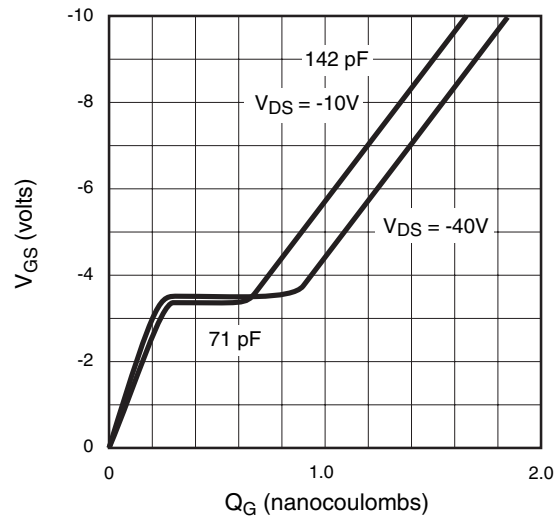
V_{th} and R_{DS} Variation with Temperature



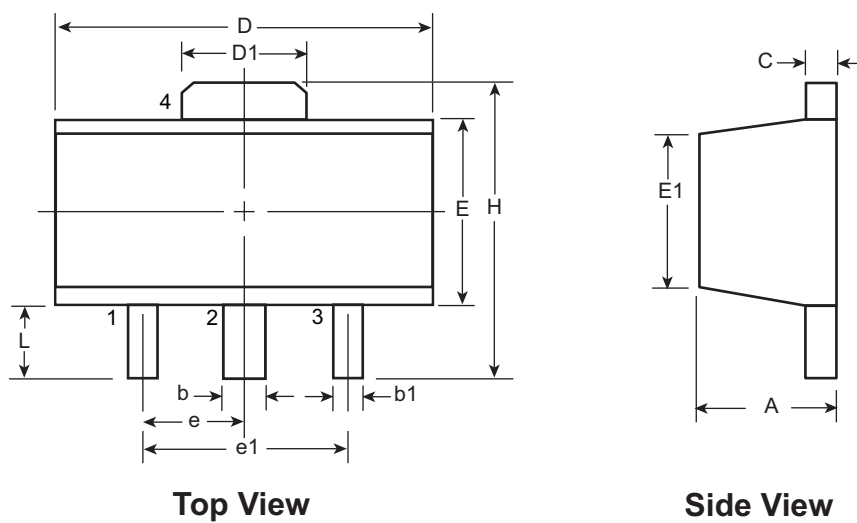
Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



3-Lead TO-243AA (SOT-89) Package Outline (N8)



Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.13	1.50 BSC	3.00 BSC	3.94	0.89
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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