P- Channel Enhancement-Mode Vertical DMOS FETs

Features

- Low threshold — -2.0V max.
- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage
- Complementary N- and P-channel devices

General Description

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

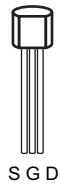
Absolute Maximum Ratings

Parameter	Value
Drain to source voltage	BV_{DSS}
Drain to gate voltage	BV_{DGS}
Gate to source voltage	±20V
Operating and storage temperature	-55°C to +150°C
Soldering temperature[1]	+300°C

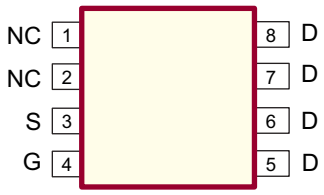
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

***Note 1**. Distance of 1.6mm from case for 10 seconds.*

Pin Configurations



TO-92



SO-8
(top view)

Ordering Information

Device	Package Options		BV_{DSS}/BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)
	SO-8	TO-92				
TP2635	-	TP2635N3	-350V	15Ω	-2.0V	-0.7A
	-	TP2635N3-G				
TP2640	TP2640LG	TP2640N3	-400V	15Ω	-2.0V	-0.7A
	TP2640LG-G	TP2640N3-G				

-G indicates package is RoHS compliant ('Green')

Thermal Characteristics

Package	I_D (continuous)[1]	I_D (pulsed)	Power Dissipation @T_C = 25°C	Θ_{jc} (°C/W)	Θ_{ja} (°C/W)	I_{DR}[1]	I_{DRM}
SO-8	-210mA	-1.25A	1.3W[2]	24	96[2]	210mA	-1.25A
TO-92	-180mA	-0.8A	1.0W	125	170	-180mA	-0.8A

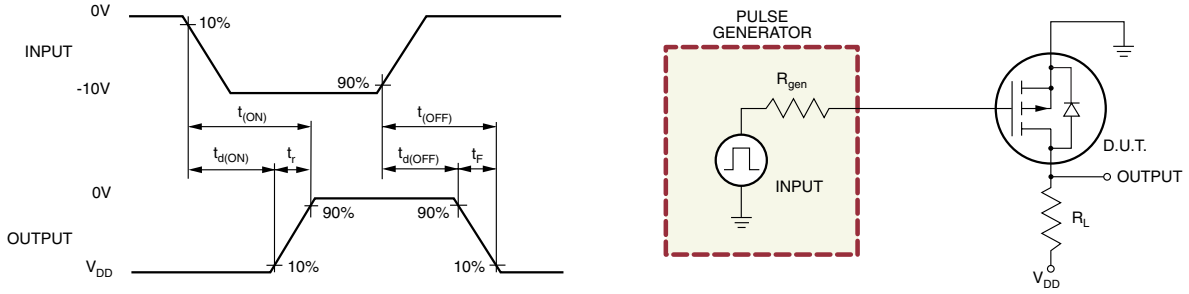
Notes:
1. I_D (continuous) is limited by max rated T_j.
2. Mounted on FR4 board, 25mm x 25mm x 1.57mm

Electrical Characteristics *(T_J = 25°C unless otherwise specified)*

Symbol	Parameter		Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source break-down voltage	TP2640	-400	-	-	V	V_{GS} = 0V, I_D = -2.0mA
		TP2635	-350				
$V_{GS(th)}$	Gate threshold voltage		-0.8	-	-2.0	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature		-	-	5	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate body leakage		-		-100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current		-	-	-1.0	μA	V_{DS} = -100V, V_{GS} = 0V
					-10.0	μA	V_{DS} = Max rating, V_{GS} = 0V
					-1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	ON-state drain current		0.7	-	-	A	V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static drain-to-source ON-state resistance		-	12	15	Ω	V_{GS} = -2.5V, I_D = -200mA
				11	15		V_{GS} = -4.5V, I_D = -150mA
				11	15		V_{GS} = -10V, I_D = -300mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature		-	-	0.75	%/°C	V_{GS} = -10V, I_D = -300mA
G_{FS}	Forward transconductance		200	-	-	m℧	V_{DS} = -25V, I_D = -300mA
C_{ISS}	Input capacitance		-	-	300	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1MHz
C_{OSS}	Common source output capacitance		-	-	50		
C_{RSS}	Reverse transfer capacitance		-	-	12		
$t_{d(ON)}$	Turn-ON delay time		-	-	10	ns	V_{DD} = 25V, I_D = 2.0A, R_{GEN} = 25Ω
t_r	Rise time		-	-	15		
$t_{d(OFF)}$	Turn-OFF delay time		-	-	60		
t_f	Fall time		-	-	40		
V_{SD}	Diode forward voltage drop		-	-	-1.8	V	V_{GS} = 0V, I_{SD} = 200mA
t_{rr}	Reverse recovery time		-	300	-	ns	V_{GS} = 0V, I_{SD} = 1.0A

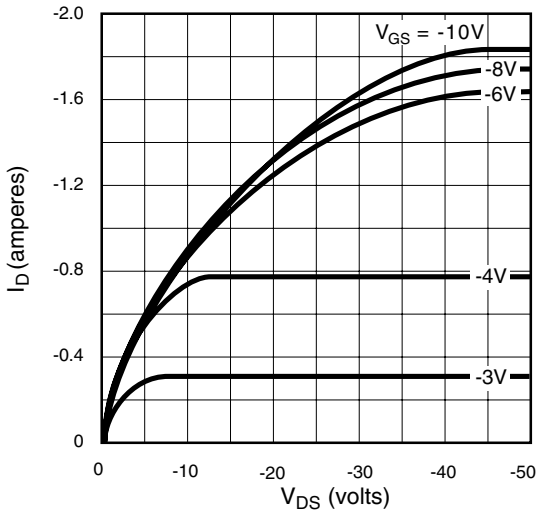
Notes:
1.All D.C. parameters 100% tested at 25C unless otherwise stated. (Pulse test: 300s pulse, 2% duty cycle.)
2.All A.C. parameters sample tested.

N- Channel Switching Waveforms and Test Circuit

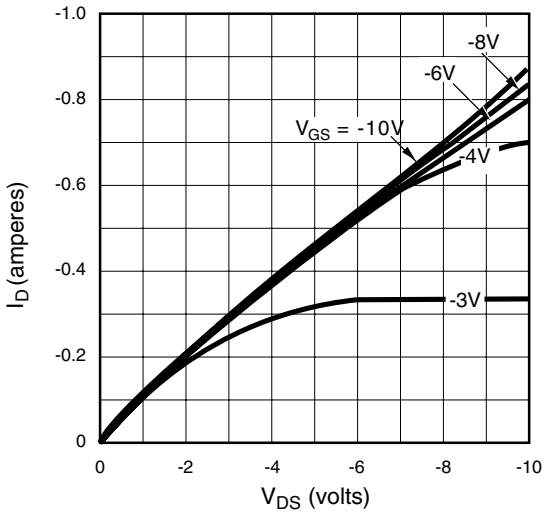


Typical Performance Curves

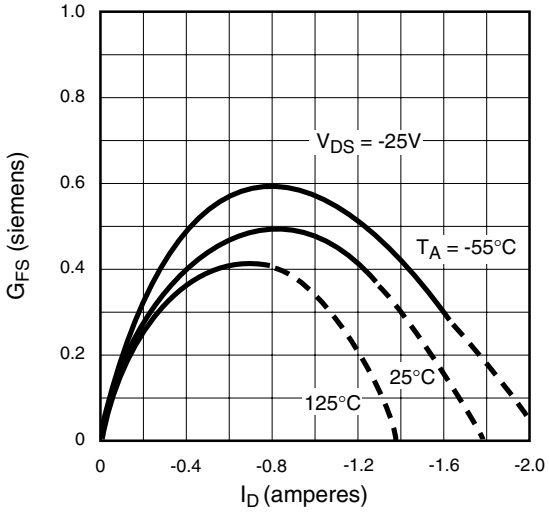
Output Characteristics



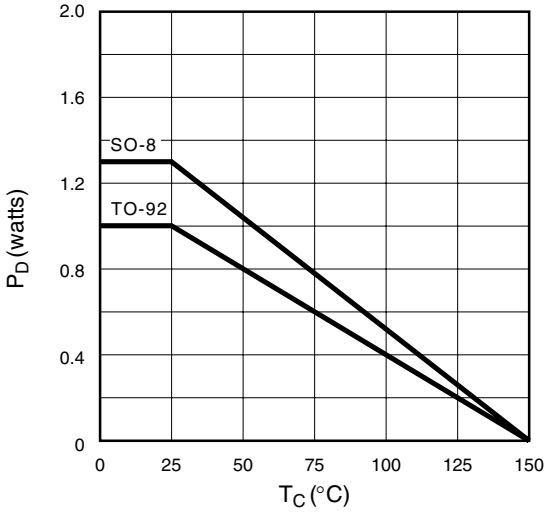
Saturation Characteristics



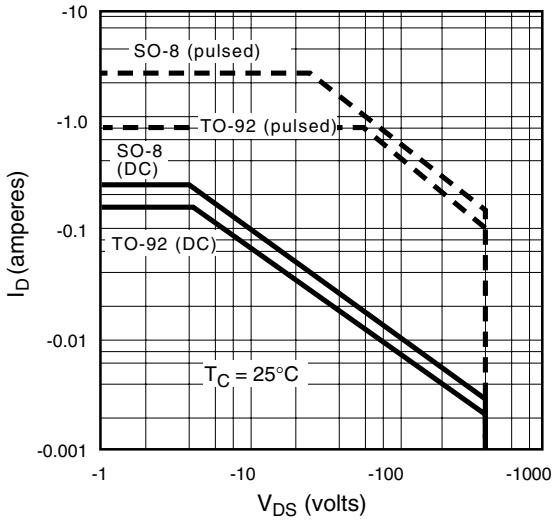
Transconductance vs. Drain Current



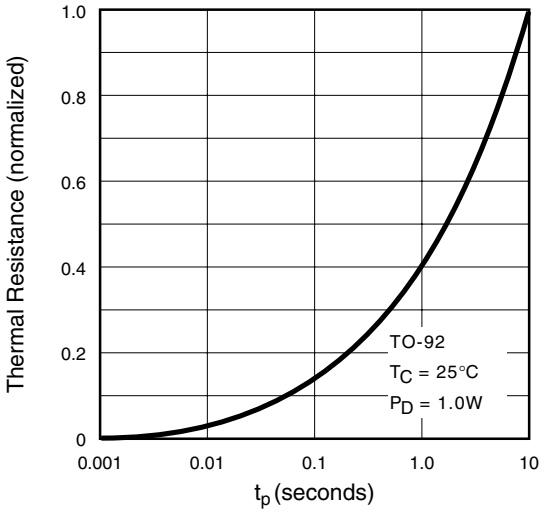
Power Dissipation vs. Temperature



Maximum Rated Safe Operating Area

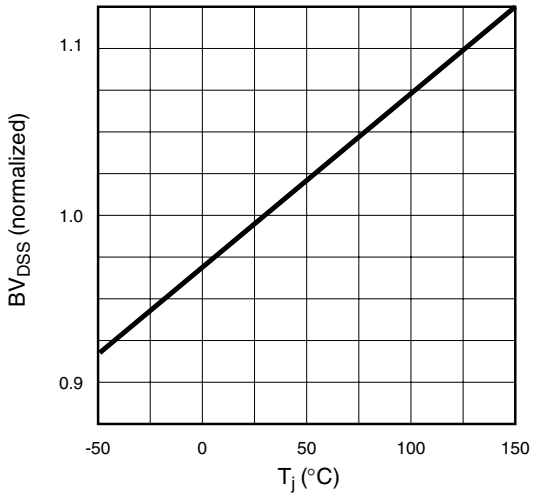


Thermal Response Characteristics

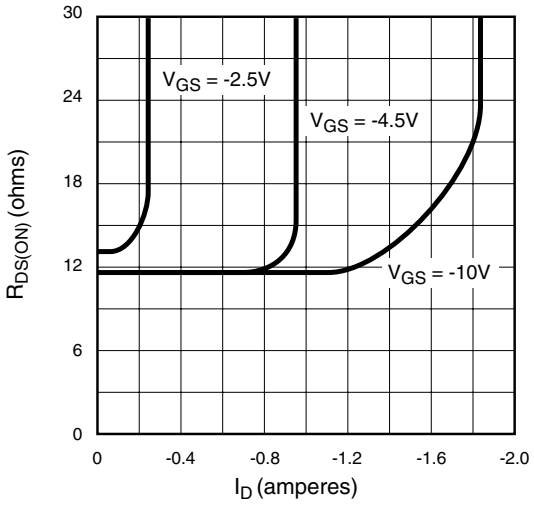


Typical Performance Curves (cont.)

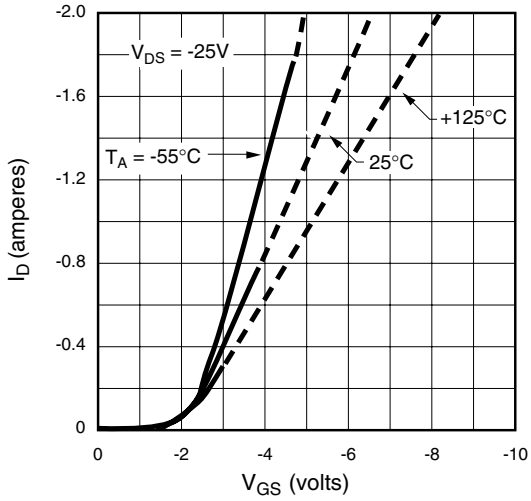
BV_{DSS} Variation with Temperature



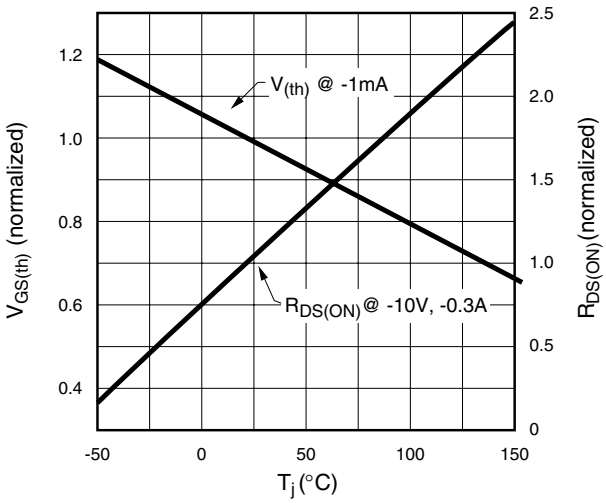
On-Resistance vs. Drain Current



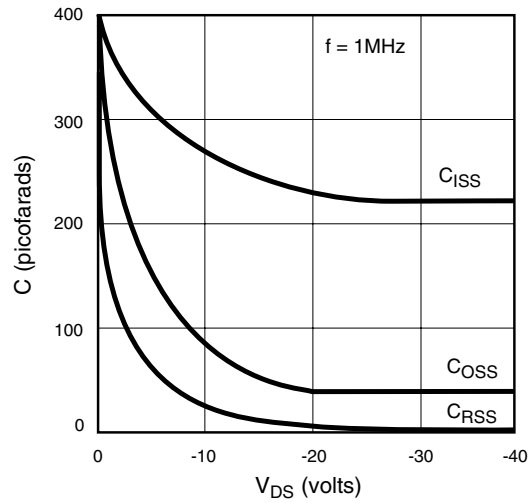
Transfer Characteristics



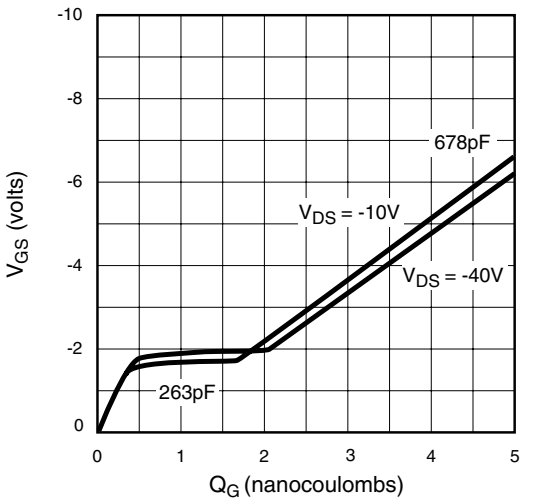
V_{TH} and R_{DS} Variation with Temperature



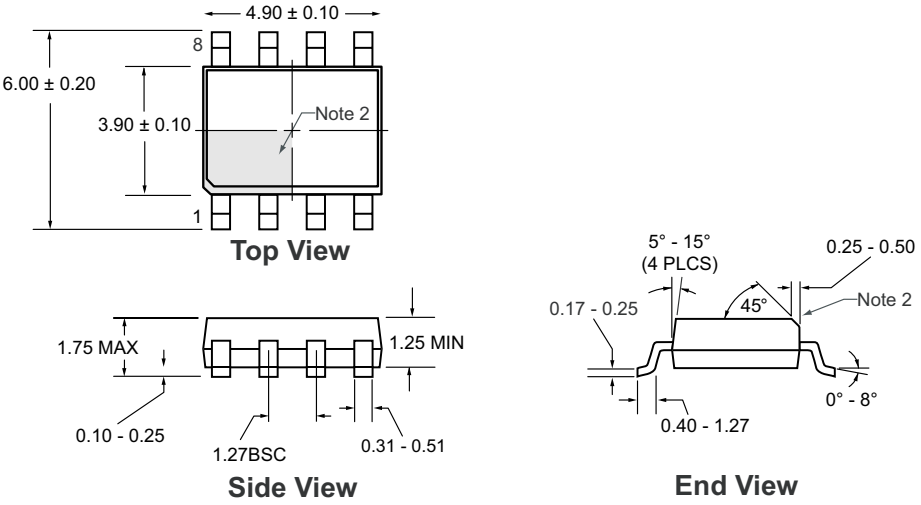
Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



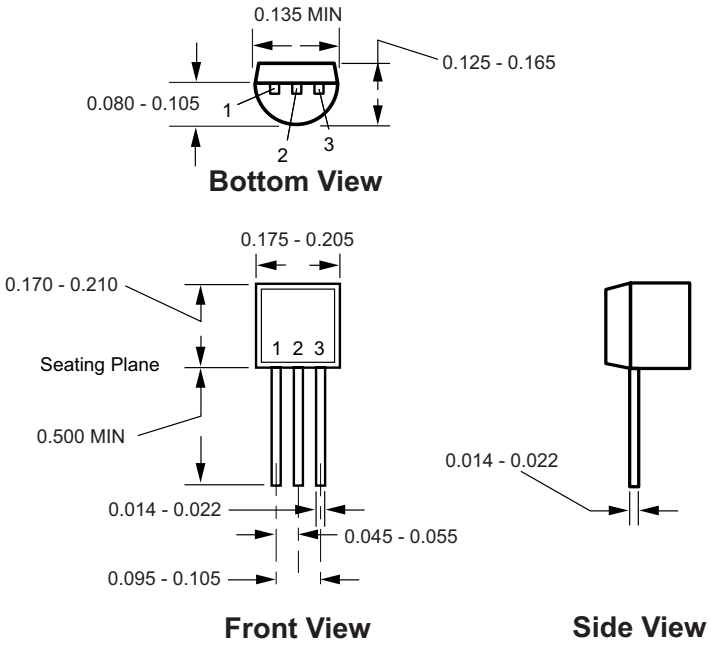
8-Lead SOIC Package Outline (LG)



Notes:

1. All dimensions in millimeters. Angles in degrees.
2. If the corner is not chamfered, then a Pin 1 identifier must be located within the area indicated.

3-Lead TO-92 Package Outline (N3)



Notes:
All dimensions are in millimeters; all angles in degrees.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 222-8888 / FAX: (408) 222-4895
www.supertex.com

Doc.# DSFP-TP2635_TP2640
C032807