TL971, TL972, TL974
OUTPUT RAIL-TO-RAIL VERY-LOW-NOISE OPERATIONAL AMPLIFIERS

SLOS467A – OCTOBER 2006 – REVISED OCTOBER 2006

FEATURES

- **Rail-to-Rail Output Voltage Swing: ±2.4 V at V_{CC} = ±2.5 V**
- **Very Low Noise Level: 4 nV/√Hz**
- **Ultra-Low Distortion: 0.003%**
- **High Dynamic Features: 12 MHz, 4 V/μs**
- **Operating Range: 2.7 V to 15 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B)**
  - **200-V Machine Model (A115-A)**
  - **1500-V Charged-Device Model (C101)**

APPLICATIONS

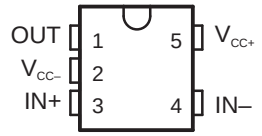
- **Portable Equipment (CD Players, PDAs)**
- **Portable Communications (Cell Phones, Pagers)**
- **Instrumentation and Sensors**
- **Professional Audio Circuits**

DESCRIPTION/ORDERING INFORMATION

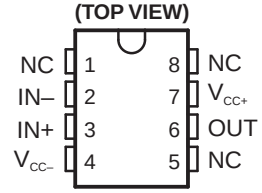
The TL97x family of operational amplifiers operates at voltages as low as ±1.35 V and features output rail-to-rail signal swing. The TL97x boast characteristics that make them particularly well suited for portable and battery-supplied equipment. Very low noise and low distortion characteristics make them ideal for audio preamplification.

The TL971 is housed in the space-saving 5-pin SOT-23 package, which simplifies board design because of the ability to be placed anywhere (outside dimensions are 2.8 mm × 2.9 mm).

TL971...DBV PACKAGE
(TOP VIEW)

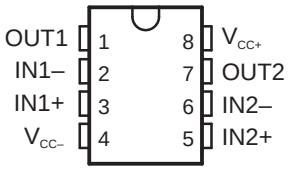


TL971...D PACKAGE
(TOP VIEW)

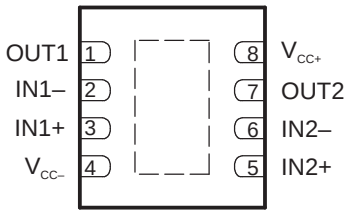


NC – No internal connection

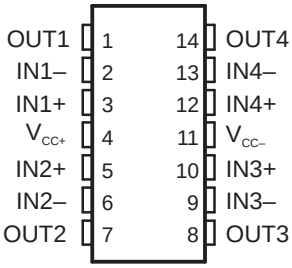
TL972...D, P, OR PW PACKAGE
(TOP VIEW)



TL972...DRG PACKAGE
(TOP VIEW)



TL974...D, N, OR PW PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE(1)			ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	Single	SOIC – D	Reel of 2500	TL971IDR	PREVIEW
			Tube of 75	TL971ID	
		SOT-23 – DBV	Reel of 3000	TL971IDBVR	PREVIEW
			Reel of 250	TL971IDBVT	
	Dual	PDIP – P	Tube of 50	TL972IP	PREVIEW
		QFN – DRG	Reel of 1000	TL972IDRGR	
		SOIC – D	Reel of 2500	TL972IDR	PREVIEW
			Tube of 75	TL972ID	
		TSSOP – PW	Reel of 2000	TL972IPWR	PREVIEW
			Tube of 150	TL972IPW	
	Quad	PDIP – N	Tube of 25	TL974IN	TL974IN
		SOIC – D	Reel of 2500	TL974IDR	SR974I
			Tube of 50	TL974ID	
		TSSOP – PW	Reel of 2000	TL974IPWR	SR974I
			Tube of 90	TL974IPW	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)			2.7	17	V
V_{ID}	Differential input voltage(3)				±1	V
V_{IN}	Input voltage(4)			V_{CC-} – 0.3	V_{CC+} + 0.3	V
θ_{JA}	Package thermal impedance, junction to free air	D package(5)	8 pin		97	°C/W
			14 pin		86	
		DBV package(5)			206	
		DRG package(6)			44	
		N package(5)			80	
		P package(5)			85	
		PW package(5)	8 pin		149	
			14 pin		113	
T_J	Maximum junction temperature				150	°C
T_{lead}	Maximum lead temperature	Soldering, 10 s			260	°C
T_{stg}	Storage temperature range			–65	150	°C
ESD	Human-Body Model (HBM)				2	kV
	Machine Model (MM)				200	V
	Charged-Device Model (CDM)				1.5	kV

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Differential voltages for the noninverting input terminal are with respect to the inverting input terminal.
(4) The input and output voltages must never exceed V_{CC} + 0.3 V.
(5) Package thermal impedance is calculated in accordance with JESD 51-7.
(6) Package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	15	V
V_{ICM}	Common-mode input voltage	V_{CC-} + 1.15	V_{CC+} – 1.15	V
T_A	Operating free-air temperature	–40	125	°C

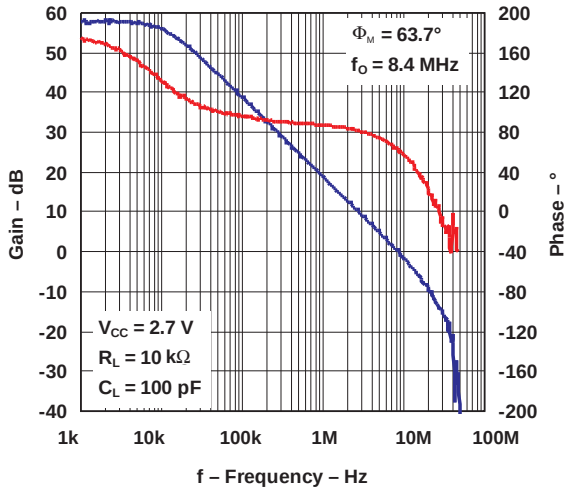
Electrical Characteristics

V_{CC+} = 2.5 V, V_{CC-} = –2.5 V, full-range T_A = –40°C to 125°C (unless otherwise noted)

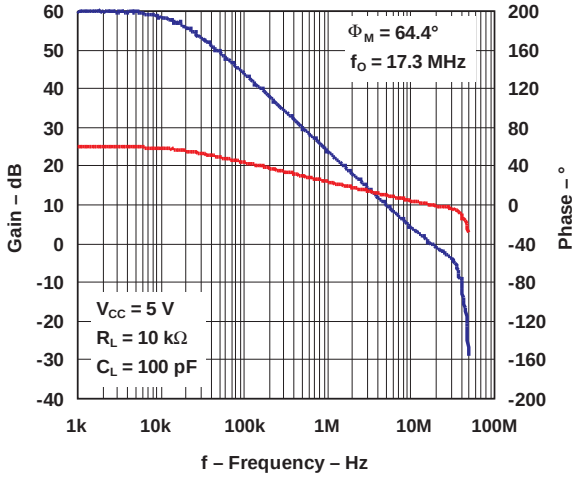
PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		1	4	mV
			Full range			6	
αV_{IO}	Input offset voltage drift	V_{ICM} = 0 V, V_O = 0 V	25°C		5		µV/°C
I_{IO}	Input offset current	V_{ICM} = 0 V, V_O = 0 V	25°C		10	150	nA
I_{IB}	Input bias current	V_{ICM} = 0 V, V_O = 0 V	25°C		200	750	nA
			Full range			1000	
V_{ICM}	Common-mode input voltage		25°C	–1.35		1.35	V
CMRR	Common-mode rejection ratio	V_{ICM} = ±1.35 V	25°C	60	85		dB
SVR	Supply-voltage rejection ratio	V_{CC} = ±2 V to ±3 V	25°C	60	70		dB
A_{VD}	Large-signal voltage gain	R_L = 2 kΩ	25°C	70	80		dB
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C	2	2.4		V
V_{OL}	Low-level output voltage	R_L = 2 kΩ	25°C		–2.4	–2	V
I_{source}	Output source current		25°C	1.3	1.5		mA
		V_{CC} = 2.5 V	Full range	1			
I_{sink}	Output sink current		25°C	50	80		mA
		V_{CC} = 2.5 V	Full range	25			
I_{CC}	Supply current (per amplifier)	Unity gain, No load	25°C		2	2.8	mA
			Full range			3.2	
GBWP	Gain bandwidth product	f = 100 kHz, R_L = 2 kΩ, C_L = 100 pF	25°C	8.5	12		MHz
SR	Slew rate	A_V = 1, V_{IN} = ±1 V	25°C	3.5	5		V/µs
			Full range	3			
Φm	Phase margin at unity gain	R_L = 2kΩ, C_L =100 pF	25°C		60		°
Gm	Gain margin	R_L = 2kΩ, C_L =100 pF	25°C		10		dB
e_n	Equivalent input noise voltage	f = 100 kHz	25°C		4		nV/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_v = –1, R_L = 10 kΩ	25°C		0.003		%

TYPICAL CHARACTERISTICS

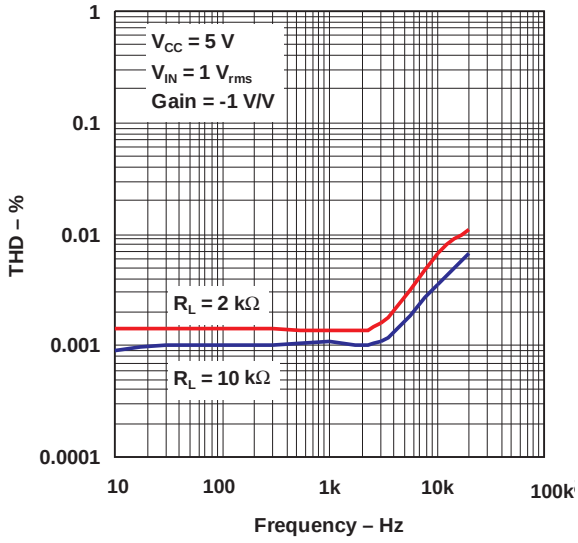
GAIN AND PHASE vs FREQUENCY



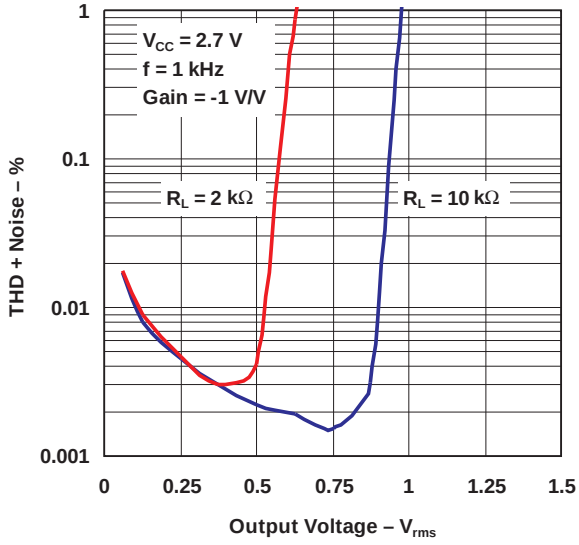
GAIN AND PHASE vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

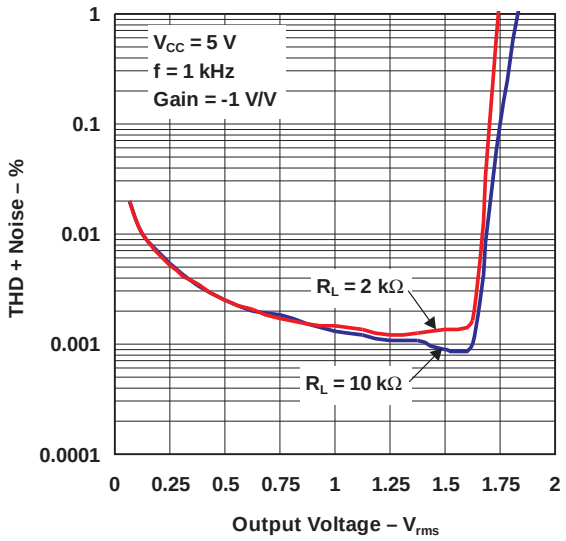


TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE

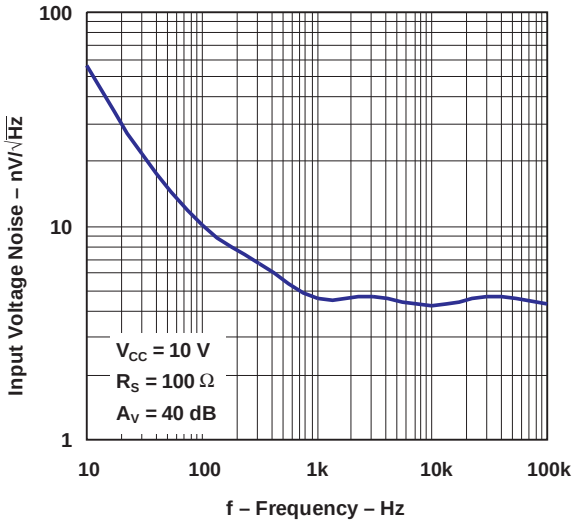


TYPICAL CHARACTERISTICS (continued)

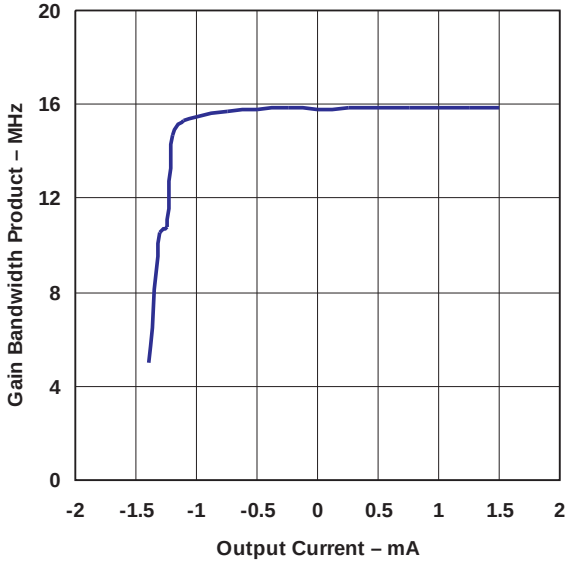
TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE



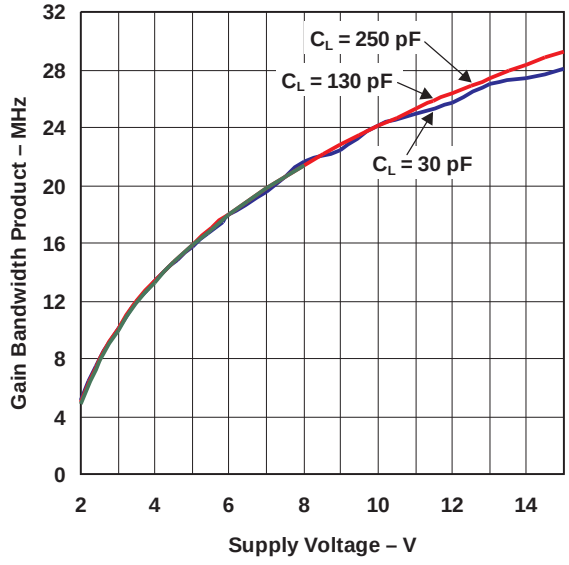
INPUT VOLTAGE NOISE vs FREQUENCY



GAIN BANDWIDTH PRODUCT vs OUTPUT CURRENT

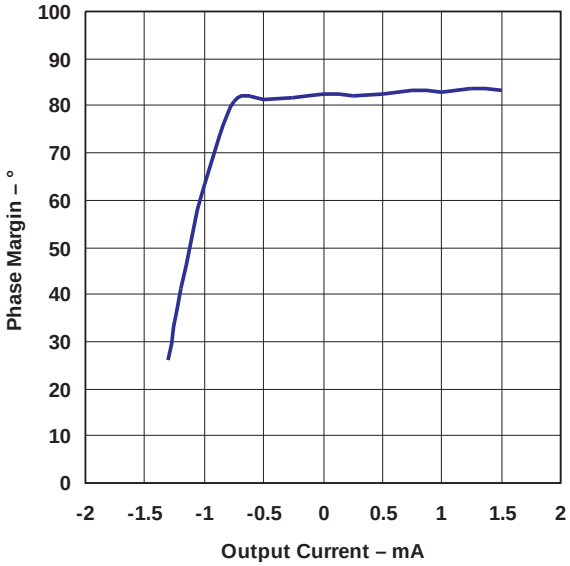


GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

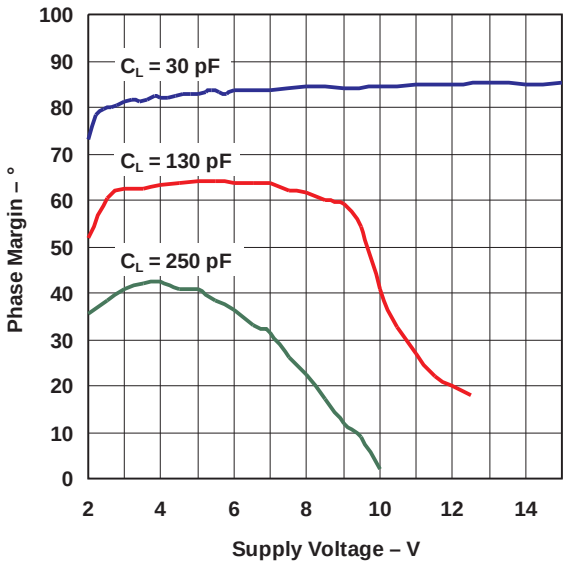


TYPICAL CHARACTERISTICS (continued)

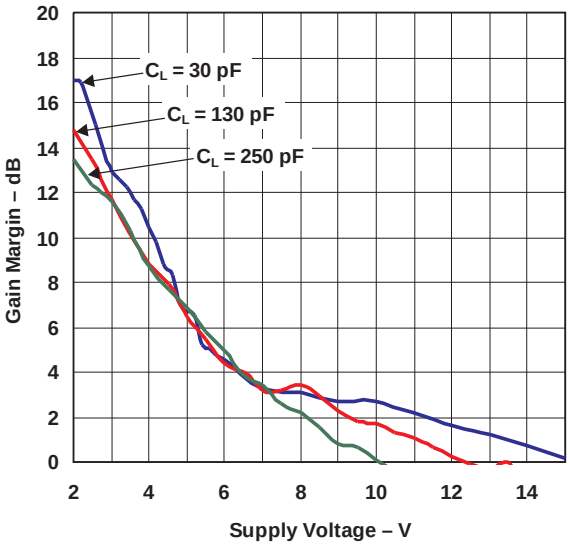
PHASE MARGIN vs OUTPUT CURRENT



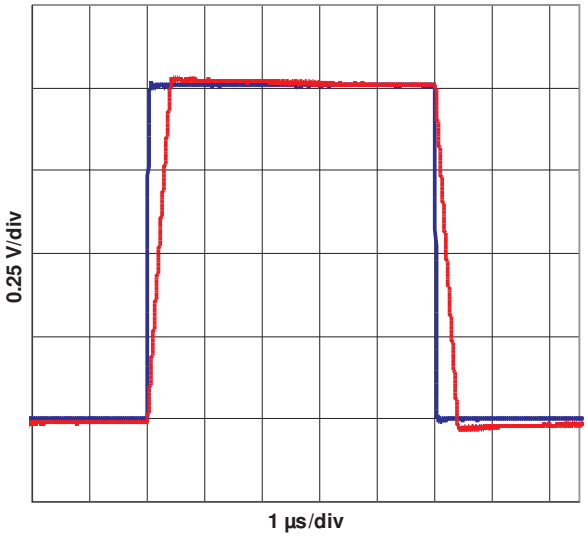
PHASE MARGIN vs SUPPLY VOLTAGE



GAIN MARGIN vs SUPPLY VOLTAGE

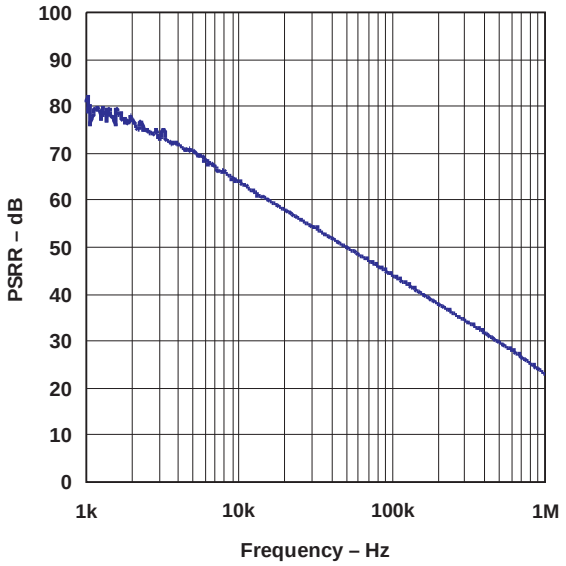


INPUT RESPONSE

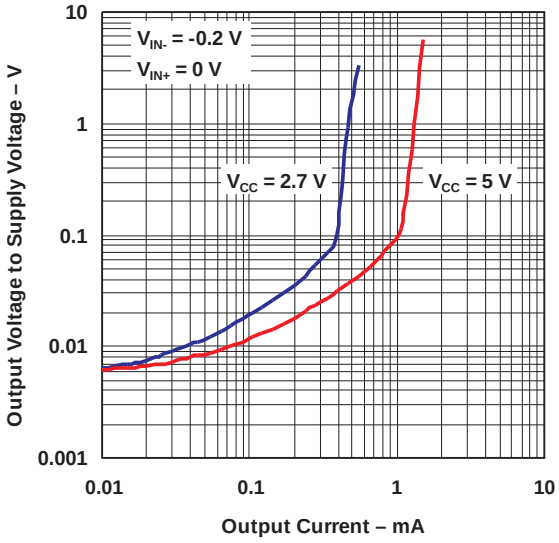


TYPICAL CHARACTERISTICS (continued)

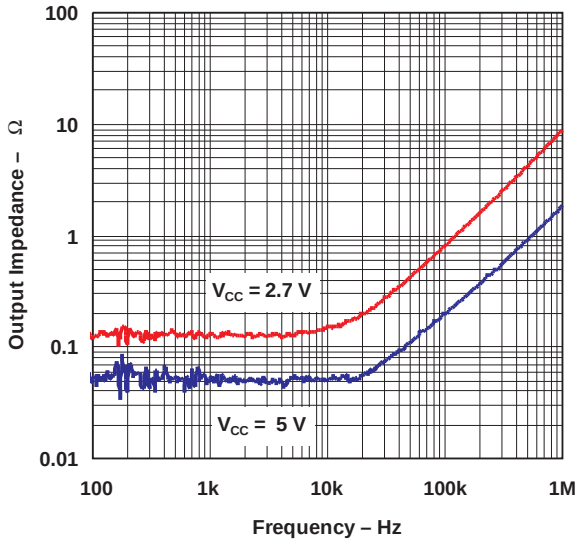
POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY



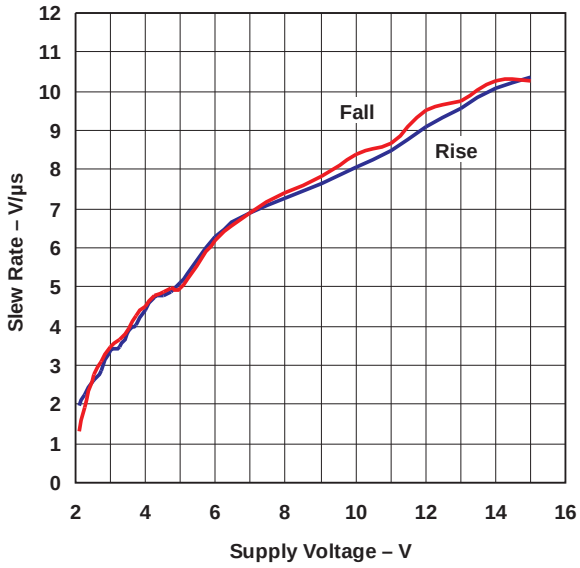
OUTPUT VOLTAGE vs OUTPUT CURRENT



OUTPUT IMPEDANCE vs FREQUENCY



SLEW RATE vs SUPPLY VOLTAGE



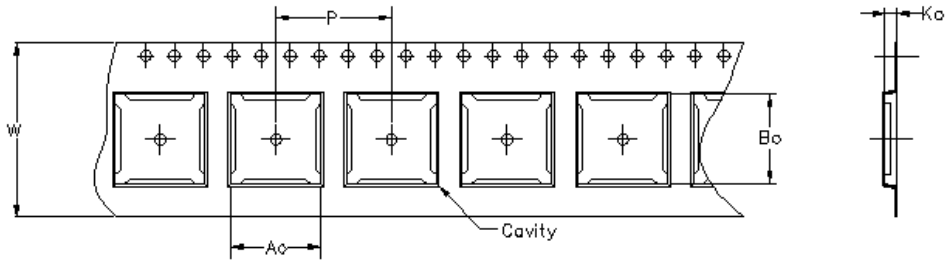
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL974ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL974IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL974IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL974IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL974IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL974INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL974IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL974IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL974IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL974IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

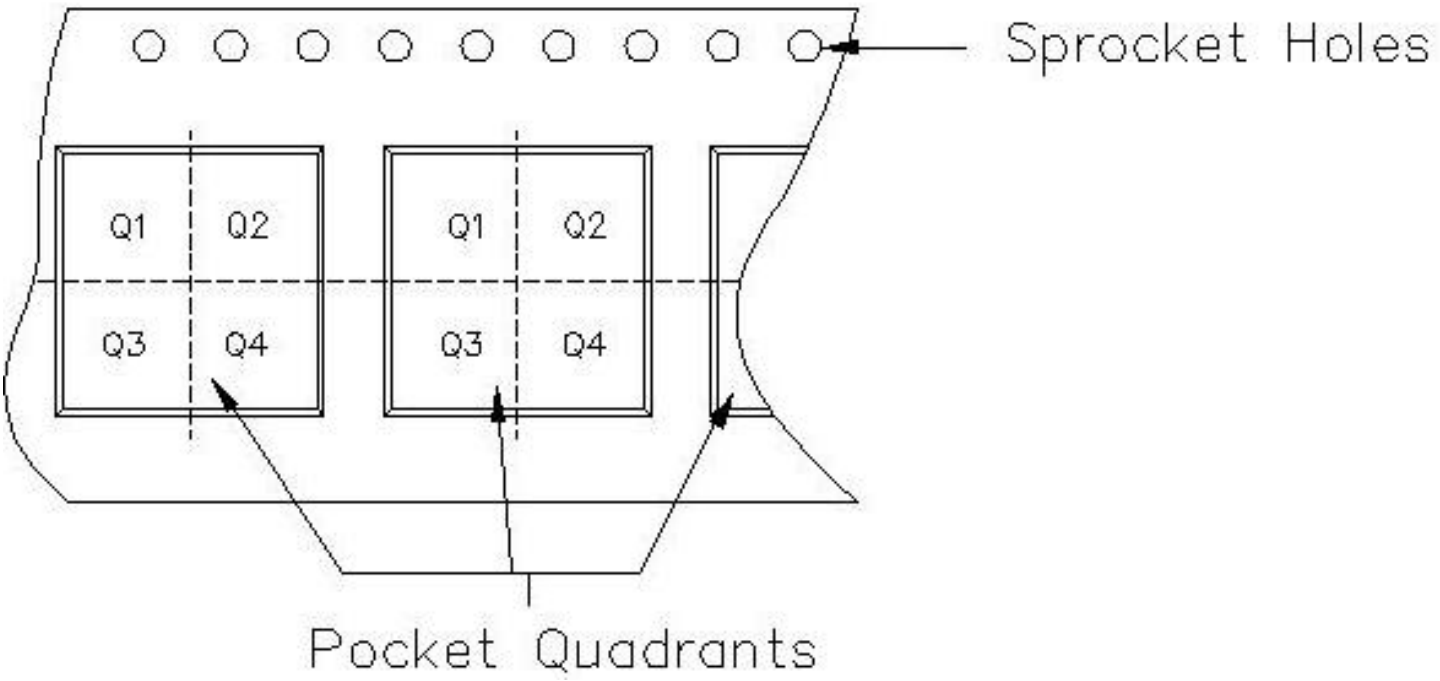
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



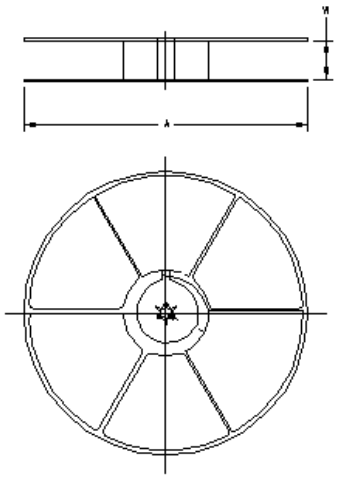
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



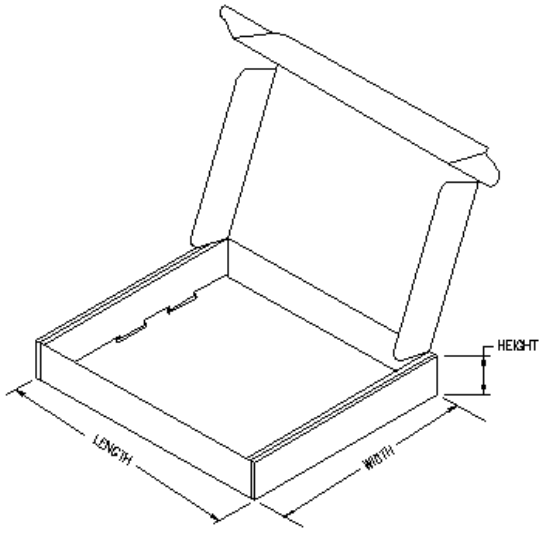
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL974IDR	D	14	FMX	330	0	6.5	9.0	2.1	8	16	Q1
TL974IPWR	PW	14	MLA	330	12	7.0	5.6	1.6	8	12	Q1



TAPE AND REEL BOX INFORMATION

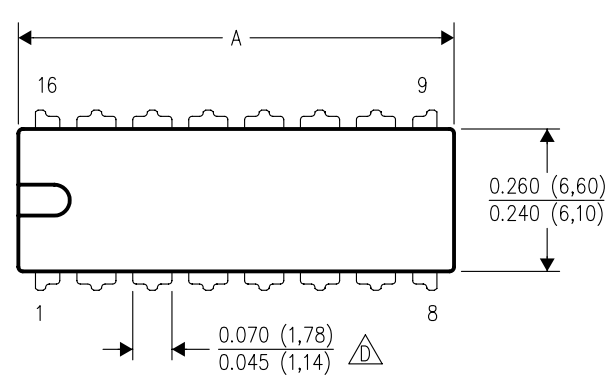
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TL974IDR	D	14	FMX	333.2	333.2	28.58
TL974IPWR	PW	14	MLA	338.1	340.5	20.64



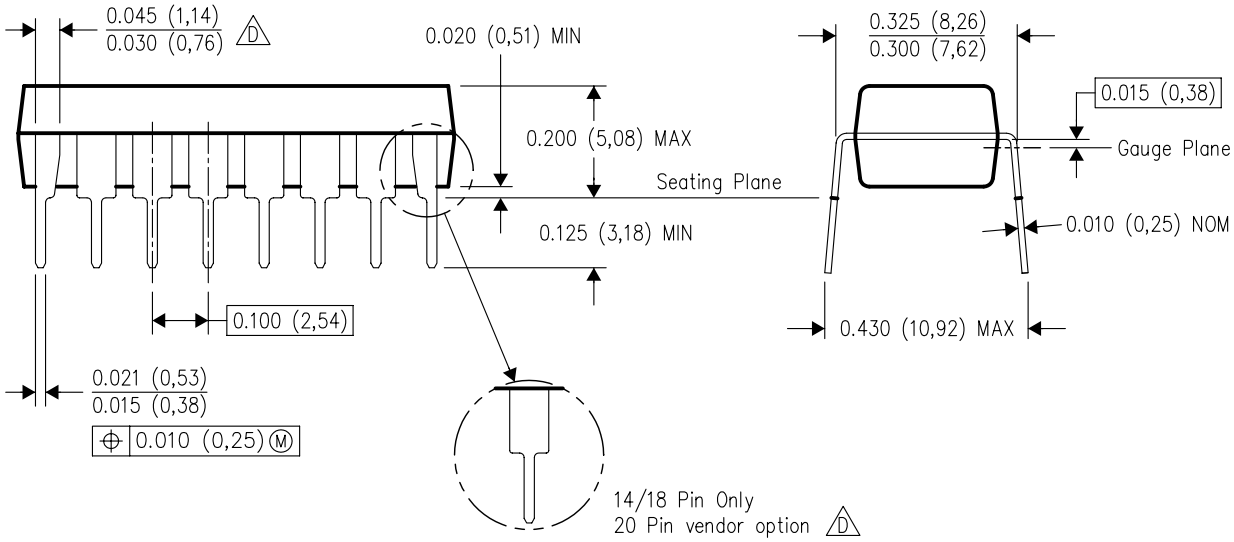
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



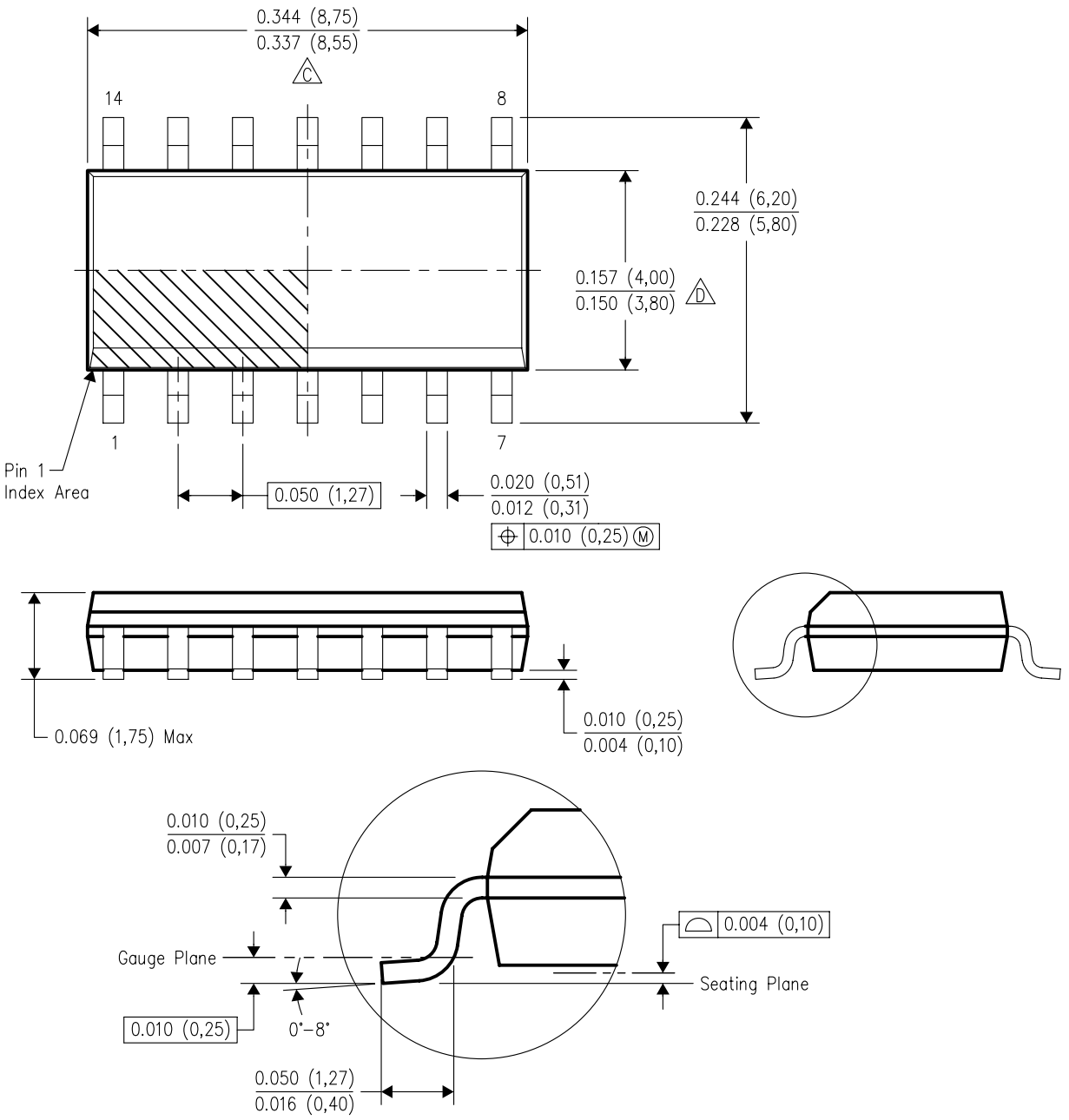
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

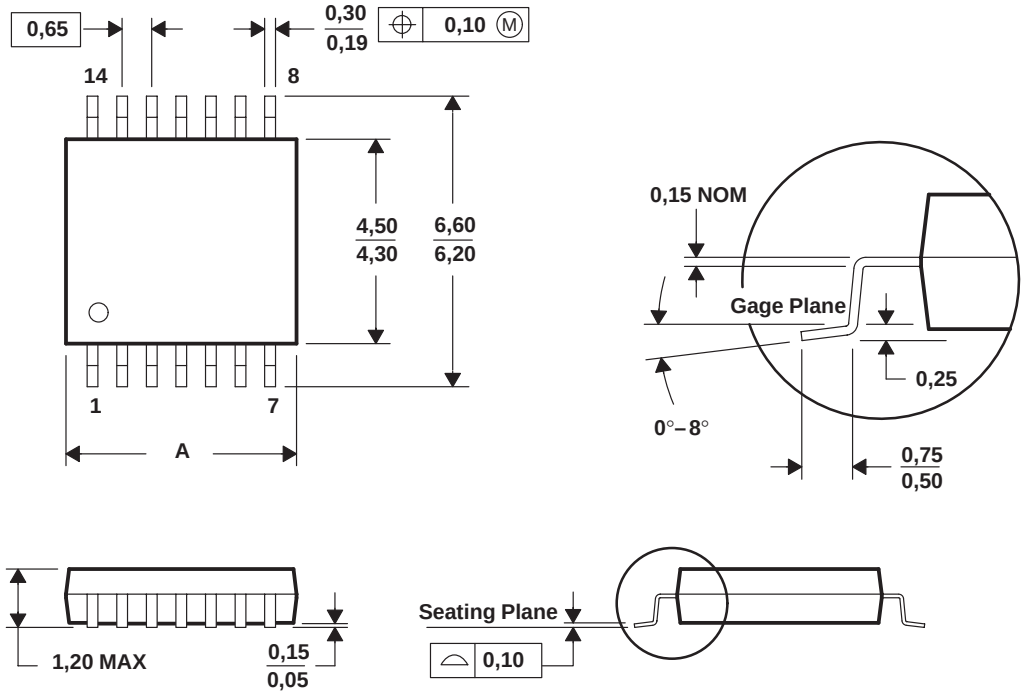
D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

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