TBB1004

Twin Build in Biasing Circuit MOS FET IC
VHF/UHF RF Amplifier

HITACHI

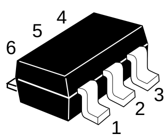
ADE-208-988H (Z)
9th. Edition
Dec. 2000

Features

- Small SMD package CMPAK-6 built in twin BBFET; To reduce using parts cost & PC board space.
- Suitable for World Standard Tuner RF amplifier.
- Very useful for total tuner cost reduction.
- Withstanding to ESD; Build in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; CMPAK-6

Outline

CMPAK-6



1. Drain(1)
2. Source
3. Gate-1(1)
4. Gate-1(2)
5. Gate-2
6. Drain(2)

Notes: 1. Marking is “DM”.
2. TBB1004 is individual type number of HITACHI TWIN BBFET.

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 -0	V
Gate2 to source voltage	V_{G2S}	+6 -0	V
Drain current	I_D	30	mA
Channel power dissipation	Pch[*3]	250	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 3. Value on the glass epoxy board (49mm × 38mm × 1mm).

Electrical Characteristics (Ta = 25°C)

The below specification are applicable for UHF unit (FET1)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5V, V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.7	1.0	V	V_{DS} = 5V, V_{G2S} = 4V, I_D = 100µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.7	1.0	V	V_{DS} = 5V, V_{G1S} = 5V, I_D = 100µA
Drain current	$I_{D(op)}$	13	17	21	mA	V_{DS} = 5V, V_{G1} = 5V V_{G2S} = 4V, R_G = 100kΩ
Forward transfer admittance	$\|y_{fs}\|$	21	26	31	mS	V_{DS} = 5V, V_{G1} = 5V, V_{G2S} =4V R_G = 100kΩ, f = 1kHz
Input capacitance	c_{iss}	1.4	1.8	2.2	pF	V_{DS} = 5V, V_{G1} = 5V
Output capacitance	c_{oss}	1.0	1.4	1.8	pF	V_{G2S} =4V, R_G = 100kΩ
Reverse transfer capacitance	c_{rss}	—	0.02	0.04	pF	f = 1MHz
Power gain	PG	16	21	—	dB	V_{DS} = V_{G1} = 5V, V_{G2S} = 4V R_G = 100kΩ, f = 900MHz Zi=S11*, Zo=S22*(:PG)
Noise figure	NF	—	1.7	2.5	dB	Zi=S11opt (:NF)

Electrical Characteristics (Ta = 25°C)

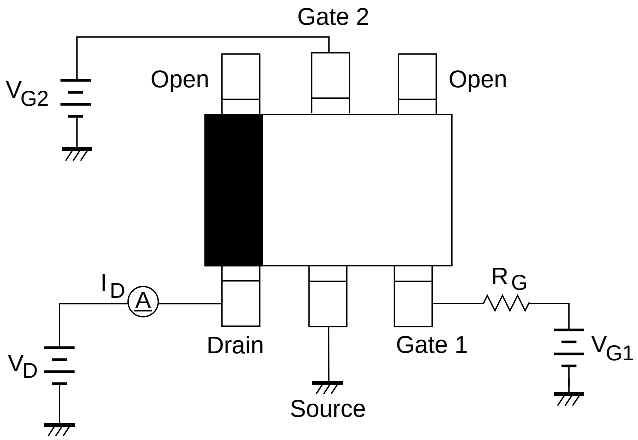
The below specification are applicable for VHF unit (FET2)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5V, V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.75	1.0	V	V_{DS} = 5V, V_{G2S} = 4V, I_D = 100µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.75	1.0	V	V_{DS} = 5V, V_{G1S} = 5V, I_D = 100µA
Drain current	$I_{D(op)}$	16	20	24	mA	V_{DS} = 5V, V_{G1} = 5V, V_{G2S} = 4V, R_G = 100kΩ
Forward transfer admittance	$\|y_{fs}\|$	27	32	37	mS	V_{DS} = 5V, V_{G1} = 5V, V_{G2S} =4V R_G = 100kΩ, f = 1kHz
Input capacitance	c_{iss}	2.3	2.7	3.1	pF	V_{DS} = 5V, V_{G1} = 5V
Output capacitance	c_{oss}	1.4	1.8	2.2	pF	V_{G2S} =4V, R_G = 100kΩ
Reverse transfer capacitance	c_{rss}	—	0.03	0.05	pF	f = 1MHz
Power gain	PG	24	29	—	dB	V_{DS} = V_{G1} = 5V, V_{G2S} = 4V
Noise figure	NF	—	1.2	1.7	dB	R_G = 100kΩ, f = 200MHz

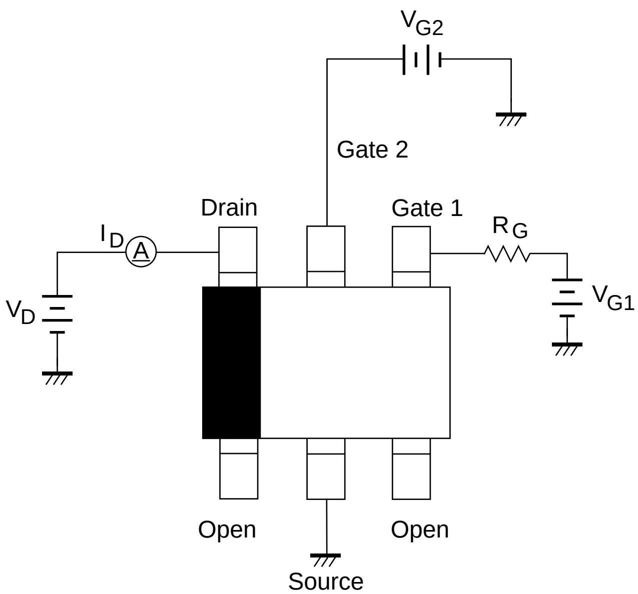
Test Circuits

- **DC Biasing Circuit for Operating Characteristic Items** ($I_{D(op)}$, |yfs|, Ciss, Coss, Crss, NF, PG)

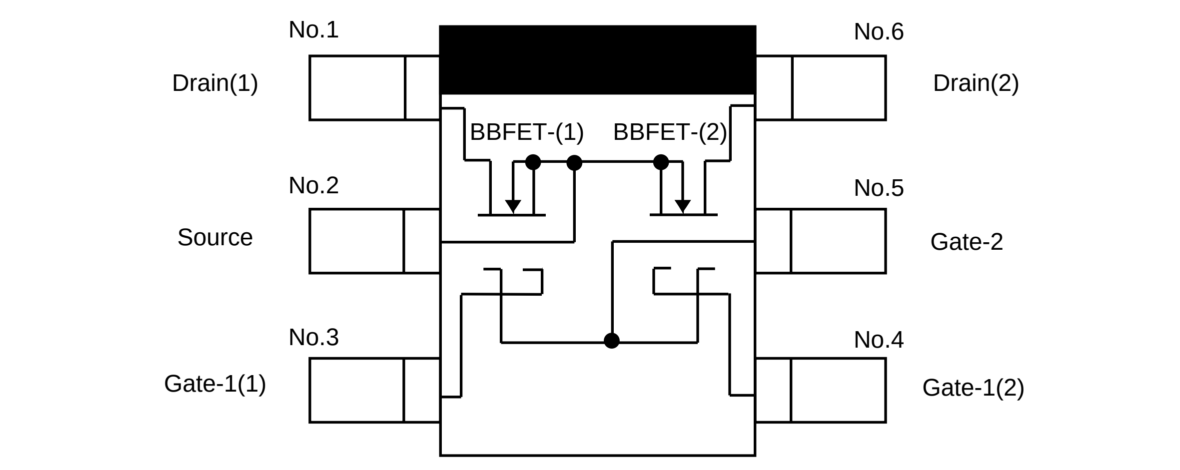
Measurment of FET1



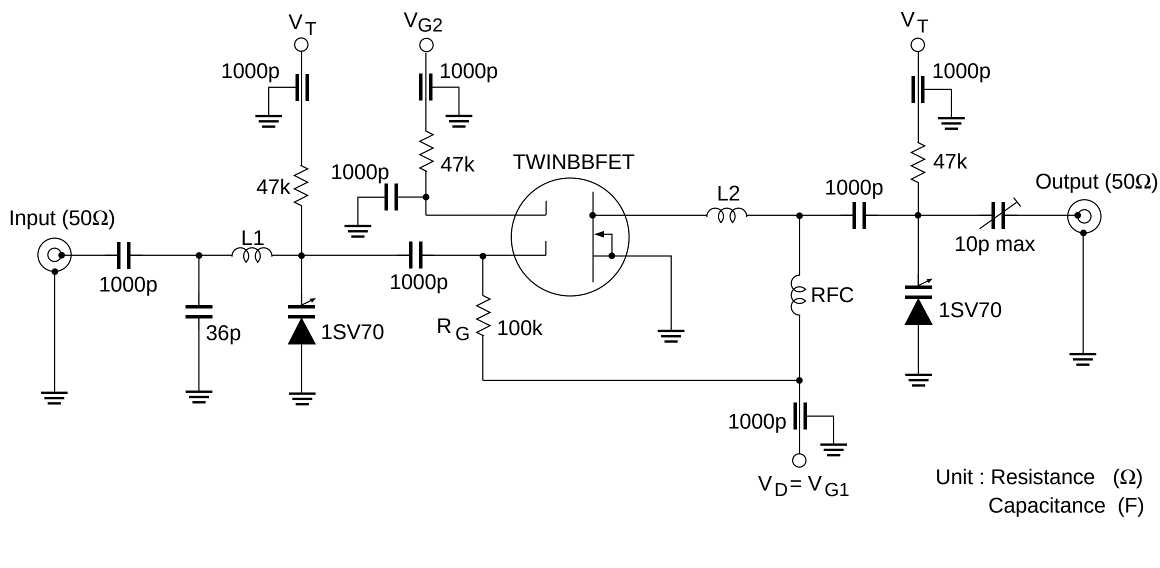
Measurment of FET2



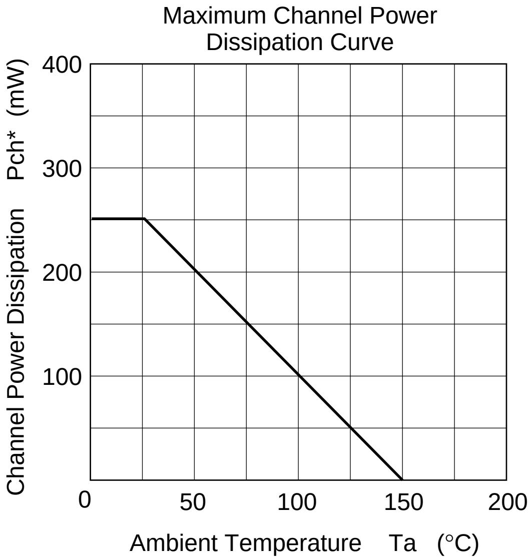
- **Equivalent Circuit**



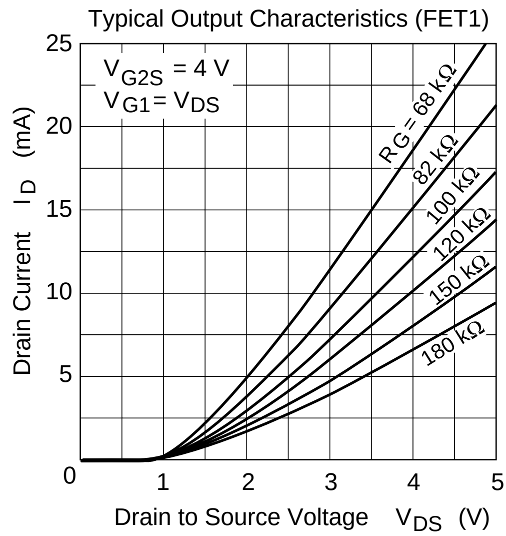
- **200 MHz Power Gain, Noise Figure Test Circuit**

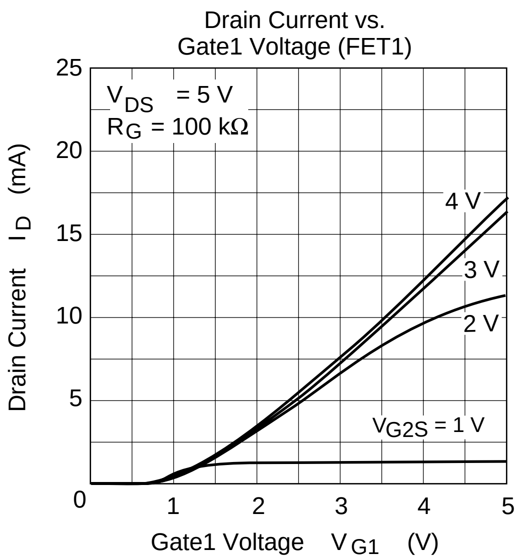


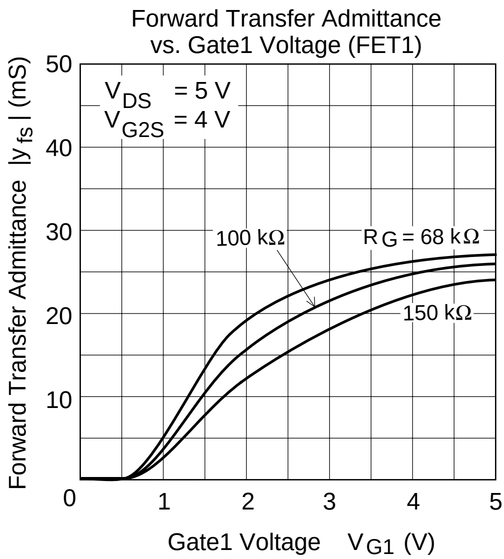
L1 : ϕ1mm Enameled Copper Wire,Inside dia 10mm, 2Turns
L2 : ϕ1mm Enameled Copper Wire,Inside dia 10mm, 2Turns
RFC : ϕ1mm Enameled Copper Wire,Inside dia 5mm, 2Turns

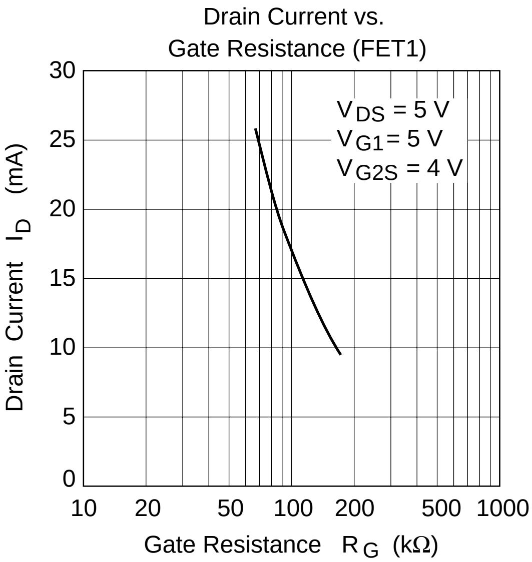


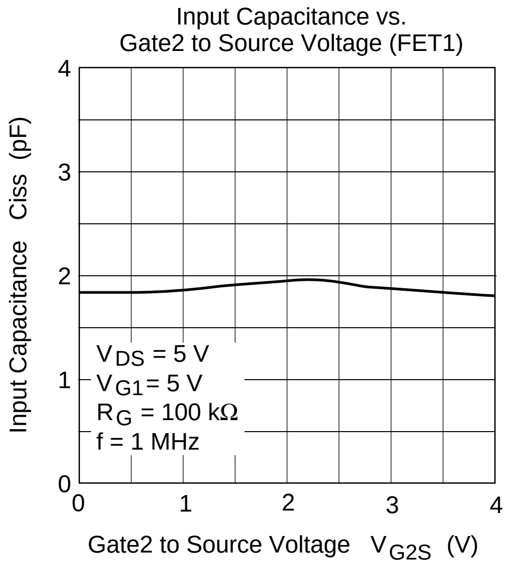
* Value on the glass epoxy board (49mm × 38mm × 1mm)

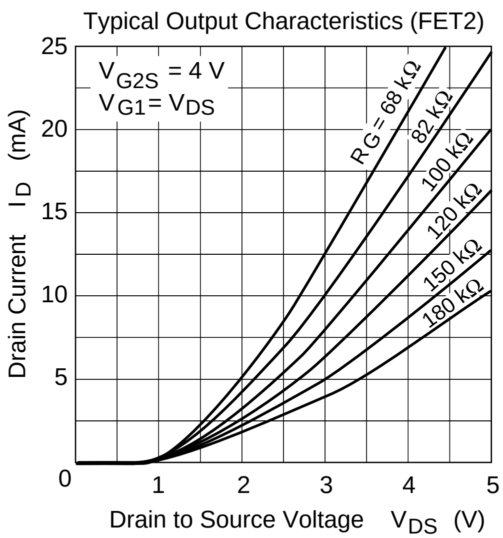


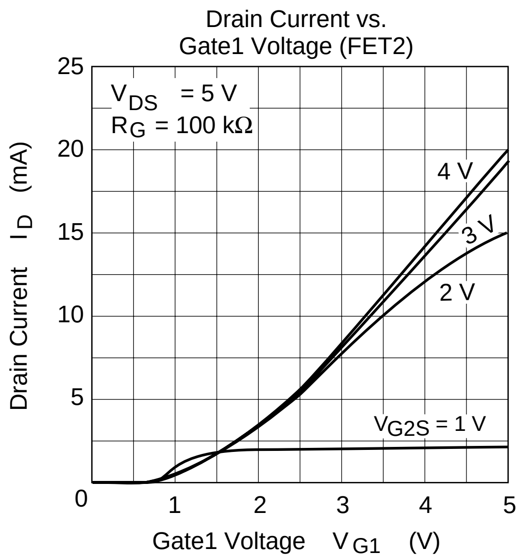


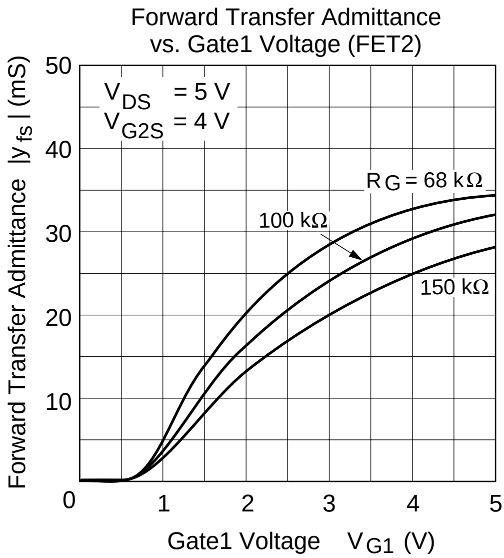


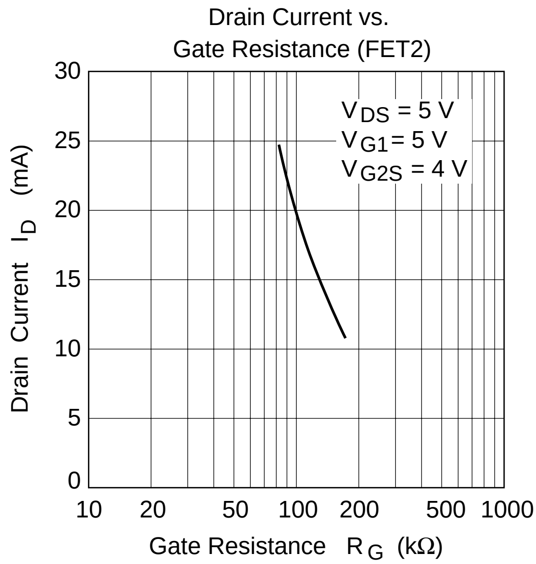

Drain Current vs.
Gate Resistance (FET1)
VDS = 5 V
VG1 = 5 V
VG2S = 4 V
Drain Current ID (mA)
Gate Resistance RG (kΩ)
30
25
20
15
10
5
0
10
20
50
100
200
500
1000

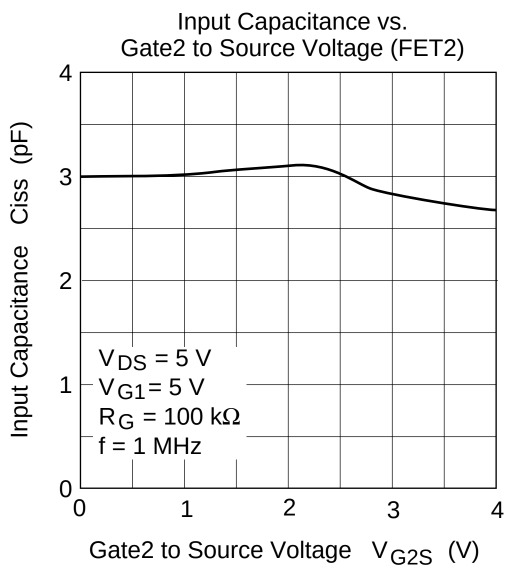

Input Capacitance vs.
Gate2 to Source Voltage (FET1)
VDS = 5 V
VG1 = 5 V
RG = 100 kΩ
f = 1 MHz
Input Capacitance Ciss (pF)
Gate2 to Source Voltage VG2S (V)
4
3
2
1
0
0
1
2
3
4

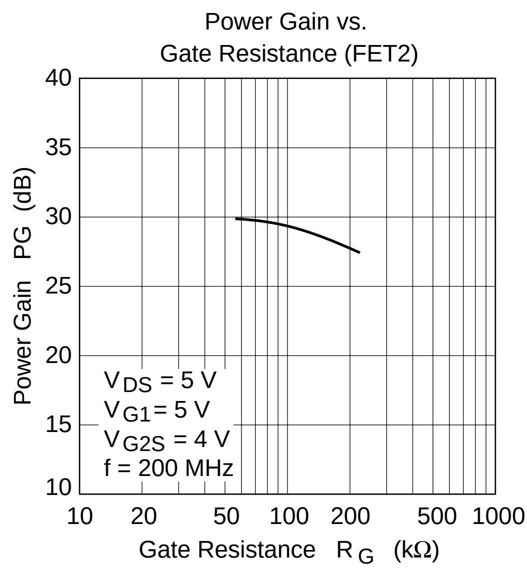

Typical Output Characteristics (FET2)
VG2S = 4 V
VG1 = VDS
RG = 68 kΩ
82 kΩ
100 kΩ
120 kΩ
150 kΩ
180 kΩ
Drain Current ID (mA)
Drain to Source Voltage VDS (V)
25
20
15
10
5
0
1
2
3
4
5

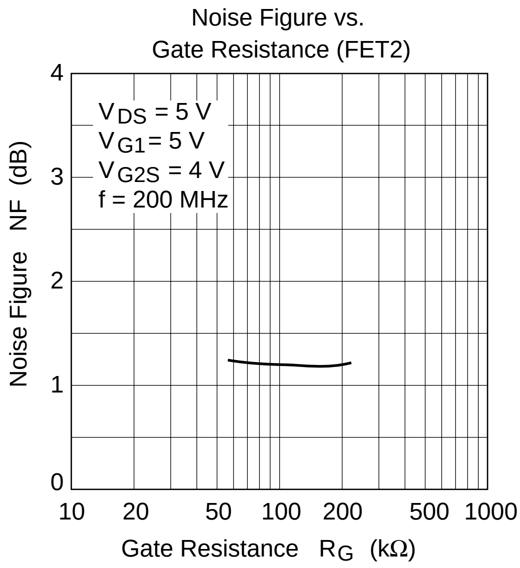

Drain Current vs.
Gate1 Voltage (FET2)
VDS = 5 V
RG = 100 kΩ
4 V
3 V
2 V
VG2S = 1 V
Drain Current ID (mA)
Gate1 Voltage VG1 (V)
25
20
15
10
5
0
1
2
3
4
5

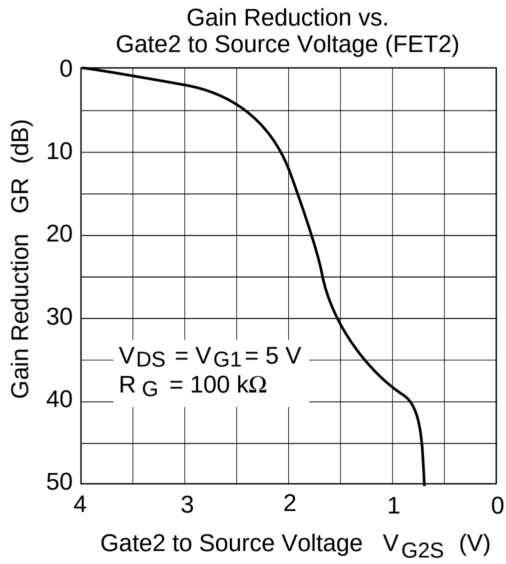

Forward Transfer Admittance
vs. Gate1 Voltage (FET2)
VDS = 5 V
VG2S = 4 V
RG = 68 kΩ
100 kΩ
150 kΩ
Forward Transfer Admittance |yfs| (mS)
Gate1 Voltage VG1 (V)
0
1
2
3
4
5
10
20
30
40
50


Drain Current vs.
Gate Resistance (FET2)
VDS = 5 V
VG1 = 5 V
VG2S = 4 V
Drain Current ID (mA)
Gate Resistance RG (kΩ)
0
5
10
15
20
25
30
10
20
50
100
200
500
1000


Input Capacitance vs.
Gate2 to Source Voltage (FET2)
VDS = 5 V
VG1 = 5 V
RG = 100 kΩ
f = 1 MHz
Input Capacitance Ciss (pF)
Gate2 to Source Voltage VG2S (V)
0
1
2
3
4

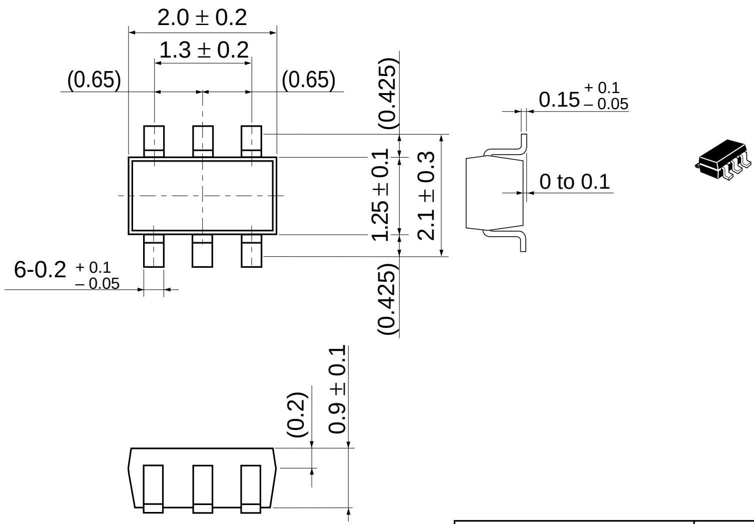

Power Gain vs.
Gate Resistance (FET2)
VDS = 5 V
VG1 = 5 V
VG2S = 4 V
f = 200 MHz
Power Gain PG (dB)
Gate Resistance RG (kΩ)
10
15
20
25
30
35
40
10
20
50
100
200
500
1000


Noise Figure vs.
Gate Resistance (FET2)
VDS = 5 V
VG1 = 5 V
VG2S = 4 V
f = 200 MHz
Noise Figure NF (dB)
4
3
2
1
0
10
20
50
100
200
500
1000
Gate Resistance RG (kΩ)


Gain Reduction vs.
Gate2 to Source Voltage (FET2)
VDS = VG1 = 5 V
R G = 100 kΩ
Gain Reduction GR (dB)
0
10
20
30
40
50
4
3
2
1
0
Gate2 to Source Voltage VG2S (V)

Package Dimensions

As of January, 2001
Unit: mm



Hitachi Code	CMPAK-6
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.006 g

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