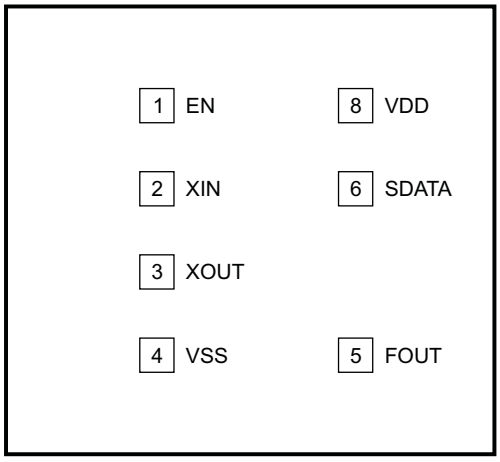
OSCILLATOR IC WITH ELECTRONIC CALIBRATION

FEATURES

- **Oscillator Gain Stage Implemented**
- **One LVCMOS Frequency Output**
- **Frequency Range of Oscillator Gain Stage = 20 MHz–100 MHz**
- **Frequency Range of LVCMOS Output = 0.625 MHz–100 MHz**
- **Electronic Trimming of Oscillator Using Capacitance Arrays**
- **Programmable Post Dividers x, x/2, x/4, x/8, x/16, x/32**
- **Nonvolatile Storage of Settings Using EEPROM Technology**
- **Easy One-Wire *In-Circuit Programming* Allows Programming and Trimming of Oscillator After Manufacturing**
- **EEPROM Programming Without the Need to Apply High Voltage to the Device**
- **Available as Die**
- **Small Form Factor From Less Than 1 mm × 1 mm, Allowing the Smallest Form Factor Available for Today's and Next-Generation Oscillators**
- **Industrial Temperature Range –40°C to 85°C**
- **Wide VDD Range: 2.25 V up to 3.3 V**
- **ESD Protection Exceeds JESD22**
  - **>2000-V Human-Body Model (A114-B)**
  - **>200-V Machine Model (A115_A)**
  - **>500-V Charged-Device Model (C101-B.01)**

Die Terminal Assignment
(Top View = Bond Pad View)



≈ 1 mm × 1 mm

M0018-03

DESCRIPTION

The CDCE401 is designed to achieve today's demanding challenges for crystal oscillator modules. The small form factor of the unpackaged die or the QFN package reduces the space consumption of the device to the technical minimum level of today's silicon technology.

The on-die trimming capacitance allows frequency trimming of the oscillator module after the manufacturing process. Therefore, by doing a post-manufacturing programming, crystal manufacturing tolerances can be trimmed out.

During power up or with each enabling, the CDCE401 oscillator start-up circuit switches off all oscillator capacitors (CXI, CXO, CBASE) to maximize negative impedance during start-up. After a certain time (1/XTAL-frequency × 2^{17} ~ 1.311 ms–6.554 ms), the capacitances are connected to tune to the trimmed frequency range.

An on-die EEPROM enables nonvolatile storage of the frequency setting. For the transfer of the programming into the EEPROM, the CDCE401 takes advantage of the SDATA input. In-circuit programming of the device is possible.

Unlike other EEPROM-based devices, it is not necessary to apply a high supply voltage to the device in order to program it.

The CDCE401 accepts crystals from 20 MHz up to 100 MHz. For lower frequencies, the CDCE401 provides a programmable post-divider.

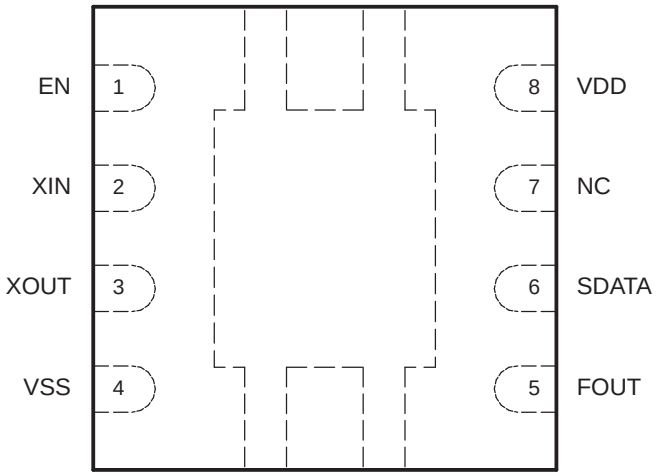
The CDCE401 features a wide supply-voltage range. This makes the device ideal to use at today's most commonly used supply voltage of 2.5 V, and operation at supply voltages of 2.8 V, 2.85 V, and 3 V for cellular applications can be addressed with a single device. Therefore, use of the device in multiple different application spaces is possible, reducing inventory costs.

The CDCE401 is characterized to work in the industrial temperature range from –40°C to 85°C.

Optional: QFN Package Terminal Assignment

For evaluation purposes, the CDCE401 is also available in a QFN package. The packaged device can be obtained together with an EVM.

DRB PACKAGE
(TOP VIEW)



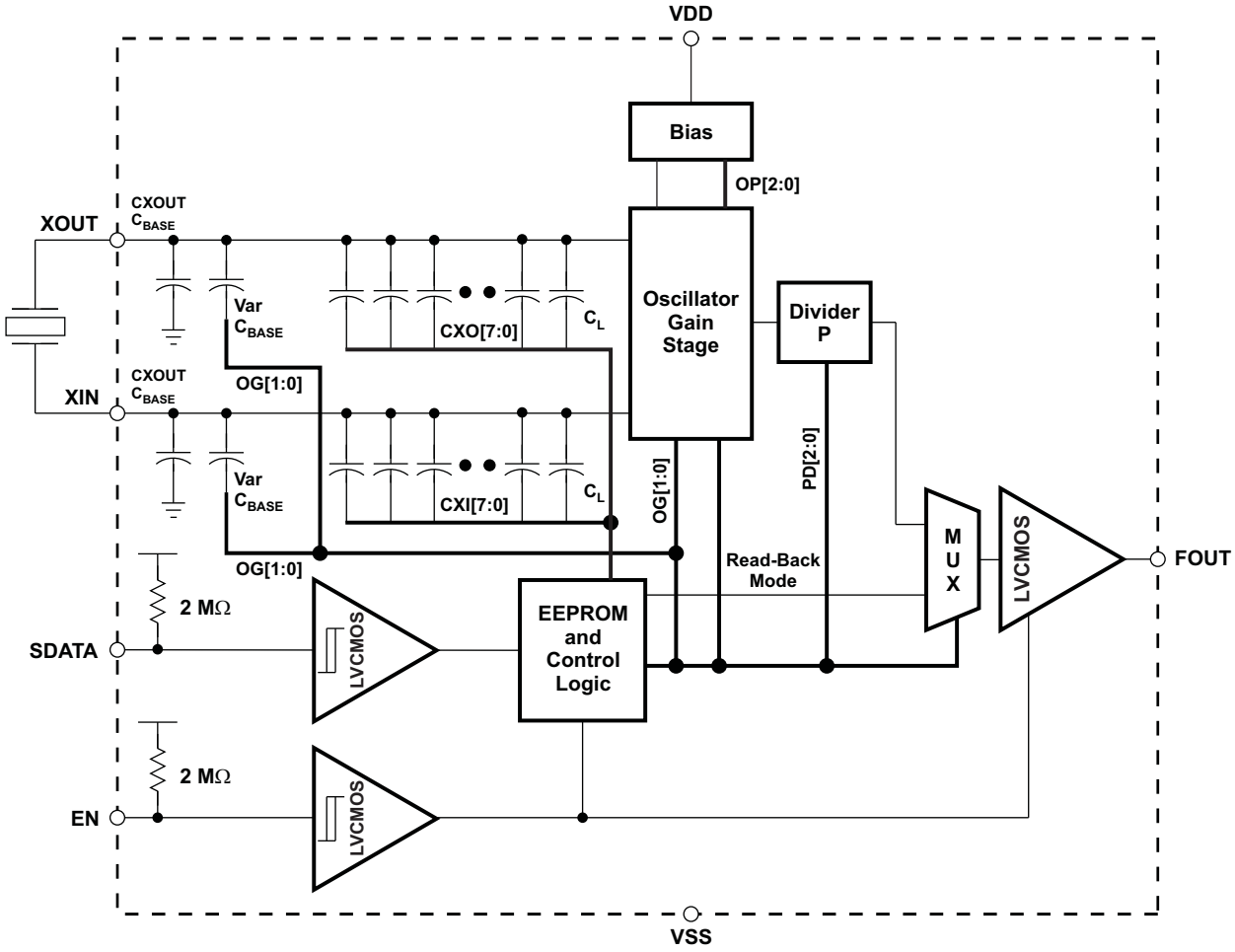
NC − No internal connection

P0012-01

Table 1. TERMINAL FUNCTIONS

TERMINAL			TYPE	DESCRIPTION
NAME	NUMBER			
	QFN	BOND PAD		
EN	1	1	Input LVCMOS	Logic select pin. Enables/disables device. Has a hysteresis of 300 mV. A 2-MΩ pullup resistor is built in.
FOUT	5	5	Output LVCMOS	Frequency output
NC	7	N/A		Not connected
SDATA	6	7	Input LVCMOS	Logic select pin. This input serves as programming input. Has a hysteresis of 300 mV. A 2-MΩ pullup resistor is built in.
VDD	8	8	Power	Voltage supply
VSS	4	4	Ground	Ground
XIN	2	2	Input oscillator	Crystal oscillator input
XOUT	3	3	Output oscillator	Crystal oscillator output

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

CONTROL PIN EN: Enable

The functions of the EN control pin are listed and explained in Table 2.

Table 2. EN Control Pin Functions

EN	FUNCTION
0	Disabled: all current sources are switched off, output is in the high-impedance state.
1	Enabled: output follows the XIN/XOUT oscillation.

SINGLE-PIN INTERFACE CONTROL COMMANDS

The CDCE401 can be configured and programmed via the SDATA input pin. For this purpose, a pulse-code-shaped signal must be applied to the device as shown in the waveforms of Figure 1 to select one of the operation modes described in the *State Flow-Diagram of the Single-Pin Interface* section. During the EEPROM programming phase, the device requires a stable VDD of 3.2 V ±100 mV for secure writing of the EEPROM cells. After each *Write-to-WordX*, the written data is latched, made effective, and offers look-ahead before the actual data is stored into the EEPROM.

Table 3 summarizes all valid programming commands.

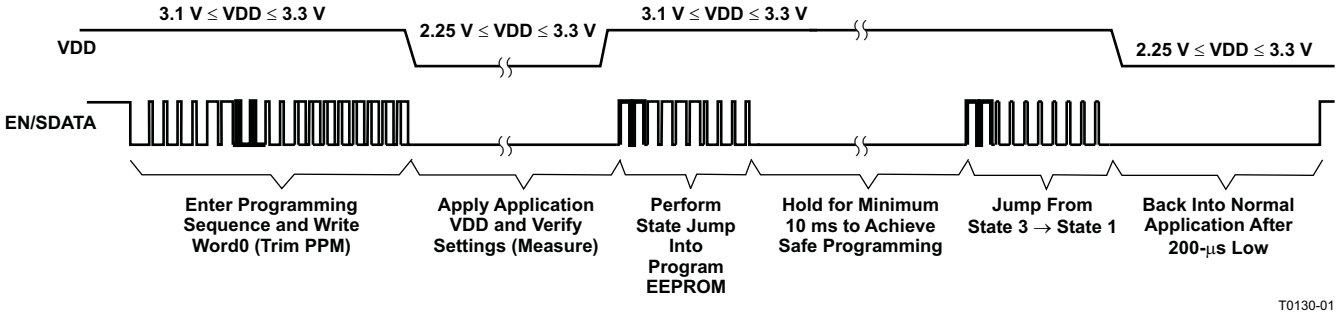


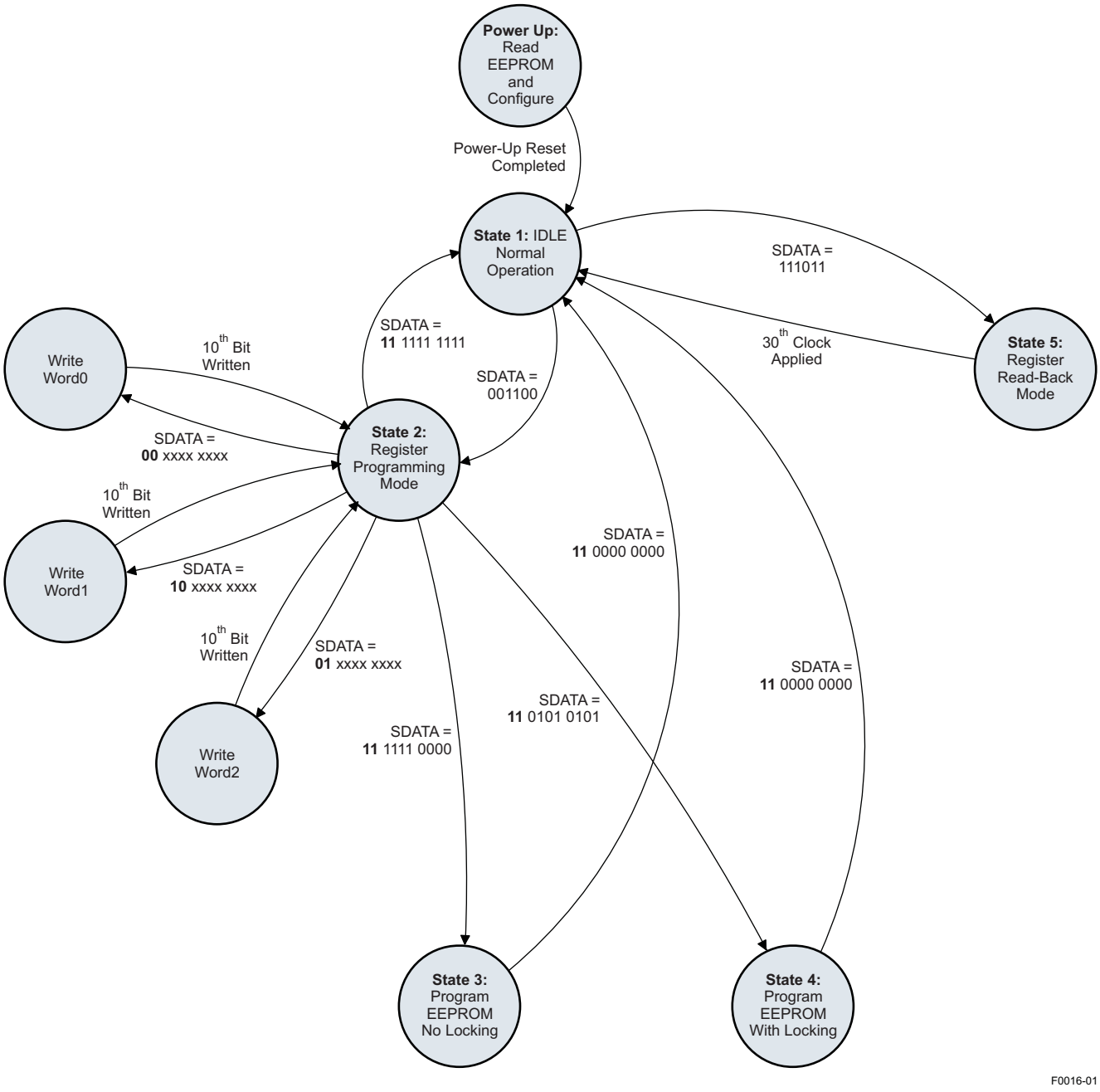
Figure 1. Typical Programming Cycle

Table 3. Single-Pin Interface Control Commands

SDATA	FUNCTION
00 1100	Enter **register programming mode** (state 1 → state 2); bits must be sent in the specified order with the specified timing. Otherwise, a time-out occurs.
11 1011	Enter **register read-back mode**; bits must be sent in the specified order with the specified timing. Otherwise a time-out occurs.
00 xxxx xxxx	**Write-to-word0** (state 2) (1)(2)(3)
10 xxxx xxxx	**Write-to-word1** (state 2) (1) (2) (3)
01 xxxx xxxx	**Write-to-word2** (state 2) (1) (2) (3)
11 xxxx xxxx	**State-machine jump**: All other patterns not defined as follows cause *exit to normal mode.*
11 1111 1111	Jump: **Exit write-to-RAM** (state 2 → state 1)
11 1111 0000	Jump: **Enter EEPROM programming without an EEPROM lock** (state 2 → state 3)
11 0101 0101	Jump: **Enter EEPROM programming with EEPROM lock** (state 2 → state 4)
11 0000 0000	Jump: **Exit EEPROM programming** (state 3 or state 4 → state 1)

(1) Each rising edge causes a bit to be latched.
(2) Between the bits, some longer time delays can occur, but this has no effect on the data.
(3) A *Write-to-WordX* is expected to be 10 bits long. After the 10th bit, the respective word is latched, and its effect can be observed as *look-ahead* function.

STATE FLOW-DIAGRAM OF THE SINGLE-PIN INTERFACE



NOTE: In states 2, 3, 4, and 5, the signal pin EN is disregarded and has no influence on power down.

ENTER REGISTER PROGRAMMING MODE

Figure 2 shows the timing behavior of data to be written into SDATA. The sequence shown is 00 1100. If the high period is as short as t1, this is interpreted as a 0. If the high period is as long as t3, this is interpreted as a 1. This behavior is achieved by shifting the incoming signal SDATA by time t_5 into signal SDATA_DELAYED. As can be seen in Figure 2, SDATA_DELAYED can be used to latch (or strobe) SDATA. The specification for the timings t_1 – t_8, t_r, and t_f are given in the *Timing Requirements* section of this document.

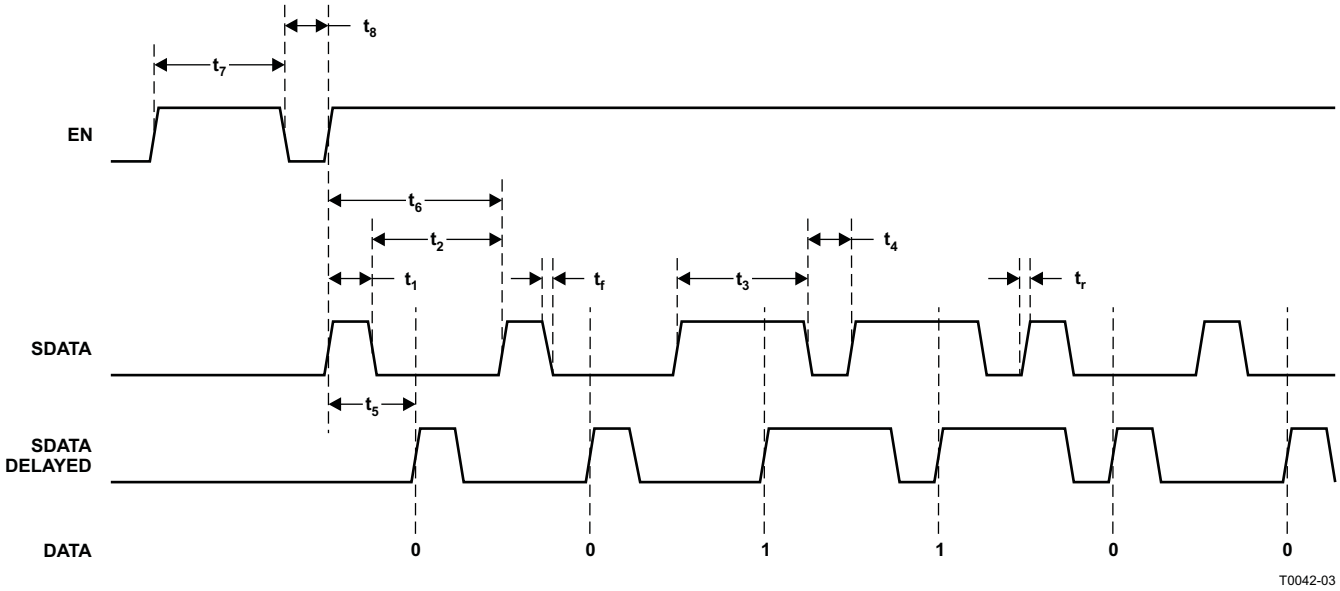


Figure 2. Timing Diagram for SDATA Programming

TYPICAL CYCLE, PROGRAMMING THREE WORDS INTO EEPROM

Figure 3 shows an *enter register programming mode* and how the different words can be written. Bold highlights the addressing of word0–word2. After that, the payload for the respective word is clocked in. In this example, this is followed by a jump from state 2 → state 3 into *enter EEPROM programming with EEPROM lock*. In the EEPROM-programming state, it is necessary to wait at least 10 ms for safe programming. The last command is a jump from state 3 into state 1 (normal operation).

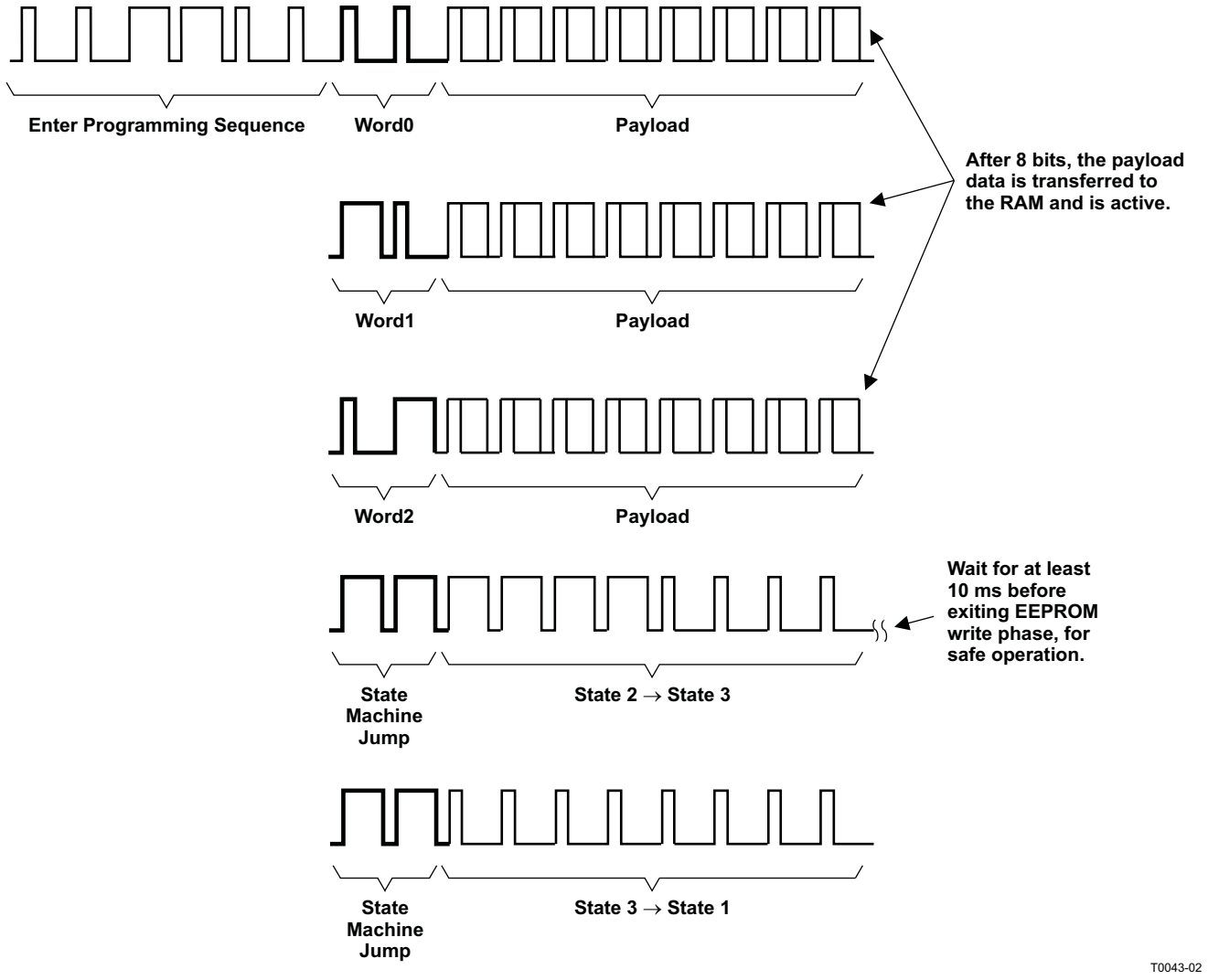


Figure 3. EEPROM Programming Example

TYPICAL WRITE/VERIFY/PROGRAM CYCLE

As stated previously in this document, for safe writing and programming, the supply voltage must be held within a narrow window of 3.2 V ±100 mV. Figure 1 illustrates writing to the device and verifying the settings, followed by a safe programming into EEPROM.

ENTER *REGISTER READ-BACK MODE*

Similar to the *enter registerprogramming mode* sequence, the *enter register read-back mode* is written into SDATA. Before the *enter register read-back mode* is written, the device must be disabled via EN for 100 µs to ensure that the EEPROM content is read out correctly with *enter register read-back mode*. After the command has been issued, the SDATA input is reconfigured as a clock input. By applying one clock, the EEPROM content is read into shift registers. Now, by further applying clocks at SDATA, the EEPROM content can be clocked out and observed at FOUT. Also, FOUT is reconfigured during that operation, as can be seen in the following figure. There are 29 bits to be clocked out. With the 30th falling clock edge, the FOUT pin is reconfigured back to normal operation.

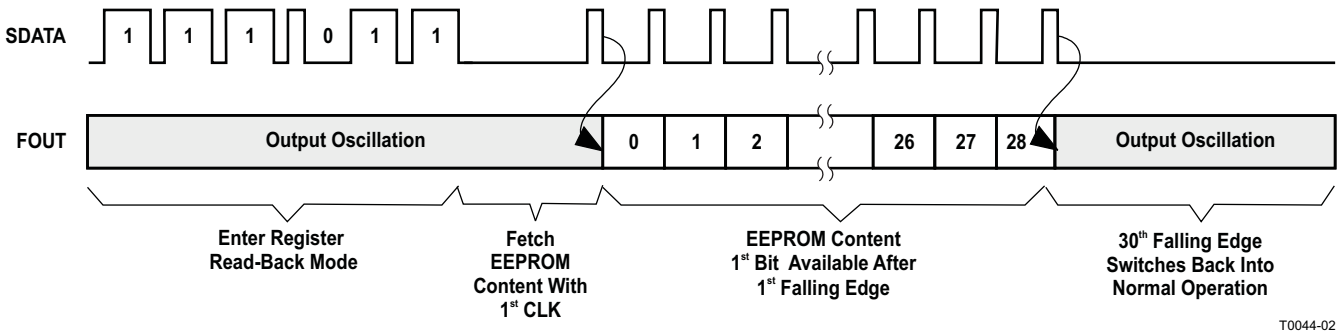


Figure 4. Typical Register Read-Back Cycle

In Table 4, the content of the bits in the output stream is summarized. Note that the MSB is clocked out first.

Table 4. Read-Back Cycle Bit Stream

OUTPUT-STREAM BITS	FUNCTION
Bits[0:2]	Revision identifier (MSB first)
Bit[3]	EEPROM status: 0 = EEPROM has never been written. 1 = EEPROM has been programmed before.
Bit[4]	EEPROM lock: 0 = EEPROM can be rewritten. 1 = EEPROM is locked; rewriting to the EEPROM is not possible.
Bits[5:12]	Storage value, word2 (MSB first)
Bits[13:20]	Storage value, word1 (MSB first)
Bits[21:28]	Storage value, word0 (MSB first)

REGISTER DESCRIPTION

WORD 0:				
BIT	**NAME**	**DESCRIPTION/FUNCTION**	**TYPE**	**DEFAULT**
0	C0	Register selection	W	0
1	C1	Register selection	W	0
2	CXI0	Load capacitance XIN, bit 0	W	0
3	CXI1	Load capacitance XIN, bit 1	W	0
4	CXI2	Load capacitance XIN, bit 2	W	0
5	CXI3	Load capacitance XIN, bit 3	W	0
6	CXI4	Load capacitance XIN, bit 4	W	0
7	CXI5	Load capacitance XIN, bit 5	W	1
8	CXI6	Load capacitance XIN, bit 6	W	1
9	CXI7	Load capacitance XIN, bit 7	W	0

WORD 1:				
BIT	**NAME**	**DESCRIPTION/FUNCTION**	**TYPE**	**DEFAULT**
0	C0	Register selection	W	1
1	C1	Register selection	W	0
2	CXO0	Load capacitance XOUT, bit 0	W	0
3	CXO1	Load capacitance XOUT, bit 1	W	0
4	CXO2	Load capacitance XOUT, bit 2	W	0
5	CXO3	Load capacitance XOUT, bit 3	W	0
6	CXO4	Load capacitance XOUT, bit 4	W	0
7	CXO5	Load capacitance XOUT, bit 5	W	1
8	CXO6	Load capacitance XOUT, bit 6	W	1
9	CXO7	Load capacitance XOUT, bit 7	W	0

WORD 2:				
BIT	**NAME**	**DESCRIPTION/FUNCTION**	**TYPE**	**DEFAULT**
0	C0	Register selection	W	0
1	C1	Register selection	W	1
2	PD0	Post-divider selection, bit 0	W	0
3	PD1	Post-divider selection, bit 1	W	0
4	PD2	Post-divider selection, bit 2	W	0
5	OG0	Oscillator gain definition, bit 0 (1)	W	1
6	OG1	Oscillator gain definition, bit 1 (1)	W	1
7	OP0	Oscillator operating-point adjustment, bit 0 (1)	W	0
8	OP1	Oscillator operating-point adjustment, bit 1 (1)	W	0
9	OP2	Oscillator operating-point adjustment, bit 2 (1)	W	0

(1) The oscillator gain bits have impact on the capacitance C_{BASE}. See the table for input capacitance values. The oscillator operating-point bits OP[2:0] are used to set the bias point of the oscillator core stage. In combination with setting the post-divider ratio PD[2:0] = 111, the current consumption can be optimized to set oscillator core current consumption for lower frequencies and higher frequencies. This ensures that the oscillator core is in operating optimally for phase noise and low XTAL-drive power. Setting core power too high impacts XTAL-drive power, which affects the lifetime of the crystal.

POST-DIVIDER SETTINGS

PD2	PD1	PD0	POST-DIVIDER SETTINGS	COMMENT
0	0	0	Post-divider × 1	Default
0	0	1	Post-divider × 1/2	
0	1	0	Post-divider × 1/4	
0	1	1	Post-divider × 1/8	
1	0	0	Post-divider × 1/16	
1	0	1	Post-divider × 1/32	
1	1	0	Test mode: turns off CXI, CXO, and C_{BASE}. Post-divider × 1 (like in default).	
1	1	1	No division: The post-divider setting PD[2:0] = 111 is used to turn off the amplifier after the oscillator core. This offers the capability to disable effectively all blocks except the oscillator core (current consumption of core only can be measured and adjusted)(1).	

(1) Setting core current consumption too high impacts the crystal drive power, which affects crystal performance and lifetime.

RECOMMENDATIONS FOR OSCILLATOR GAIN(2) AND OPERATING POINT DEFINITIONS

OG[1:0]	OP[2:0]	OSCILLATOR OSCILLATOR OPERATING FREQUENCY	COMMENT
11	000	Oscillator gain for 20 MHz ≤ frequency < 40 MHz	Default
10	000	Oscillator gain for 40 MHz ≤ frequency < 60 MHz	
01	000	Oscillator gain for 60 MHz ≤ frequency < 80 MHz	
00	000	Oscillator gain for 80 MHz ≤ frequency ≤ 100 MHz	

(2) The oscillator gain bits have an impact on the capacitance C_{BASE}. See the table for input capacitance values. This table is valid for the whole supply voltage range. Depending on the crystal series equivalent resistance, the OP[2:0] bits might require different settings. Contact TI for assistance.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
VDD	Supply voltage range	–0.5 to 8	V
V_I	Input voltage range(2)	–0.5 to VDD + 0.5	V
V_O	Output voltage range(2)	–0.5 to VDD + 0.5	V
	Input current (V_I < 0, V_I > VDD)	±20	mA
I_O	Continuous output current	±50	mA
θ_{JA}	Package thermal impedance:(3) QFN8 package	TBD	K/W
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51 (no-airflow condition) and JEDEC2S2P (high-k board).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SUPPLY VOLTAGES, CURRENTS AND TEMPERATURE RANGE						
VDD	Supply voltage: the four target supply-voltage ranges are: a) 2.5 V ±10% = 2.25 V–2.75 V b) 2.8 V ±10% = 2.52 V–3.08 V c) 2.85 V ±10%= =2.56 V–3.14 V d) 3 V ±10% = 2.7 V–3.30 V		2.25	3	3.3	V
VDD	Supply voltage during configuration of the device and EEPROM writing		3.1	3.2	3.3	V
I_{DD}	Supply current	$f_{CLOCK\text{-}max}$ = 100 MHz, $V_{DD\text{-}max}$ = 3.3 V, $C_{L\text{-}max}$ = 15 pF			20	mA
$I_{DD(DIS)}$	Disable current	f_{IN} = 0 MHz, $V_{DD\text{-}max}$			10	µA
T_A	Operating free-air temperature		–40		85	°C
LVCMOS INPUT PARAMETER (SDATA, EN)						
V_{IH}	High-level input voltage	VDD = 3.3 V	VDD – 0.5		VDD + 0.3	V
V_{IL}	Low-level input voltage	VDD = 3.3 V	V_{SS} – 0.3		V_{SS} + 0.5	V
R_{PULLUP}	Pullup resistor (EN and SDATA)		1.4	2	3.5	MΩ
LVCMOS OUTPUT PARAMETER (FOUT)						
V_{OH}	High-level output voltage	I_{OH} = –6 mA	VDD – 0.3			V
V_{OL}	Low-level output voltage	I_{OL} = 6 mA			V_{SS} + 0.3	V
V_{OH_12mA}	High-level output voltage	I_{OH} = –12 mA	VDD – 0.6			V
V_{OL_12mA}	Low-level output voltage	I_{OL} = 12 mA			V_{SS} + 0.6	V
I_{OZH}/I_{OZL}	Output current in high-impedance state	V_{OUT} = VDD and V_{OUT} = V_{SS}			±10	µA

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load, and operating free-air temperature

PARAMETER				MIN	NOM	MAX	UNIT
XIN/XOUT REQUIREMENTS							
f_{CLK_IN}	Crystal frequency			20		100	MHz
f_{Range}	Trimming range (range is dependent on connected crystal)			±20			ppm
C_{BASE_XIN}	Base input capacitance into XIN, measured single-ended with all CXx turned off	OG0 = 1	OG1 = 1		33		pF
		OG0 = 1	OG1 = 0		30		
		OG0 = 0	OG1 = 1		27		
		OG0 = 0	OG1 = 0		25		

TIMING REQUIREMENTS (continued)

over recommended ranges of supply voltage, load, and operating free-air temperature

PARAMETER				MIN	NOM	MAX	UNIT
C_{BASE_XOUT}	Base input capacitance into XOUT, measured single-ended with all CXx turned off	OG0 = 1	OG1 = 1		25		pF
		OG0 = 1	OG1 = 0		17		
		OG0 = 0	OG1 = 1		16		
		OG0 = 0	OG1 = 0		11		
CXI[7:0] CXO[7:0]	Crystal tune capacitance, measured single-ended against VSS (subtracted from C_{BASE}), i.e.: CXI[0:7] = C_{XIN} – C_{BASE}(OGx) or CXO[0:7] = C_{XOUT} – C_{BASE}(OGx)		CXx7		6		pF
			CXx6		3		
			CXx5		1.5		
			CXx4		0.75		
			CXx3		375		fF
			CXx2		187		
			CXx1		94		
			CXx0		47		
FOUT OUTPUT PARAMETER							
f_{CLK_OUT}	Crystal frequency			20		100	MHz
t_r/t_f	Rise and fall time	10% to 90% VDD and $C_{Load,max}$ = 15 pF			2	3	ns
f_{max}	Highest output frequency	$C_{Load,max}$ = 15 pF				100	MHz
C_{Load}	Load capacitance					15	pF
odc	Output duty cycle	At VDD/2, 20 MHz ≤ freq ≤ 80 MHz		45%	50%	55%	
		At VDD/2, 80 MHz < freq ≤ 100MHz		40%	50%	60%	
SDATA/EN TIMING							
$f_{SDATACLK}$	Repeat frequency of programming				200		kHz
t_1	LOW signal: high-pulse duration			0.5	1	1.2	µs
t_2	LOW signal: low-pulse duration while entering programming sequence			3.8	4	4.2	µs
	LOW signal: low-pulse duration while programming bits			3.8			
t_3	HIGH signal: high-pulse duration			3.8	4	4.5	µs
t_4	HIGH signal: low-pulse duration while entering programming sequence			0.5	1	1.2	µs
	HIGH signal: low-pulse duration while programming bits			0.5			
t_5	Time delay between SDATA signal and SDATA_Delayed signal at VDD = 3.3 V			1.5	2.5	3.5	µs
t_6	Time between bits during *enter programming mode* and *enter read-back mode* beyond which a time-out must occur			10		30	µs
t_7	EN high time before first SDATA can be clocked in			60			µs
t_8	EN low time before first SDATA bit is clocked in			2		10	µs
t_r/t_f	Rise and fall time from 20% to 80% of VDD			1		15	ns

DEVICE CHARACTERISTICS

over recommended ranges of supply voltage, load, and operating free-air temperature (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise specifications under following assumptions for 20-MHz and 40-MHz crystals: f = 20 MHz (L_S = 22.79 mH, C_S = 2.78 fF, C_P = 0.77 pF) and post-divider ×1 f = 40 MHz (L_S = 6.231 mH, C_S = 2.541 fF, C_P = 0.628 pF) and post-divider ×1						
phn_{10}	Phase noise at 10 Hz				–65	dBc/Hz
phn_{100}	Phase noise at 100 Hz				–95	dBc/Hz
phn_{1k}	Phase noise at 1 kHz				–125	dBc/Hz
phn_{10k}	Phase noise at 10 kHz				–140	dBc/Hz
phn_{100k}	Phase noise at 100 kHz				–145	dBc/Hz
phn_{1M}	Phase noise at 1 MHz				–145	dBc/Hz
Phase noise specifications under following assumptions for 60-MHz and 80-MHz crystals: f = 60 MHz (L_S = 2.015 mH, C_S = 3.493 fF, C_P = 0.876 pF) and post-divider ×1 f = 80 MHz (L_S = 0.907 mH, C_S = 4.376 fF, C_P = 1.156 pF) and post-divider ×1						
phn_{10}	Phase noise at 10 Hz				–65	dBc/Hz
phn_{100}	Phase noise at 100 Hz				–95	dBc/Hz
phn_{1k}	Phase noise at 1 kHz				–125	dBc/Hz
phn_{10k}	Phase noise at 10 kHz				–133	dBc/Hz
phn_{100k}	Phase noise at 100 kHz				–140	dBc/Hz
phn_{1M}	Phase noise at 1 MHz				–145	dBc/Hz
Phase noise specifications under following assumptions for 100-MHz crystals: f = 100 MHz (L_S = 0.515 mH, C_S = 4.923 fF, C_P = 1.468 pF) and post-divider ×1						
phn_{10}	Phase noise at 10 Hz				–65	dBc/Hz
phn_{100}	Phase noise at 100 Hz				–90	dBc/Hz
phn_{1k}	Phase noise at 1 kHz				–120	dBc/Hz
phn_{10k}	Phase noise at 10 kHz				–130	dBc/Hz
phn_{100k}	Phase noise at 100 kHz				–135	dBc/Hz
phn_{1M}	Phase noise at 1 MHz				–145	dBc/Hz

(1) All parameters are defined for the test load given in SubSec1 5.1.

TEST LOAD CONDITION

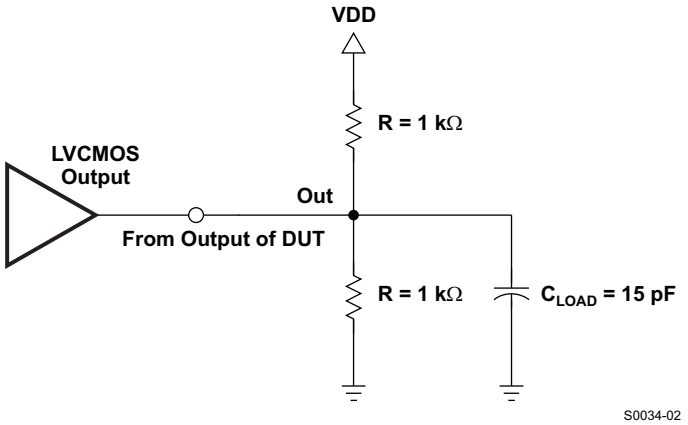


Figure 5. LVCMOS Output Test Load for All Specifications Except Phase Noise Values

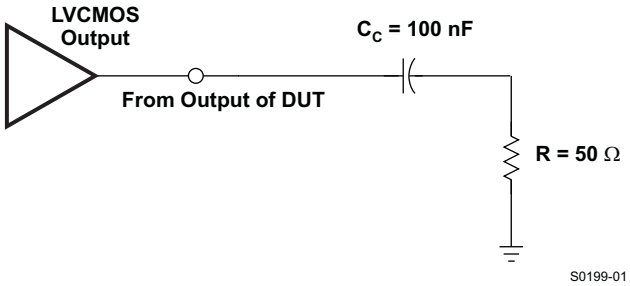


Figure 6. LVCMOS Output Test Load for Phase Noise Values

APPLICATION INFORMATION

CRYSTAL OSCILLATOR LEVEL CONVERSION

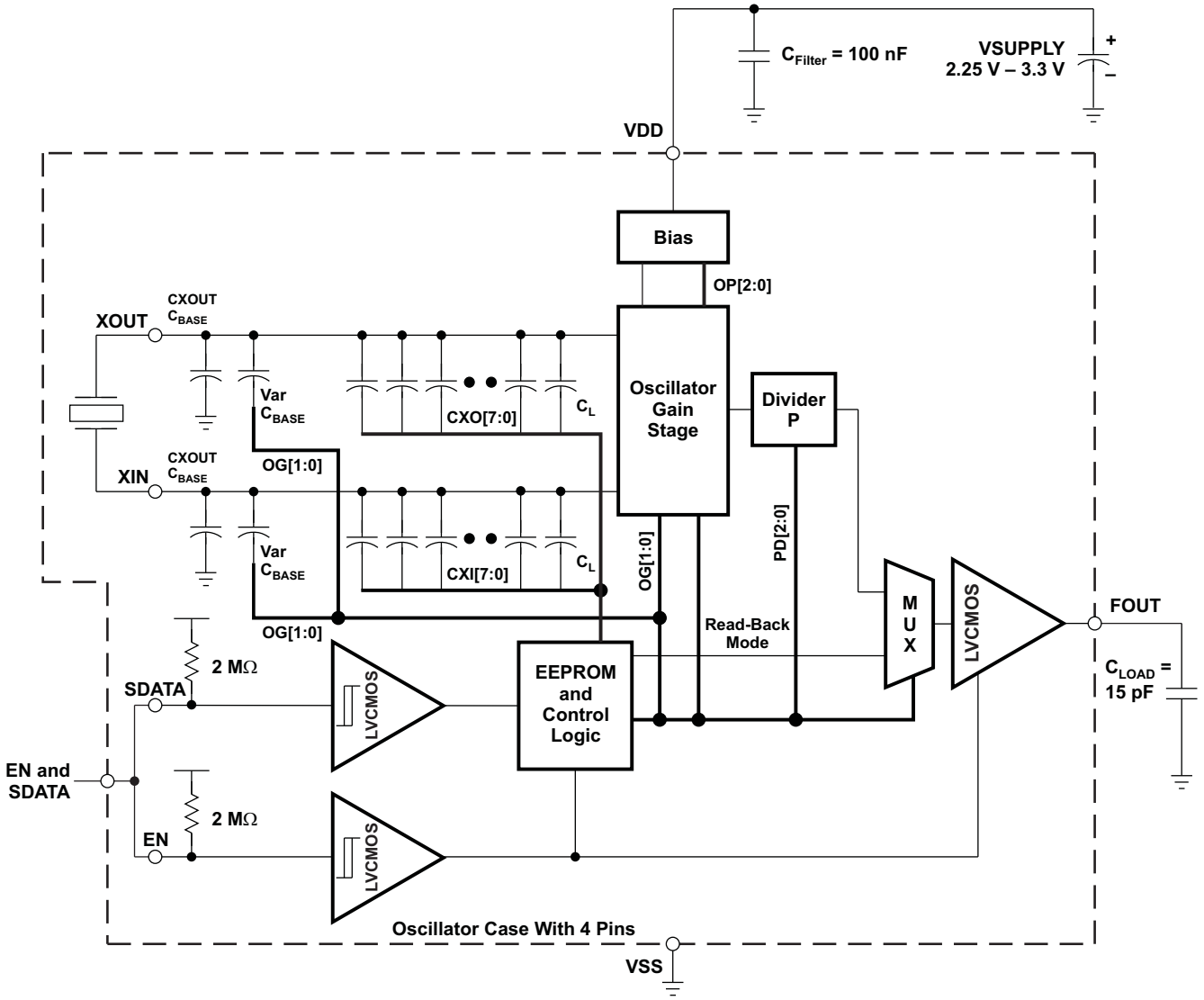
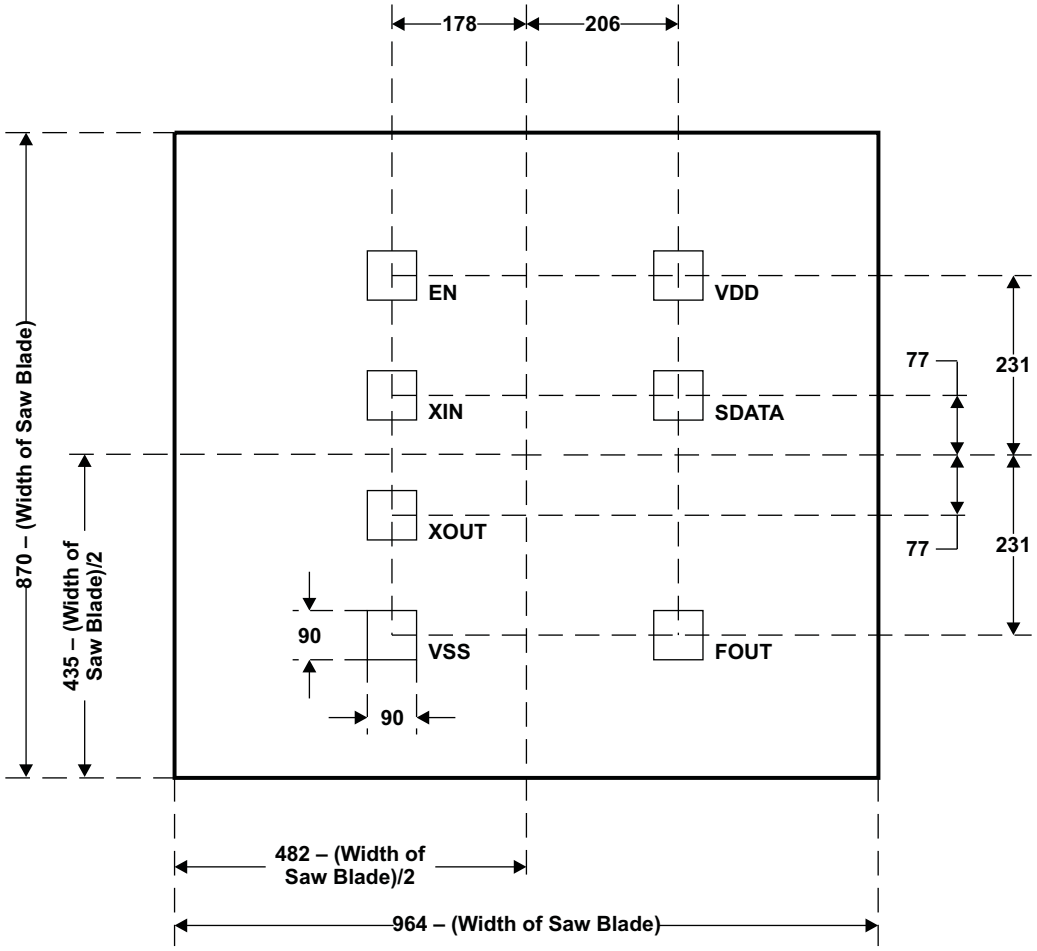


Figure 7. Crystal Oscillator Application at 40 MHz in a 4-Pin Oscillator Case

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise specifications under following assumptions: Crystal with f = 40 MHz (L_S = 10.534 mH, C_S = 2.208 pF, C_P = 0.551 pF) and post-divider ×1						
phn_{10}	Phase noise at 10 Hz	VDD = 2.5 V		–70		dBc/Hz
phn_{100}	Phase noise at 100 Hz	VDD = 2.5 V		–100		dBc/Hz
phn_{1k}	Phase noise at 1 kHz	VDD = 2.5 V		–130		dBc/Hz
phn_{10k}	Phase noise at 10 kHz	VDD = 2.5 V		–145		dBc/Hz
phn_{100k}	Phase noise at 100 kHz	VDD = 2.5 V		–150		dBc/Hz
phn_{1M}	Phase noise at 1 MHz	VDD = 2.5 V		–150		dBc/Hz



Note: All Units μm

M0018-04

Figure 8. Die Dimensions (Top View – Bond Pad Locations)

PACKAGING INFORMATION

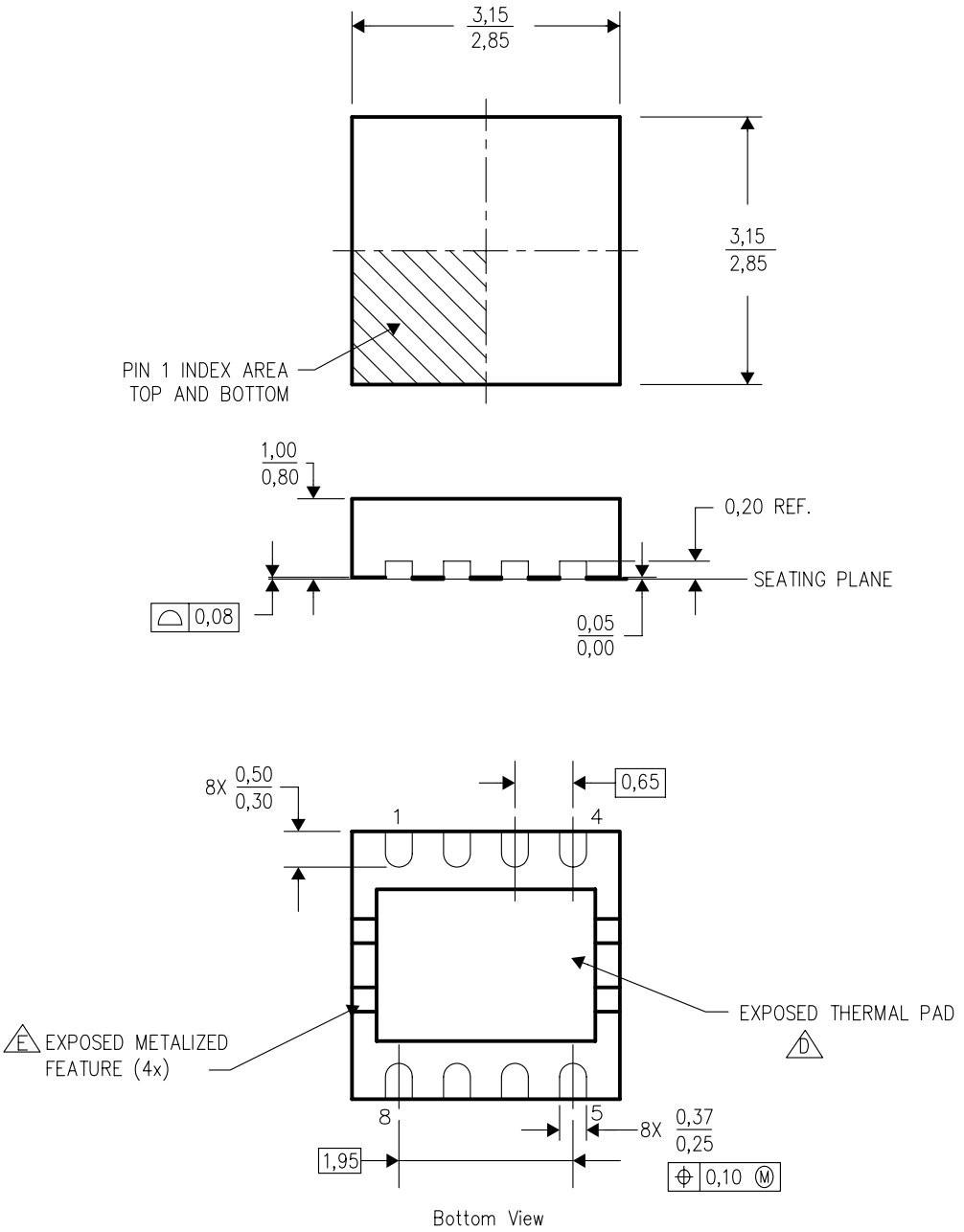
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CDCE401YS	PREVIEW	XCEPT	YS	0		Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DRB (S–PDSO–N8) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

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