## Design Idea DI-101 DPA-Switch Under-Voltage with Wide Hysteresis

| Application | Device | Power Output | Input Voltage | Output Voltage | Topology |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PoE/VoIP | DPA423G | - | $34-57$ VDC | - | - |

## Design Highlights

- High hysteresis under-voltage lockout for Power over Ethernet (PoE) Powered Devices (PDs)
- Turn-on threshold of 42 VDC and turn-off threshold of 34 VDC
- Compliance to PoE standard (IEEE 802.3af) over complete voltage window ensures compatibility with PSE equipment. Tested by University of New Hampshire Interoperability Consortium (UNH-IOC)*


## Wide Hysteresis Under-Voltage

The default under-voltage lockout and overvoltage shutdown thresholds of the DPA-Switch are programmed with a single resistor $\left(\mathrm{R}_{\mathrm{LS}}\right)$ connected from the positive input voltage to the L-pin. The default overvoltage and under-voltage thresholds have a fixed ratio (ratio approximately 2.7:1).

In a PoE system, the Power Sourcing Equipment (PSE) provides a minimum operating voltage of 44 VDC. However, the PoE specification allows CAT-5 (Ethernet) cable lengths up to 100 meters/ 300 ft (with up to $20 \Omega$ of cable impedance). At peak operating current $(350 \mathrm{~mA})$, the voltage at the PD can drop to approximately


Figure 1. DPA-Switch with Wide Hysteresis UVLO.

37 VDC ( $350 \mathrm{~mA} \times 20 \Omega$ ). A minimum of 7 VDC undervoltage hysteresis is required to accommodate the cable drop voltage and prevent nuisance lockouts from occurring.

## Operation

This circuit takes advantage of accurate DPA-Switch L-pin current sensing as the basis for a new composite threshold, programmed for 42 VDC turn-on and 34 VDC turn-off. The DPA-Switch detects the input voltage via current in the L-pin resistor $\mathrm{R}_{\mathrm{LS}}$. Above an UV-on threshold $(50 \mu \mathrm{~A})$, the DPA-Switch begins switching and below an UV-off threshold $(47 \mu \mathrm{~A})$, the DPA-Switch is disabled. Transistor Q1 is turned on via bias resistor R2, causing a voltage drop across R3 and subtracting a fixed current of approximately $10 \mu \mathrm{~A}$ (moving the effective threshold to $60 \mu \mathrm{~A}$ ) from the L-pin. When the power supply becomes operational, the bias voltage pulls up via R1, turning off Q1, cutting off the R3 current and returning to the default UV-off threshold $(47 \mu \mathrm{~A})$.


Figure 2. L-Pin Current without/with Wide UVLO Circuit.

## Design Formulae

Component values can be calculated according to the following formulae and parameters:

Design parameters were selected as follows:
$\mathrm{V}_{\mathrm{UV} \text { _ON }}=42$ VDC $\quad$ Input under-voltage on-threshold
$\mathrm{V}_{\text {UV_OfF }}=34$ VDC $\quad$ Default under-voltage offthreshold
$\mathrm{V}_{\mathrm{DIN}}=1.4 \mathrm{VDC}$
$\mathrm{R} 1=10 \mathrm{k} \Omega$

Diode drop for PoE reverse protection input diodes
This value is assumed

From the DPA-Switch data sheet we have the following:
$\mathrm{I}_{\text {UV_ON }}=50 \mu \mathrm{~A}$
$\mathrm{I}_{\mathrm{UV} \text { OFF }}=47 \mu \mathrm{~A}$
$\mathrm{V}_{\mathrm{L}}=2.35 \mathrm{VDC}$
$\mathrm{V}_{\mathrm{C}}=5.8 \mathrm{VDC}$

L-pin current for UV turn on
L-pin current for UV turn off
L-pin voltage at $I_{L}=I_{U V \text { on }}$
Control-pin voltage
We can assume:
$\mathrm{V}_{\mathrm{Q1}(\mathrm{BE})}=0.6 \mathrm{VDC} \quad$ Transistor base-emitter voltage
$\mathrm{V}_{\mathrm{QI}(\mathrm{BE}) \text { REV }}<4 \mathrm{VDC} \quad 80 \%$ of the max reverse base-
emitter voltage
$\beta=100 \quad$ Transistor minimum current gain
Bias Voltage $\left(\mathrm{V}_{\text {BIAs }}\right)=8 \mathrm{VDC}$
Resistor values $\mathrm{R}_{\mathrm{LS}}, \mathrm{R} 2$ and R 3 are calculated as follows:
$R_{L S}=\frac{V_{\text {UV_OFF }}-V_{L}-V_{D I N}}{I_{U V \_O F F}}$
$R_{3}=\frac{\left(V_{L}-V_{Q 1(B E)}\right) \cdot R_{L S}}{V_{U V_{-} O N}-I_{U V_{-} O N} \cdot R_{L S}-V_{L}-V_{D I N}}$
$R_{2}<\frac{R_{1} \cdot\left(V_{\text {QIIBEREV }}+V_{L}\right)}{V_{\text {BASS }}-V_{L}-V_{Q I(B B) R E V}}$

For design verification:

$$
\begin{aligned}
& V_{U V_{-} O N}=\left(I_{U V_{\_} O N}+\frac{V_{L}-V_{Q 1(B E)}}{R_{3}}\right) \cdot R_{L S}+V_{L}+V_{D I N} \\
& V_{U V_{-} O F F}=I_{U V_{-} O F F} \cdot R_{L S}+V_{L}+V_{D I N} \\
& V_{O V \_O F F}=I_{O V_{-} O F F} \cdot R_{L S}+V_{L}+V_{D I N} \\
& V_{Q 1(B E) R E V}=\frac{V_{B I A S} \cdot R_{2}}{R_{1}+R_{2}}-V_{L}
\end{aligned}
$$

## Key Design Points

- Use a $1 \%$ resistor for $\mathrm{R}_{\mathrm{LS}}$ to maintain the highest accuracy for the turn-on/turn-off thresholds.
- The over-voltage threshold is fixed at $\mathrm{I}_{\text {ov_off }}=135 \mu \mathrm{~A}$, and can be calculated according to the formula above $\left(\mathrm{V}_{\text {OV_OFF }}\right)$.
- The bias voltage $\left(\mathrm{V}_{\text {BIAS }}\right)$ is divided by R 2 and R 1 . The reverse base emitter voltage $\mathrm{V}_{\mathrm{Q} 1(\mathrm{BE}) \text { Rev }}$ is the divided bias voltage minus $\mathrm{V}_{\mathrm{L}}$. Make sure $\mathrm{V}_{\mathrm{Q} 1(\mathrm{BE}) \mathrm{REV}}$ stays below 5 V (the transistor rating).
- For PoE applications, make sure to include voltage drops of input diodes ( $\mathrm{V}_{\mathrm{DIN}}$ ) and pass-FET drop when calculating $\mathrm{R}_{\mathrm{LS}}$. For non-PoE applications, assume $\mathrm{V}_{\mathrm{DIN}}=0$.
- Note: Due to the L-pin synchronization function (with a 1 V threshold), resistor R 2 should be sufficiently large to prevent Q1 turn-on below L-pin voltage 1 V .


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