Design Idea DI-101
DPA-Switch® Under-Voltage with Wide Hysteresis

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
PoE/VoIP	DPA423G	-	34-57 VDC	-	-

Design Highlights

- High hysteresis under-voltage lockout for Power over Ethernet (PoE) Powered Devices (PDs)
- Turn-on threshold of 42 VDC and turn-off threshold of 34 VDC
- Compliance to PoE standard (IEEE 802.3af) over complete voltage window ensures compatibility with PSE equipment. Tested by University of New Hampshire Interoperability Consortium (UNH-IOC)*

Wide Hysteresis Under-Voltage

The default under-voltage lockout and overvoltage shutdown thresholds of the *DPA-Switch* are programmed with a single resistor (R_{LS}) connected from the positive input voltage to the L-pin. The default overvoltage and under-voltage thresholds have a fixed ratio (ratio approximately 2.7:1).

In a PoE system, the Power Sourcing Equipment (PSE) provides a minimum operating voltage of 44 VDC. However, the PoE specification allows CAT-5 (Ethernet) cable lengths up to 100 meters/ 300 ft (with up to 20 Ω of cable impedance). At peak operating current (350 mA), the voltage at the PD can drop to approximately 37 VDC (350 mA × 20 Ω). A minimum of 7 VDC under-voltage hysteresis is required to accommodate the cable drop voltage and prevent nuisance lockouts from occurring.

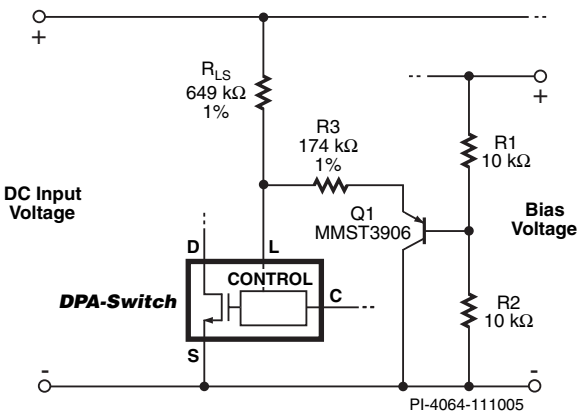

Figure 1. DPA-Switch with Wide Hysteresis UVLO.

Operation

This circuit takes advantage of accurate *DPA-Switch* L-pin current sensing as the basis for a new composite threshold, programmed for 42 VDC turn-on and 34 VDC turn-off. The *DPA-Switch* detects the input voltage via current in the L-pin resistor R_{LS}. Above an UV-on threshold (50 µA), the *DPA-Switch* begins switching and below an UV-off threshold (47 µA), the *DPA-Switch* is disabled. Transistor Q1 is turned on via bias resistor R2, causing a voltage drop across R3 and subtracting a fixed current of approximately 10 µA (moving the effective threshold to 60 µA) from the L-pin. When the power supply becomes operational, the bias voltage pulls up via R1, turning off Q1, cutting off the R3 current and returning to the default UV-off threshold (47 µA).

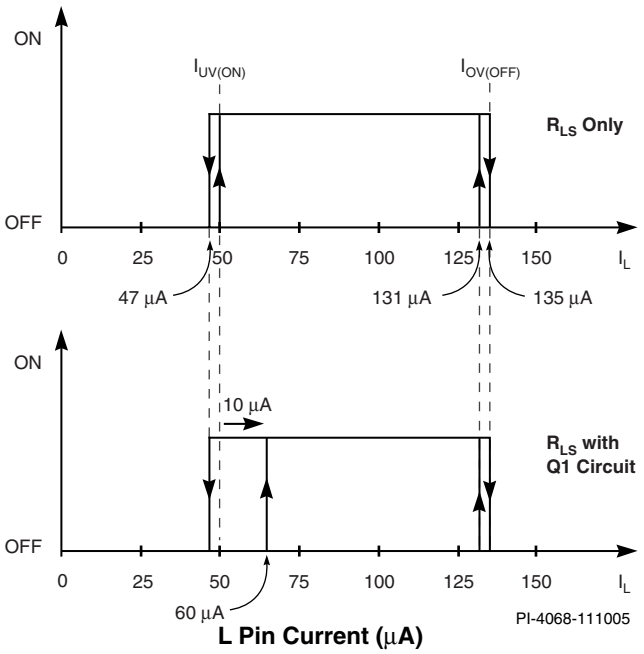

Figure 2. L-Pin Current without/with Wide UVLO Circuit.

*UNH-IOC test reports are available on the PI website www.powerint.com/poe

Design Formulae

Component values can be calculated according to the following formulae and parameters:

Design parameters were selected as follows:

V_{UV_ON} = 42 VDC	Input under-voltage on-threshold
V_{UV_OFF} = 34 VDC	Default under-voltage off-threshold
V_{DIN} = 1.4 VDC	Diode drop for PoE reverse protection input diodes
R1 = 10 kΩ	This value is assumed

From the *DPA-Switch* data sheet we have the following:

I_{UV_ON} = 50 µA	L-pin current for UV turn on
I_{UV_OFF} = 47 µA	L-pin current for UV turn off
V_L = 2.35 VDC	L-pin voltage at $I_L = I_{UV\_ON}$
V_C = 5.8 VDC	Control-pin voltage

We can assume:

$V_{Q1(BE)}$ = 0.6 VDC	Transistor base-emitter voltage
$V_{Q1(BE)REV}$ < 4 VDC	80% of the max reverse base-emitter voltage
β = 100	Transistor minimum current gain

Bias Voltage (V_{BIAS}) = 8 VDC

Resistor values R_{LS}, R2 and R3 are calculated as follows:

$$R_{LS} = \frac{V_{UV\_OFF} - V_L - V_{DIN}}{I_{UV\_OFF}}$$

$$R_3 = \frac{(V_L - V_{Q1(BE)}) \cdot R_{LS}}{V_{UV\_ON} - I_{UV\_ON} \cdot R_{LS} - V_L - V_{DIN}}$$

$$R_2 < \frac{R_1 \cdot (V_{Q1(BE)REV} + V_L)}{V_{BIAS} - V_L - V_{Q1(BE)REV}}$$

For design verification:

$$V_{UV\_ON} = \left(I_{UV\_ON} + \frac{V_L - V_{Q1(BE)}}{R_3}\right) \cdot R_{LS} + V_L + V_{DIN}$$

$$V_{UV\_OFF} = I_{UV\_OFF} \cdot R_{LS} + V_L + V_{DIN}$$

$$V_{OV\_OFF} = I_{OV\_OFF} \cdot R_{LS} + V_L + V_{DIN}$$

$$V_{Q1(BE)REV} = \frac{V_{BIAS} \cdot R_2}{R_1 + R_2} - V_L$$

Key Design Points

- Use a 1% resistor for R_{LS} to maintain the highest accuracy for the turn-on/turn-off thresholds.
- The over-voltage threshold is fixed at I_{OV_OFF} = 135 µA, and can be calculated according to the formula above (V_{OV_OFF}).
- The bias voltage (V_{BIAS}) is divided by R2 and R1. The reverse base emitter voltage $V_{Q1(BE)REV}$ is the divided bias voltage minus V_L. Make sure $V_{Q1(BE)REV}$ stays below 5 V (the transistor rating).
- For PoE applications, make sure to include voltage drops of input diodes (V_{DIN}) and pass-FET drop when calculating R_{LS}. For non-PoE applications, assume V_{DIN} = 0.
- Note: Due to the L-pin synchronization function (with a 1 V threshold), resistor R2 should be sufficiently large to prevent Q1 turn-on below L-pin voltage 1 V.

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